

# HD74HC589 ● 8-bit Serial or Parallel-input/Serial-output Shift Register (with 3-state outputs)

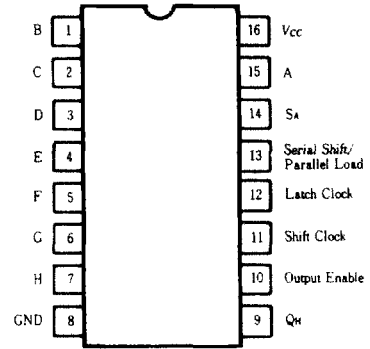
The HD74HC589 is similar in function to the HD74HC597, which is not a 3-state device.

This device consists of an 8-bit storage latch which feeds parallel data to an 8-bit shift register. Data can also be loaded serially (see Function Table). The shift register output,  $Q_H$ , is a three-state output, allowing this device to be used in bus-oriented systems.

## FEATURES

- High Speed Operation:  $t_{pd}$  (Shift Clock to  $Q_H$ )=15ns typ. ( $C_L=50pF$ )
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage:  $V_{CC}=2\sim 6V$
- Low Input Current:  $1\mu A$  max.
- Low Quiescent Supply Current:  $I_{CC}$  (static)= $4\mu A$  max. ( $T_a=25^\circ C$ )

## PIN ARRANGEMENT

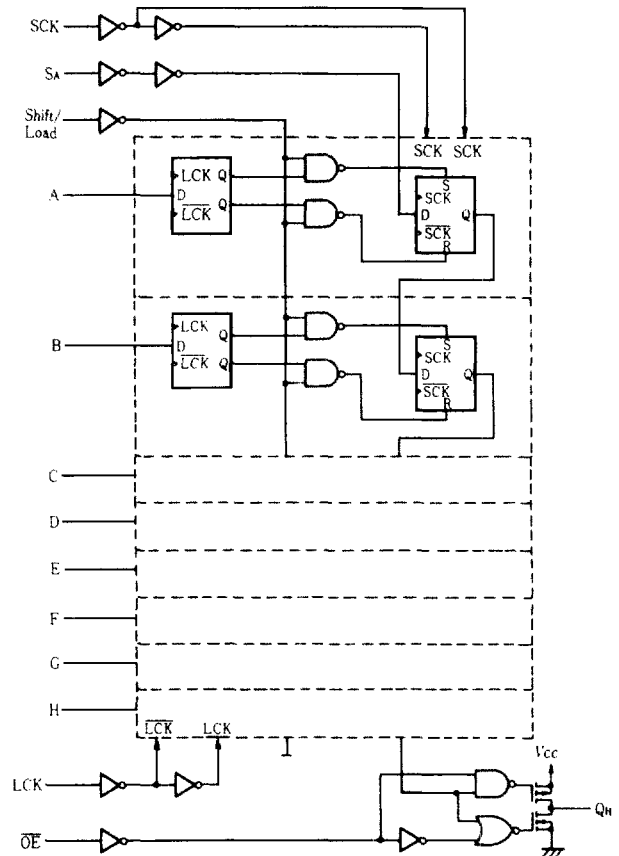


(Top View)

## FUNCTION TABLE

Latch Clock LCK	Shift Clock SCK	Serial Shift/ Parallel Load	Output Enable $\overline{OE}$	Function
	×	×	×	Data are loaded into input latches
	×	L	L	Data are loaded from input into shift registers
×	×	L	L	Data are transferred from input latches to shift registers
L,H,	L,H,	×	H	Outputs are disabled
×		H	L	Serial Shift $Q_n = Q_{n-1}$ . $Q_0 = SER$

## LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage Range	$V_{CC}$	-0.5~+7.0	V
Input Voltage	$V_{IH}$	-0.5~ $V_{CC}+0.5$	V
Output Voltage	$V_{OUT}$	-0.5~ $V_{CC}+0.5$	V
Output Current	$I_{OUT}$	±35	mA
DC Current Drain per $V_{CC}$ , GND	$I_{CC}$ , $I_{GND}$	±75	mA
DC Input Diode Current	$I_{IK}$	±20	mA
DC Output Diode Current	$I_{OK}$	±20	mA
Power Dissipation per Package	$P_T$	500	mW
Storage Temperature	$T_{stg}$	-65~+150	°C

■ DC CHARACTERISTICS

Item	Symbol	$V_{CC}(V)$	Test Conditions	$T_a = 25^\circ C$			$T_a = -40 \sim +85^\circ C$		Unit						
				min	typ	max	min	max							
Input Voltage	$V_{IH}$	2.0			1.5	—	—	1.5	—	V					
		4.5			3.15	—	—	3.15	—						
		6.0			4.2	—	—	4.2	—						
	$V_{IL}$	2.0			—	—	0.5	—	0.5	V					
		4.5			—	—	1.35	—	1.35						
		6.0			—	—	1.8	—	1.8						
Output Voltage	$V_{OH}$	2.0	$V_{IH} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20 \mu A$	1.9	2.0	—	1.9	—	V					
		4.5			4.4	4.5	—	4.4	—						
		6.0			5.9	6.0	—	5.9	—						
		4.5			4.18	—	—	4.13	—						
	$V_{OL}$			$V_{IH} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20 \mu A$	—	0.0	0.1	—	0.1	V				
						4.5	—	0.0	0.1	—		0.1			
						6.0	—	0.0	0.1	—		0.1			
						4.5	—	—	0.26	—		0.33			
						6.0			$I_{OL} = 7.8 mA$	—		—	0.26	—	0.33
Off-state output current	$I_{OZ}$	6.0	$V_{IH} = V_{IH}$ or $V_{IL}$ , $V_{OUT} = V_{CC}$ or GND	—	—	±0.5	—	±5.0	μA						
Input Current	$I_{in}$	6.0	$V_{IH} = V_{CC}$ or GND	—	—	±0.1	—	±1.0	μA						
Quiescent Supply Current	$I_{CC}$	6.0	$V_{IH} = V_{CC}$ or GND, $I_{out} = 0 \mu A$	—	—	4.0	—	40	μA						

■ AC CHARACTERISTICS (  $C_L=50\text{pF}$ , Input  $t_r=t_f=6\text{ns}$  )

Item	Symbol	$V_{CC}(V)$	Test Conditions	$T_a=25^\circ\text{C}$			$T_a=-40\sim+85^\circ\text{C}$		Unit
				min.	typ.	max.	min.	max.	
Maximum Clock Frequency	$f_{max}$	2.0		--	--	5	--	4	MHz
		4.5		--	--	27	--	21	
		6.0		--	--	32	--	25	
Propagation Delay Time	$t_{PLH}$ $t_{PHL}$	2.0	Latch Clock to $Q_H$	--	--	200	--	250	ns
		4.5		--	20	40	--	50	
		6.0		--	--	34	--	43	
	$t_{PLH}$ $t_{PHL}$	2.0	Shift Clock to $Q_H$	--	--	175	--	220	ns
		4.5		--	15	35	--	44	
		6.0		--	--	30	--	37	
	$t_{PLH}$ $t_{PHL}$	2.0	Serial Shift/Parallel Load to $Q_H$	--	--	175	--	220	ns
		4.5		--	16	35	--	44	
		6.0		--	--	30	--	37	
Output Enable Time	$t_{ZL}$ $t_{ZH}$	2.0		--	--	150	--	190	ns
		4.5		--	9	30	--	38	
		6.0		--	--	26	--	33	
Output Disable Time	$t_{LZ}$ $t_{HZ}$	2.0		--	--	150	--	190	ns
		4.5		--	14	30	--	38	
		6.0		--	--	26	--	33	
Pulse Width	$t_w$	2.0		80	--	--	100	--	ns
		4.5		16	8	--	20	--	
		6.0		14	--	--	17	--	
Setup Time	$t_{su}$	2.0	Data to Latch Clock	100	--	--	125	--	ns
		4.5		20	1	--	25	--	
		6.0		17	--	--	21	--	
	$t_{su}$	2.0	$S_A$ to Shift Clock	100	--	--	125	--	ns
		4.5		20	--	--	25	--	
		6.0		17	--	--	21	--	
	$t_{su}$	2.0	Serial Shift/Parallel Load to Shift Clock	100	--	--	125	--	ns
		4.5		20	--	--	25	--	
		6.0		17	--	--	21	--	
Hold Time	$t_h$	2.0	Latch Clock to Data	5	--	--	5	--	ns
		4.5		5	0	--	5	--	
		6.0		5	--	--	5	--	
	$t_h$	2.0	Shift Clock to $S_A$	5	--	--	5	--	ns
		4.5		5	--	--	5	--	
		6.0		5	--	--	5	--	
	$t_h$	2.0	Shift Clock to Serial Shift/Parallel Load	5	--	--	5	--	ns
		4.5		5	--	--	5	--	
		6.0		5	--	--	5	--	
Output Rise/Fall Time	$t_{TLH}$ $t_{THL}$	2.0		--	--	75	--	95	ns
		4.5		--	5	15	--	19	
		6.0		--	--	13	--	16	
Input Capacitance	$C_{in}$	--		--	5	10	--	10	pF