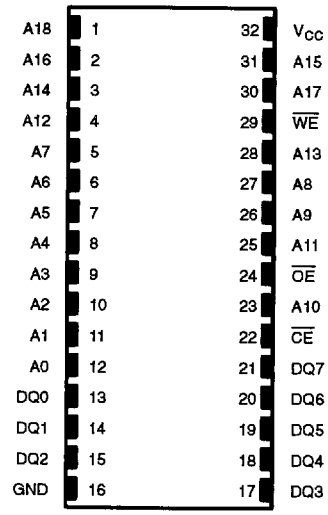
DALLAS SEMICONDUCTOR

DS1750Y
3–Volt Partitionable 4096K NV SRAM

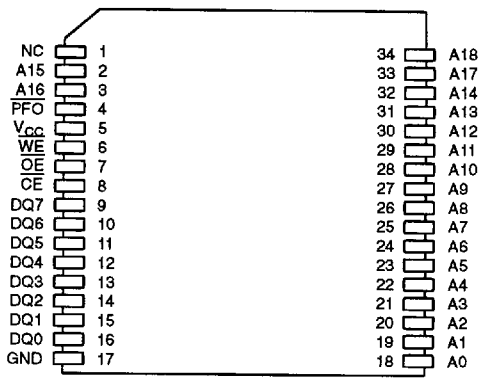
FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Directly replaces 512K x 8 volatile static RAM
- Write protects selected blocks of memory when programmed
- Unlimited write cycles
- Low-power CMOS
- 2.7 volt to 3.6 volt operation
- Read and write access times as fast as 150 ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Optional industrial temperature range of -40°C to +85°C, designated IND
- JEDEC standard 28-pin DIP package
- Low Profile Module (LPM) package
  - Fits into standard 68–pin PLCC surface mountable socket
  - 255 mils package height
  - Power Fail Output ($\overline{PFO}$) warns system of impending V_{CC} power failure

PIN ASSIGNMENT



32-PIN ENCAPSULATED PACKAGE
740 MIL EXTENDED



34–PIN LOW PROFILE MODULE (LPM)

PIN DESCRIPTION

A0 - A18	– Address Inputs
DQ0 - DQ7	– Data In/Data Out
$\overline{CE}$	– Chip Enable
$\overline{WE}$	– Write Enable
$\overline{OE}$	– Output Enable
$\overline{PFO}$	– Power Fail Output (LPM only)
V_{CC}	– Power (2.7 to 3.6 volts)
GND	– Ground
NC	– No Connect

DESCRIPTION

The DS1750 4096K Nonvolatile SRAMs, are 4,194,304-bit, fully static, nonvolatile SRAMs organized as 524,288 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. In addition, the device has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt programs and important data. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interfacing. DIP–package DS1750 devices can be used in place of existing 512K x 8 SRAMs directly conforming to the popular bytewide 32–pin DIP standard. DS1750 devices in the Low Profile Module package are specifically designed for surface mount applications. DS1750 LPM devices also have an additional pin, a Power Fail Output that can be used to warn a system of impending V_{CC} power failure.

READ MODE

The DS1750 devices execute a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (low). The unique address specified by the 19 address inputs (A_0 - A_{18}) defines which of the 524,288 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access.

WRITE MODE

The DS1750 devices excute a write cycle whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1750Y device provides full functional capability for V_{CC} greater than 2.70 volts and write protects by 2.50 volts. Data is maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAMs constantly monitor V_{CC}. Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become "don't care," and all outputs become high impedance. As V_{CC} falls below approximately 2.6 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 2.6 volts, the power switching circuit connects external V_{CC} to RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 2.70 volts.

FRESHNESS SEAL

Each DS1750 is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied and remains at a level greater than V_{TP}, the lithium energy source is enabled for battery backup operation.

PARTITION PROGRAMMING MODE

The register controlling the partitioning logic is selected by recognition of a specific binary pattern which is sent on address lines A15 - A18. These address lines are the four upper order address lines being sent to RAM. The pattern is sent by 20 consecutive read cycles with the exact pattern as shown in Table 1. Pattern matching must be accomplished using read cycles; any write cycles will reset the pattern matching circuitry. If this pattern is matched perfectly, then the 21st through 24th read cycles will load the partition register. Since there are 16 protectable partitions, the size of each partition is 512K/16 or 32K x 8. Each partition is represented by one of the 16 bits contained in the 21st through 24th read cycles as defined by A15 through A18 and shown in Table 2. A logical 1 in a bit location write protects the corresponding partition. A logical 0 in a bit location disables write protection. For example, if during the pattern match sequence bit 22 on address pin A16 was a 1, this would cause the partition register location for partition 5 to be set to a 1. This in turn would cause the DS1750 devices to internally inhibit $\overline{WE}$ when A18 A17 A16 A15=0101. Note that while programming the partition register, data which is being accessed from the RAM should be ignored, since the purpose of the 24 read cycles is to program the partition register, not to access data from RAM.

PATTERN MATCH TO WRITE PARTITION REGISTER Table 1

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A15	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A16	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
A17	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A18	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	X

FIRST BITS ENTERED

LAST BITS ENTERED

PARTITION REGISTER MAPPING Table 2

Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A_{14} A_{13} A_{12} A_{11})
A15	BIT 21	PARTITION 0	0000
A16	BIT 21	PARTITION 1	0001
A17	BIT 21	PARTITION 2	0010
A18	BIT 21	PARTITION 3	0011
A15	BIT 22	PARTITION 4	0100
A16	BIT 22	PARTITION 5	0101
A17	BIT 22	PARTITION 6	0110
A18	BIT 22	PARTITION 7	0111
A15	BIT 23	PARTITION 8	1000
A16	BIT 23	PARTITION 9	1001
A17	BIT 23	PARTITION 10	1010
A18	BIT 23	PARTITION 11	1011
A15	BIT 24	PARTITION 12	1100
A16	BIT 24	PARTITION 13	1101
A17	BIT 24	PARTITION 14	1110
A18	BIT 24	PARTITION 15	1111

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	0°C to 70°C, –40°C to +85°C for IND parts
Storage Temperature	–40°C to +70°C, –40°C to +85°C for IND parts
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1750Y Power Supply Voltage	V_{CC}	2.7		3.6	V	
Logic 1	V_{IH}	2.2		V_{CC}	V	
Logic 0	V_{IL}	0.0		+0.4	V	

DC ELECTRICAL CHARACTERISTICS

(t_A: See Note 10) (V_{CC}=2.7V to 3.6V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	µA	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	µA	
Output Current @ 2.2V	I_{OH}	-0.5			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	14
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}		5.0	7.0	mA	
Standby Current $\overline{CE}$ = V_{CC} - 0.5V	I_{CCS2}		3.0	4.0	mA	
Operating Current	I_{CCO1}			40	mA	
Write Protection Voltage	V_{TP}	2.50	2.60	2.70	V	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

AC ELECTRICAL CHARACTERISTICS

(t_A: See Note 10) (V_{CC}=2.7V to 3.6V)

PARAMETER	SYMBOL	DS1750Y-150		DS1750Y-200		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	150		200		ns	
Access Time	t_{ACC}		150		200	ns	
$\overline{OE}$ to Output Valid	t_{OE}		70		100	ns	
$\overline{CE}$ to Output Valid	t_{CO}		150		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Valid	t_{COE}	5		5		ns	5
Output High Z from Deselection	t_{OD}		50		50	ns	5
Output Hold from Address Change	t_{OH}	5		5		ns	
Write Cycle Time	t_{WC}	150		200		ns	
Write Pulse Width	t_{WP}	120		150		ns	3
Address Setup Time	t_{AW}	0		0		ns	
Write Recovery Time	t_{WR1} t_{WR2}	10 10		10 10		ns ns	12 13
Output High Z from $\overline{WE}$	t_{ODW}		50		50	ns	5
Output Active from $\overline{WE}$	t_{OEW}	5		5		ns	5
Data Setup Time	t_{DS}	60		80		ns	4
Data Hold Time	t_{DH1} t_{DH2}	10 10		10 10		ns ns	12 13

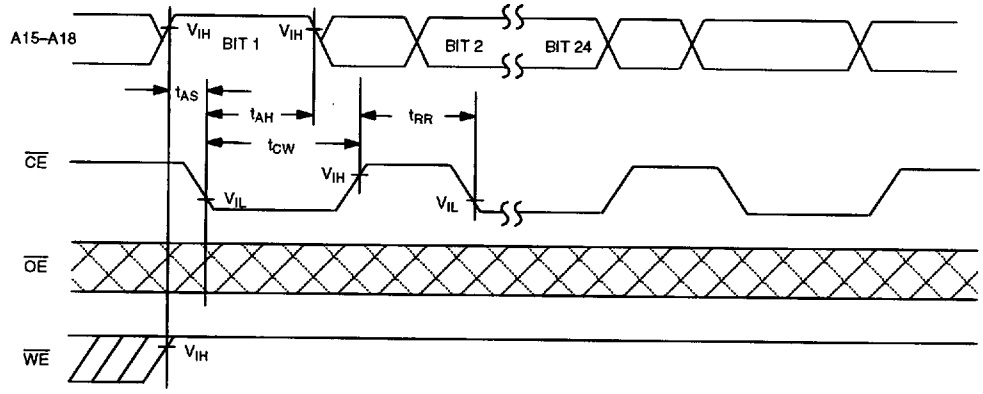
AC ELECTRICAL CHARACTERISTICS

(t_A: See Note 10) (V_{CC}=2.7V to 3.6V)*

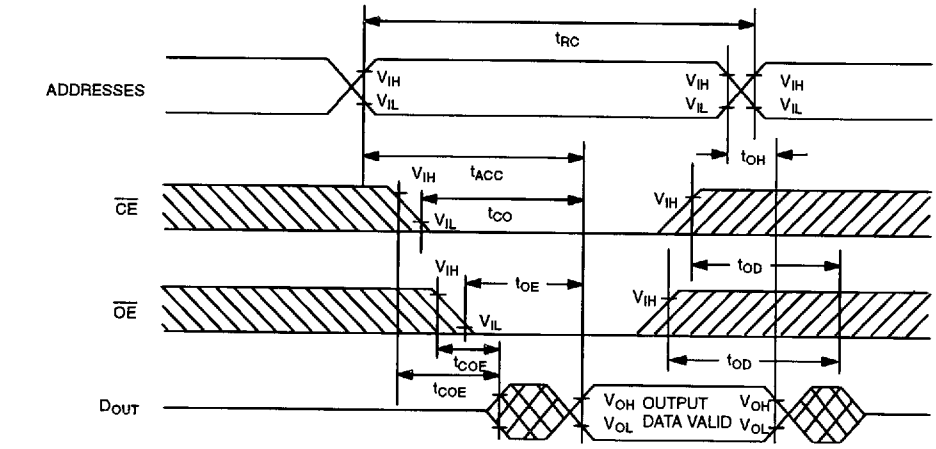
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	0			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	20			ns	
$\overline{CE}$ Pulse Width	t_{CW}	75			ns	

*For loading partition register

TIMING DIAGRAM: LOADING PARTITION REGISTER

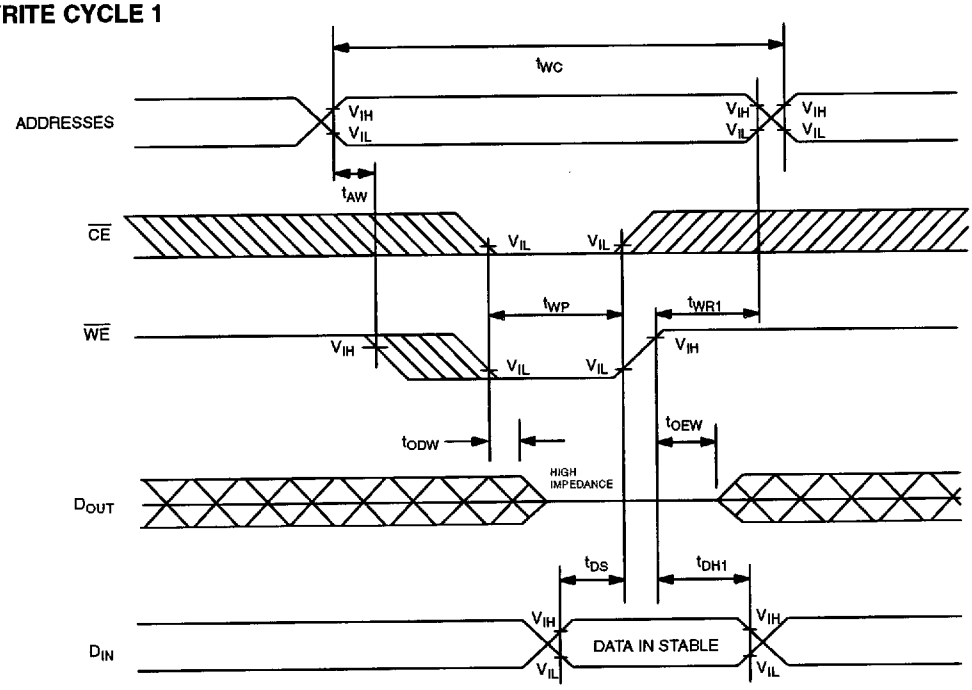


READ CYCLE



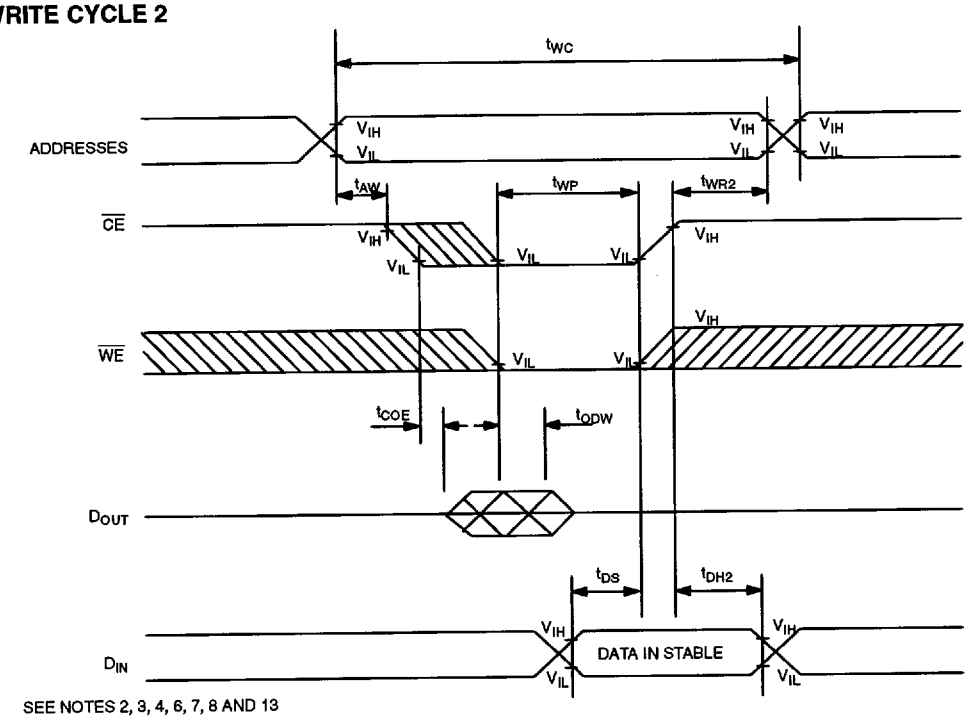
SEE NOTE 1

WRITE CYCLE 1



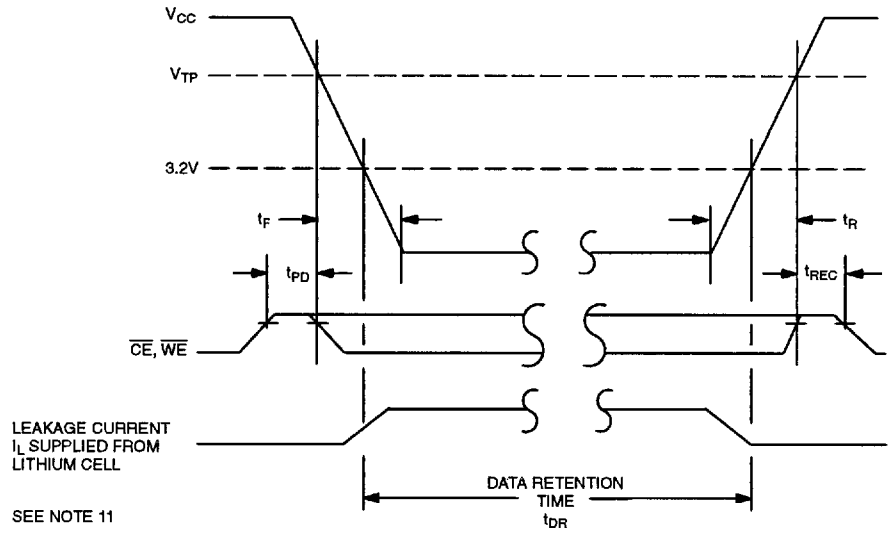
SEE NOTES 2, 3, 4, 6, 7, 8 AND 12

WRITE CYCLE 2



SEE NOTES 2, 3, 4, 6, 7, 8 AND 13

POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

(t_A: See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$, $\overline{WE}$ at V_{IH} before Power-Down	t_{PD}	0			µs	11
V_{CC} Slew from V_{TP} to 0V ($\overline{CE}$ at V_{IH})	t_F	300			µs	
V_{CC} Slew from 0V to V_{TP} ($\overline{CE}$ at V_{IH})	t_R	0			µs	
$\overline{CE}$, $\overline{WE}$ at V_{IH} after Power-Up	t_{REC}	100		200	ms	

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention Time	t_{DR}	10			years	9

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES:

1. $\overline{WE}$ is high for a read cycle.
2. $\overline{OE} = V_{IH}$ or V_{IL}. If $\overline{OE} = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{DS} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high impedance state during this period.
8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1750 has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For standard products, this range is 0°C to 70°C. For industrial products (IND), this range is –40°C to +85°C.
11. In a power down condition the voltage on any pin may not exceed the voltage on V_{CC}.
12. t_{WR1}, t_{DH1} are measured from $\overline{WE}$ going high.
13. t_{WR2}, t_{DH2} are measured from $\overline{CE}$ going high.
14. The power fail output signal ($\overline{PFO}$) is driven active (V_{OL}=0.4V) when the V_{CC} trip point occurs. While active, the $\overline{PFO}$ pin can sink 4 mA and will maintain a maximum output voltage of 0.4 volts. When inactive, the voltage output of $\overline{PFO}$ is 2.4 volts minimum and will source a current of 1 mA. This signal is only present on the LPM package variations.

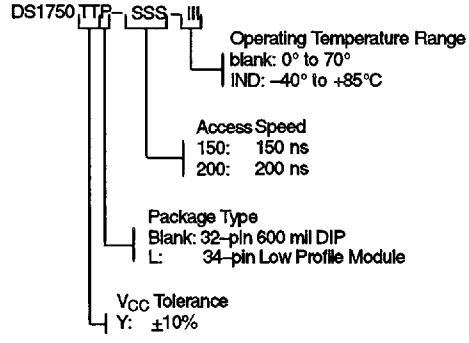
DC TEST CONDITIONS

Outputs Open
Cycle = 200 ns
All voltages are referenced to ground

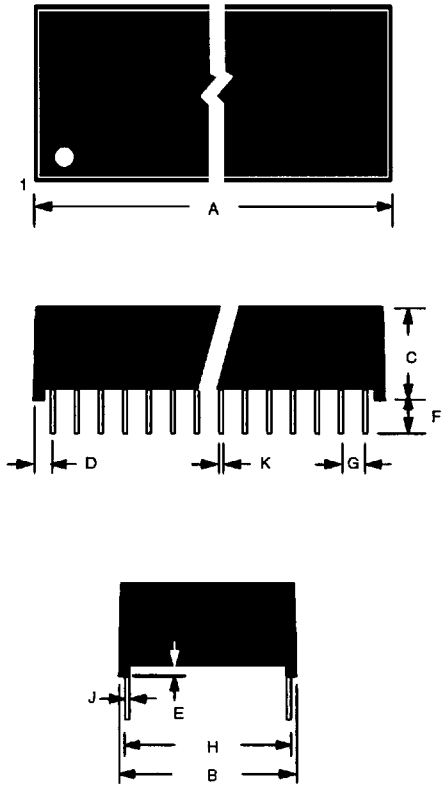
AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels:
  0.0 to 2.7 volts
Timing Measurement Reference Levels
  Input: 1.5V
  Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

ORDERING INFORMATION

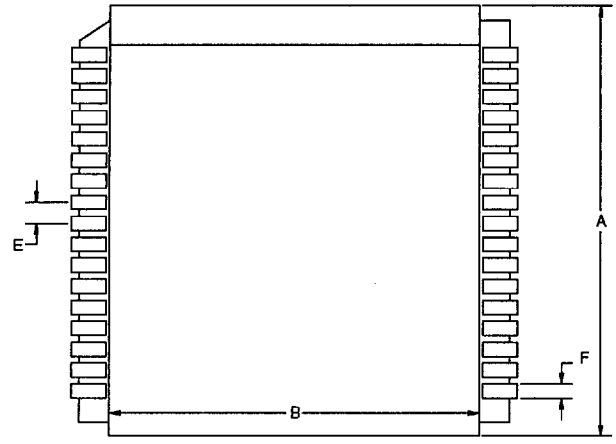


DS1750Y NONVOLATILE SRAM, 32–PIN 740 MIL EXTENDED MODULE

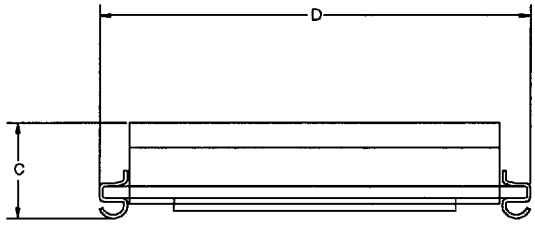


PKG	32-PIN	
DIM	MIN	MAX
A IN.	1.680	1.700
MM	42.67	43.18
B IN.	0.720	0.740
MM	18.29	18.80
C IN.	0.355	0.375
MM	9.02	9.52
D IN.	0.080	0.110
MM	2.03	2.79
E IN.	0.015	0.025
MM	0.38	0.63
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

DS1750Y 34–PIN LOW PROFILE MODULE (LPM)



PKG	INCHES	
DIM	MIN	MAX
A	0.955	0.980
B	0.840	0.855
C	0.230	0.250
D	0.975	0.995
E	0.047	0.053
F	0.015	0.025



Suggested 68–pin PLCC surface mountable sockets with leads on two sides only are:

McKenzie	PLCC34P–SMT–3
Harwin	HIS–40001–04
Robinson Nugent	PLCC–34–SMT
Dallas Semiconductor	DS34PIN–PLC

For recommended prototype/breadboard sockets, contact the Dallas Semiconductor factory.