## *Advance Product Information*

# *VSC836*

*2.5Gb/s*
*64x65 Crosspoint Switch*

## *Features*

- 64 Input by 65 Output Crosspoint Switch
- 2.5Gb/s NRZ Data Bandwidth
- 160Gb/s Aggregate Bandwidth
- TTL Compatible Control I/O
- PECL Compatible Data Inputs
- On-chip Input Terminations
- PECL Compatible Differential Output Driver
- Single 3.3V Supply, 28W Maximum Dissipation
- High Performance 35mm 440 BGA Package

## *General Description*

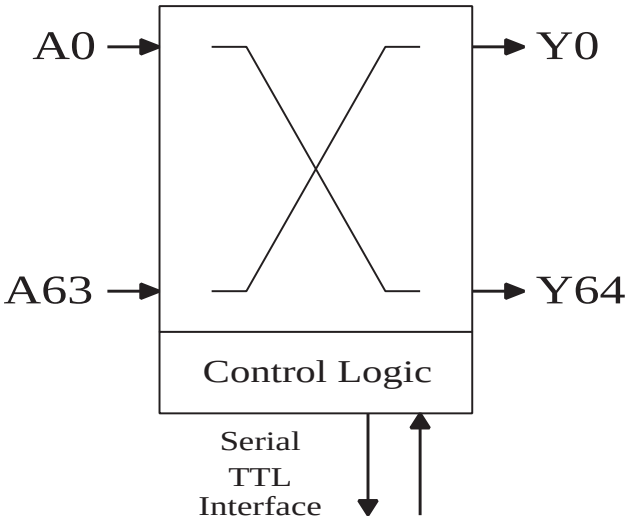
The VSC836 is a monolithic 64x65 asynchronous crosspoint switch, designed to carry broadband data streams up to 2.5Gb/s. The non-blocking switch core is programmed through a serial port interface that allows random access programming of each output port. A high degree of signal integrity is maintained through the chip through fully differential signal paths.

The crosspoint function is based on a multiplexer tree architecture. Each of the 65 data outputs is driven by a 64:1 multiplexer tree that can be programmed to any one of its 64 inputs, allowing one input to be multi-cast to several outputs. The signal path is asynchronous, so there are no restrictions on the phase, frequency, or signal pattern at each input, nor is any phase related clock required for retiming.

Each output driver is a fully differential switched current driver with on-die terminations for maximum signal integrity. Data inputs are terminated on die through 50 ohm resistors to an external $V_{TERM}$ supply.

The serial port interface uses TTL levels and provides separate pins for data input and output. Core programming can be sequential for each address or multiple program assignments can be queued and issued simultaneously.

## *VSC836 Block Diagram*







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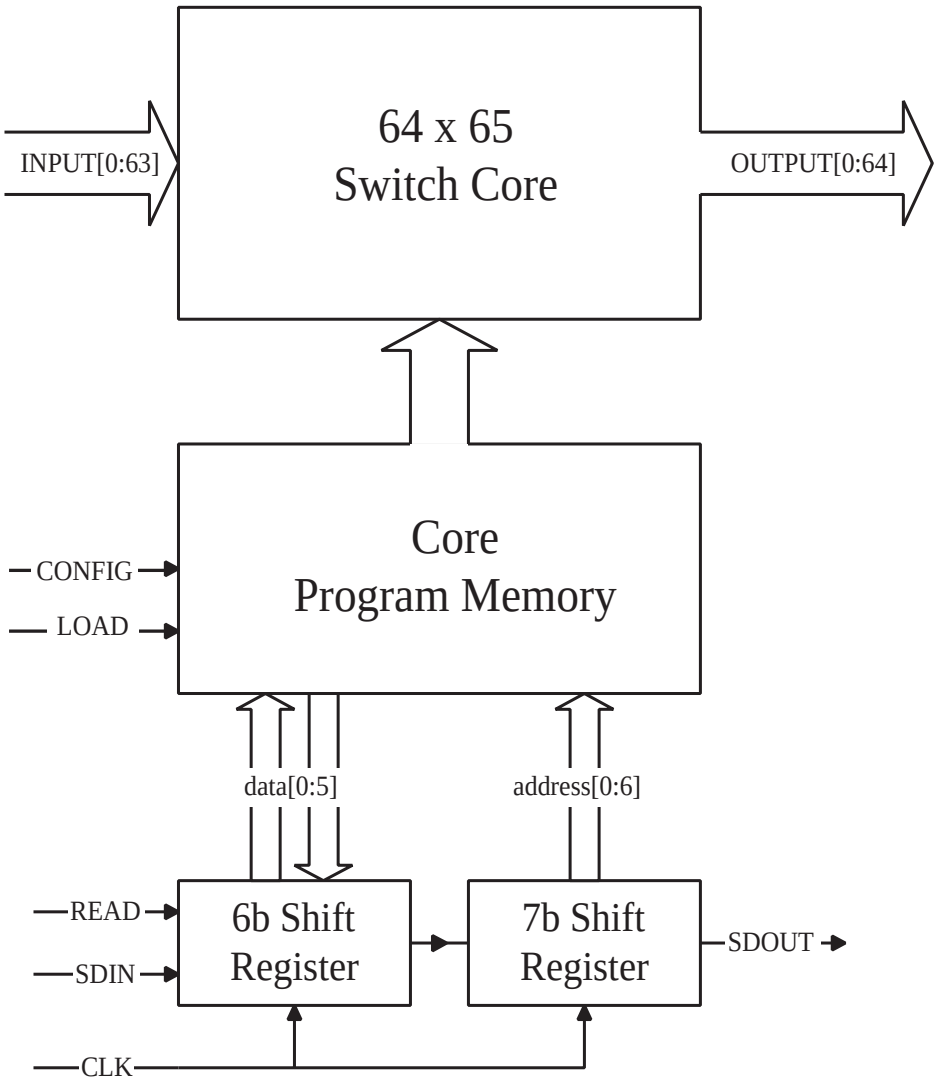
## *Functional Block Diagram*



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## Functional Description

### Input / Output Characteristics

All data inputs must be differential and biased to PECL levels. On-chip terminations are provided, with a nominal impedance of 50 ohms. All input termination resistors are tied to $V_{TERM}$. To minimize power dissipation, the $V_{TERM}$ supply should be biased within ±100mV of the input common mode voltage (nominally 2.0 volts). The recommended application for a DC coupled input is to float $V_{TERM}$ with an external bypass capacitor. Because the $V_{TERM}$ is common to all the inputs, care should be taken to minimize any common-mode noise between inputs. The $V_{TERM}$ supply can be biased below the input common-mode voltage at the expense of increased on-chip power dissipation.

Data outputs are provided through differential current switches with on-chip back-terminations. The drive level of the output circuit is designed to handle external 50 ohm termination. Although external termination is not required for correct functional operation, it is strongly recommended to assure proper signal levels and minimize reflections.

### Programming interface

The switch core is programmed through a serial interface circuit that allows sequential reads or writes to the program memory array. The program memory array is buffered to allow multiple programming instructions to be loaded simultaneously with the CONFIG pin.

The program data is composed of two parts: output pin address, and input pin address. The output pin address, denoted by A0 through A6, specifies which output channel is to be programmed. The input pin address, denoted by D0 through D5, specifies which input port the switch slice should connect to. The format of the program data is simple binary, where the binary value maps directly to the switch slice position and/or input port number. For example: program data 0000100/010110 would direct output channel Y4 to connect to input channel A22.

To program the switch core, the address and data (13 bits total) for the given output port must be serially clocked into the SDIN input. The LOAD pin must be asserted with the last serial program bit to load the program data into the on-chip program register. The program data will be held in the register until it is either reprogrammed or the chip is powered off. The last step to programming the switch core is to transfer the program data to the registers that control the state of each switch slice. The transfer is completed by asserting the CONFIG pin. The CONFIG pin can be used as a strobe to allow multiple program commands to be implemented simultaneously. The CONFIG pin can also be tied high (always asserted) so the core will reprogram after every LOAD pulse. Refer to Figure 1 illustrating typical write cycle sequence.

To read the current programming of the switch core, the desired address to query must be clocked into the chip's SDIN port. The format of the program data is the same as for writing. Because of the depth of the on-chip registers, the address bits must be followed by another 6 CLK cycles so the address data is correctly positioned in the internal register. The dummy bits that are clocked in during the last 6 bits of the program data will be overwritten when READ is asserted. As the last dummy bit is clocked in, the READ pin must be asserted to load the on-chip program data into the shift register used for the serial interface logic. Refer to Figure 2 illustrating the timing for a read sequence.




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**Figure 1: Write Cycle Timing**

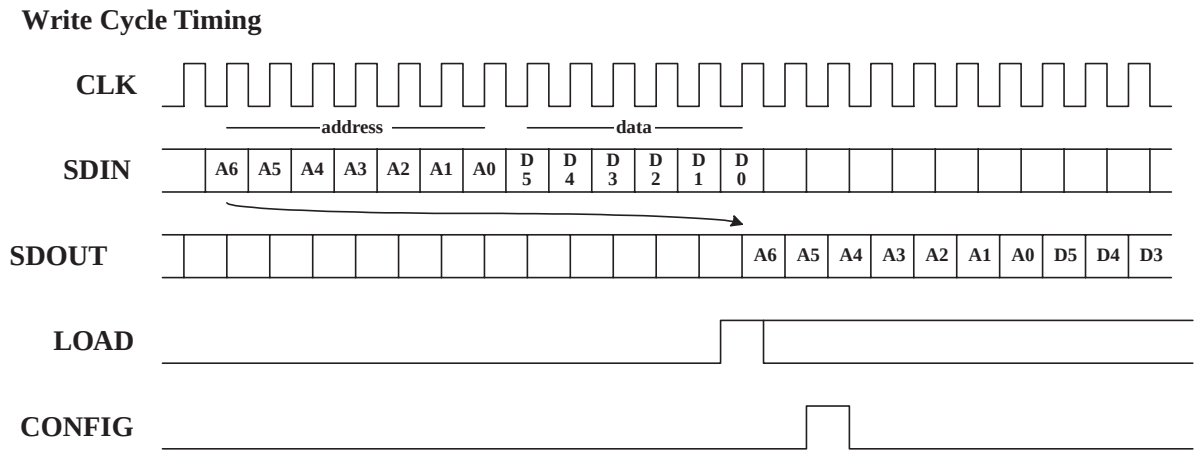
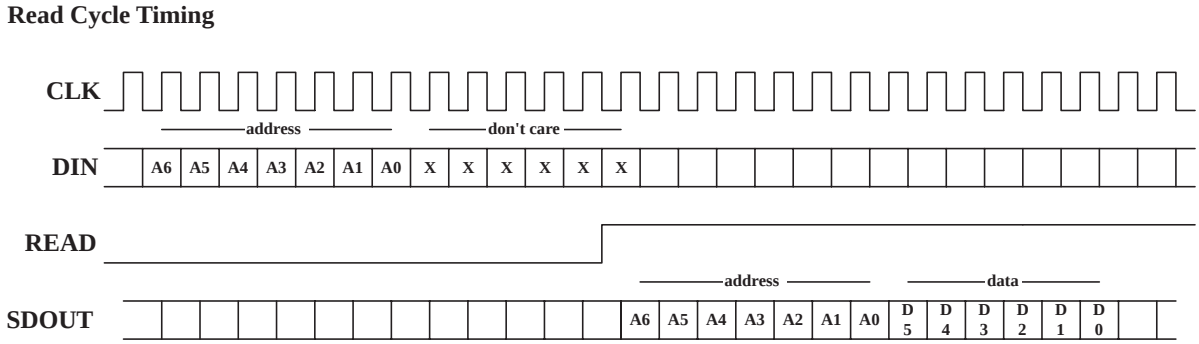



**Figure 2: Read Cycle Timing**



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## AC Characteristics

**Table 1: Data Path**

| *Parameter* | *Description* | *Min* | *Typ* | *Max* | *Units* |
|---|---|---|---|---|---|
| $F_{RATE}$ | Data rate | — | — | 2.5 | Gbits/s |
| $T_{SKW}$ | Channel to channel delay skew (1) | — | 1 | — | ns |
| $t_R$, $t_F$ | High-speed input rise/fall times, 20% to 80% | — | — | 150 | ps |
| $t_R$, $t_F$ | High-speed output rise/fall times, 20% to 80% | — | — | 150 | ps |
| $t_{jR}$ | Output delay jitter, rms (1) | — | — | 25 | ps |
| $t_{jP}$ | Output delay jitter, peak-peak (1) | — | — | 100 | ps |
| $t_{jP}$ | Output data eye jitter, peak-peak, $2^{31}$ PRBS (4) | - | - | 100 | ps |

*note: Unless otherwise stated, all specifications are guaranteed but not tested.*
*note 1: Skew between any two input channels to a given output.*
*note 2: Skew between any two output channels from the same input channel.*
*note 3: Required for high-speed output rise/fall spec at $F_{RATE}$=2.5 Gbits/s. For lower rate signals, use 0.375/$F_{RATE}$*
*note 4: Broadband jitter added to a jitter-free signal; jitter is primarily in the form of ISI for random data*

**Table 2: Program Interface**

| *Parameter* | *Description* | *Min* | *Typ* | *Max* | *Units* |
|---|---|---|---|---|---|
| $T_{PER(CLK)}$ | Serial clock period | 40 | — | — | ns |
| $T_{PW(CLK)}$ | Serial clock pulse width | 16 | — | — | ns |
| $T_{SU(SDIN)}$ | Serial data input setup time | 2 | — | — | ns |
| $T_{HO(SDIN)}$ | Serial data input hold time | 2 | — | — | ns |
| $T_{SU(READ)}$ | READ pulse setup time | 2 | — | — | ns |
| $T_{HO(READ)}$ | READ pulse hold time | 2 | — | — | ns |
| $T_{SU(LOAD)}$ | LOAD pulse setup time | 2 | — | — | ns |
| $T_{HO(LOAD)}$ | LOAD pulse hold time | 2 | — | — | ns |
| $T_{PD(SDOUT)}$ | Serial data output propagation delay (note 2) | — | — | 10 | ns |
| $T_{D(CONFIG)}$ | Configuration pulse delay time | 3 | — | — | ns |
| $T_{PW(CONFIG)}$ | Configuration pulse width | 30 | — | — | ns |
| $T_{PD(CONFIG)}$ | Configuration delay | — | — | 5 | ns |

*Note 1: Tested on a sample basis only.*
*Note 2: 20pF load.*




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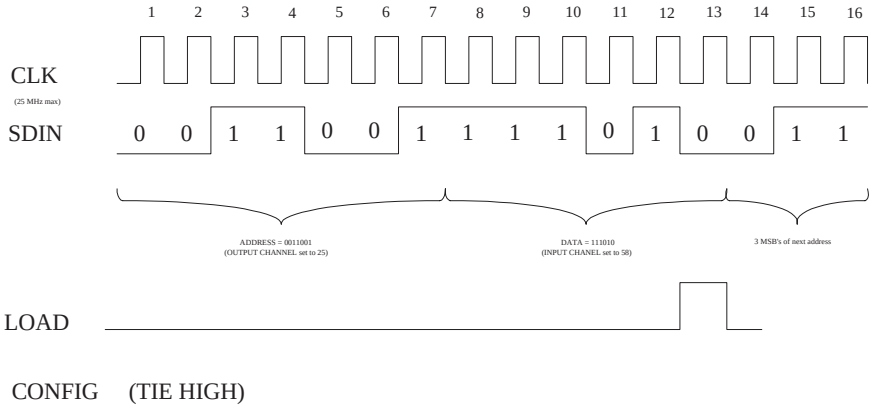
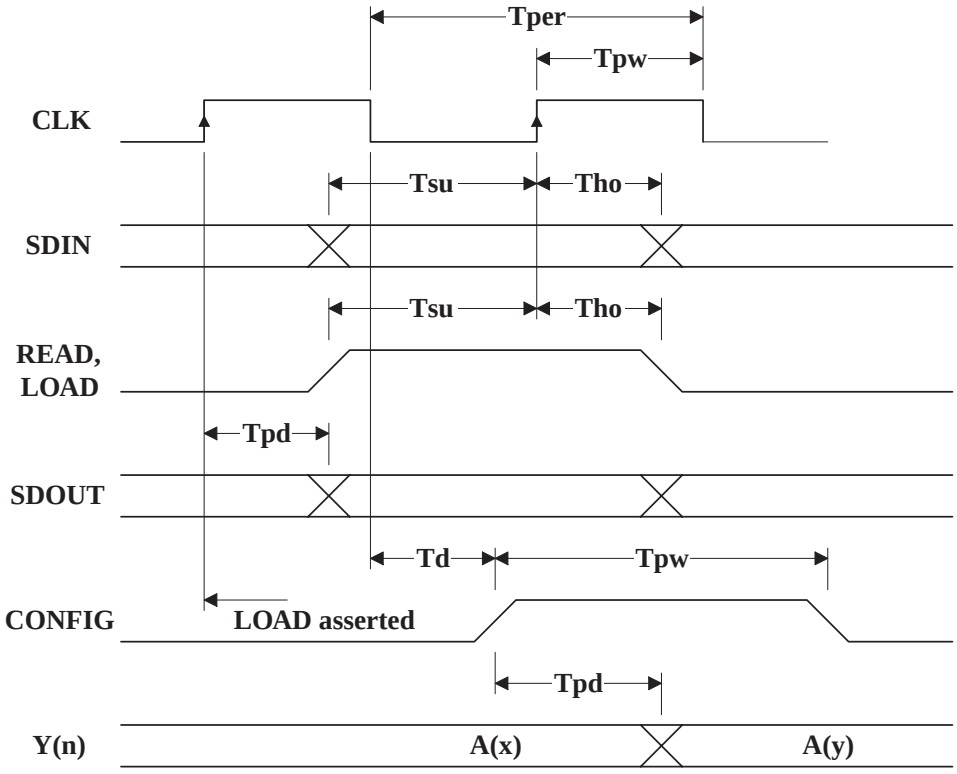
**Figure 3: Programming Example**




Serial programming example:
Connect output channel 25 to input channel 58

(all levels TTL)

**Figure 4: AC Timing Diagram**



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## DC Characteristics

**All characteristics are over the specified operating conditions.**

**Table 3: Power**

| *Parameter* | *Description* | *Max* | *Units* |
|---|---|---|---|
| $I_{CC}$ | $V_{CC}$ supply current | 5400 | mA |
| $I_{CCP}$ | $V_{CCP}$ supply current | 2600 | mA |
| $I_{TERM}$ | $V_{TERM}$ supply current | +/-512 | mA |
| $P_T$ | Total chip power ($I_{TERM}$=0) | 28 | W |

*Note: Specified with outputs terminated with 50 ohms to +2.0 volts.*

**Table 4: Program Input Levels (TTL)**

| *Parameter* | *Description* | *Min* | *Typ* | *Max* | *Units* | *Conditions* |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH voltage (TTL) | 2.0 | — | 3.5 | V | — |
| $V_{IL}$ | Input LOW voltage (TTL) | 0 | — | 0.8 | V | — |
| $I_{IH}$ | Input HIGH current (TTL) | — | — | 500 | µA | $V_{IN}$ = 2.4V |
| $I_{IL}$ | Input LOW current (TTL) | — | — | -500 | µA | $V_{IN}$ = 0.5V |
| Voh | Output HIGH voltage (TTL) | 2.4 | — | — | V | $I_{OH}$ = -2mA |
| Vol | Output LOW voltage (TTL) | — | — | 0.4 | V | $I_{OL}$ = 2mA |

**Table 5: Data Input Levels (Differential PECL)**

| *Parameter* | *Description* | *Min* | *Typ* | *Max* | *Units* | *Conditions* |
|---|---|---|---|---|---|---|
| $V_{ID}$ | Input differential voltage | 400 | — | 1000 | mV | single-ended measurement |
| $V_{ICM}$ | Input common-mode voltage | 1.8 | — | 2.3 | V | $V_{TERM}$=$V_{CC}$-1.3V |

**Table 6: Data Output Levels (Differential PECL)**

| *Parameter* | *Description* | *Min* | *Typ* | *Max* | *Units* | *Conditions* |
|---|---|---|---|---|---|---|
| $V_{OD}$ | Output differential voltage | 600 | — | 1000 | mV | note 1 |
| $V_{OCM}$ | Output common-mode voltage | 1.8 | — | 2.3 | V | note 1 |

*note 1: VCC=VCCP=3.3V, VEE=0*




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## Absolute Maximum Ratings

Power Supply Voltage ($V_{CC}$) Potential to GND ..... -0.5 V to +4.0 V
TTL Input Voltage Applied ..... -0.5 V to Vcc+0.5 V
ECL Input Voltage Applied ..... -0.5 V to $V_{CC}$ +0.5 V
Output Current ($I_{OUT}$) ..... 50 mA
Case Temperature Under Bias ($T_C$) ..... $-55^o$ to + $125^o$C
Storage Temperature ($T_{STG}$) ..... $-65^o$ to + $150^o$C

*Note: Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.*

## Operating Conditions

Supply voltage ($V_{EE}$) ..... 0 V
Supply voltage ($V_{CC}$) ..... +3.3V ±5%
Supply voltage ($V_{CCP}$) ..... +3.3V ±5%
Termination voltage ($V_{TERM}$) ..... $V_{CC}$-1.3V
Case Temperature Operating Range ($T$) ..... $0^o$ to $85^o$C

## ESD Ratings

Proper ESD procedures should be used when handling this product. The VSC836 is rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 1000V.



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## Package Pin Descriptions

**Figure 5: .Functional Pinout Floorplan**

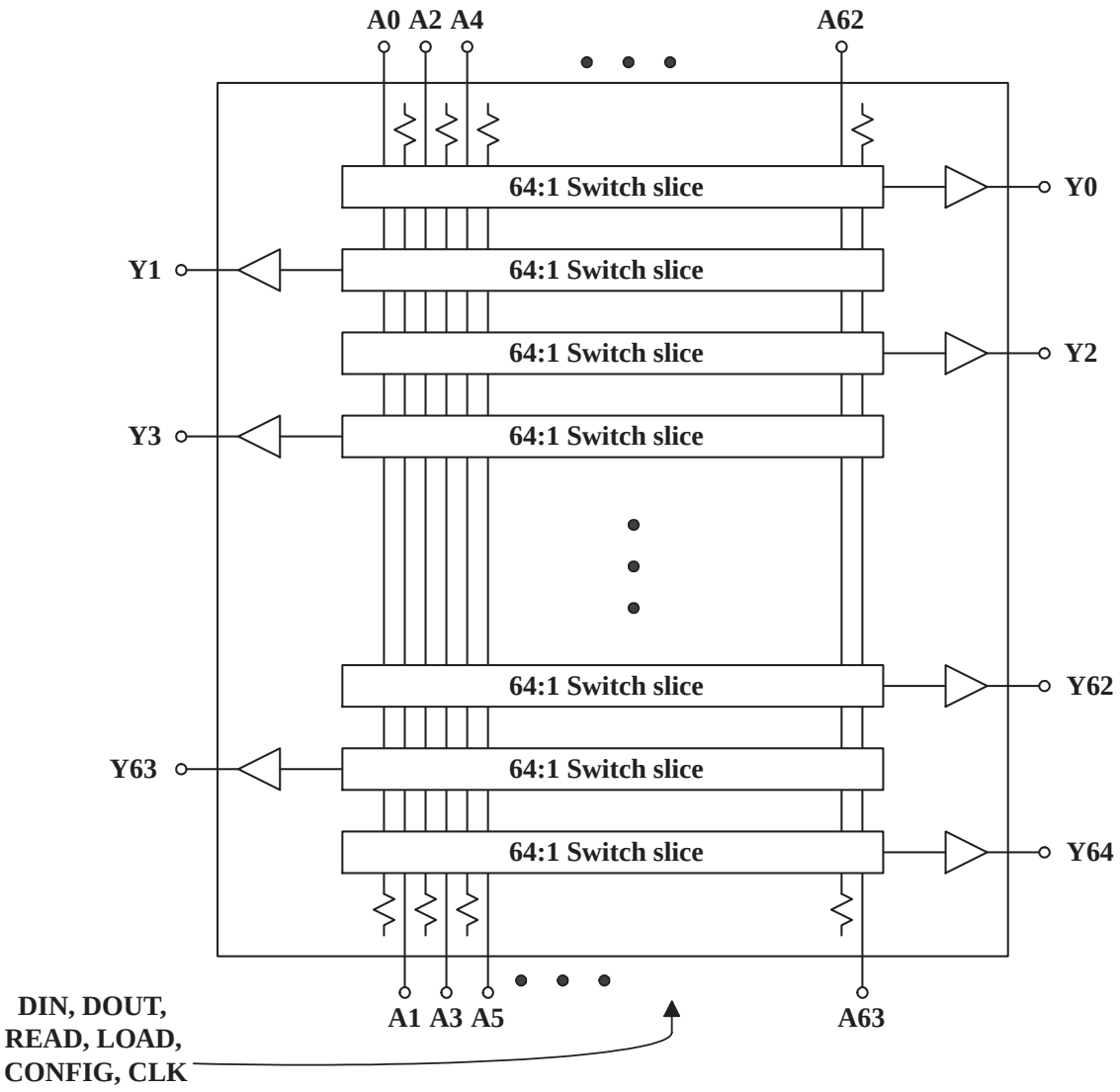





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**Figure 6: Pinout Diagram**

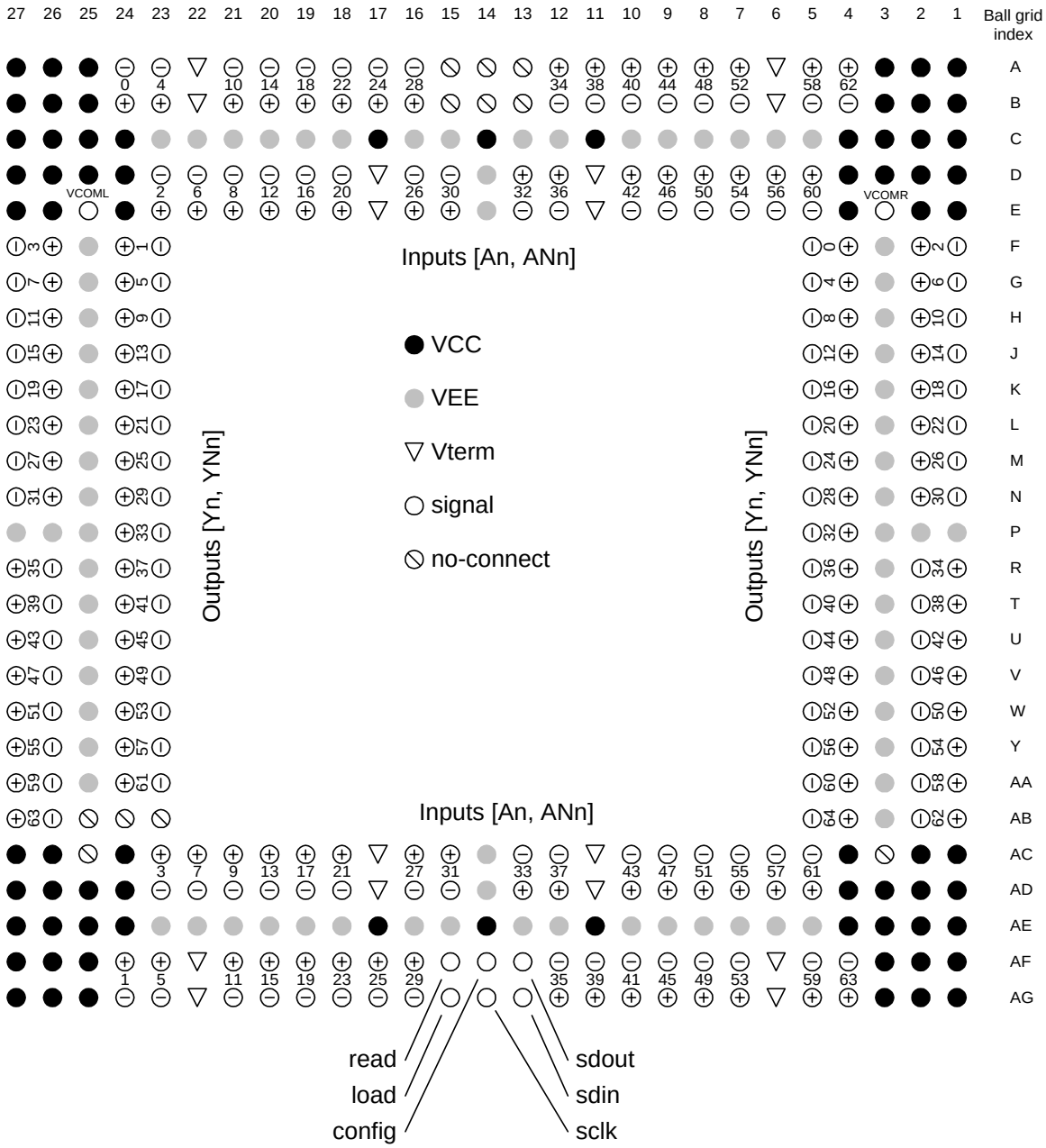




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**Table 7: Package Pin Identification**

| *Signal Name* | *Pin* | *Function* | *Level* |
|---|---|---|---|
| | ***High Speed Data Inputs*** | | |
| A0, NA0 | B24, A24 | Data Input | PECL |
| A1, NA1 | AF24, AG24 | Data Input | PECL |
| A2, NA2 | E23, D23 | Data Input | PECL |
| A3, NA3 | AC23, AD23 | Data Input | PECL |
| A4, NA4 | B23, A23 | Data Input | PECL |
| A5, NA5 | AF23, AG23 | Data Input | PECL |
| A6, NA6 | E22, D22 | Data Input | PECL |
| A7, NA7 | AC22, AD22 | Data Input | PECL |
| A8, NA8 | E21, D21 | Data Input | PECL |
| A9, NA9 | AC21, AD21 | Data Input | PECL |
| A10, NA10 | B21, A21 | Data Input | PECL |
| A11, NA11 | AF21, AG21 | Data Input | PECL |
| A12, NA12 | E20, D20 | Data Input | PECL |
| A13, NA13 | AC20, AD20 | Data Input | PECL |
| A14, NA14 | B20, A20 | Data Input | PECL |
| A15, NA15 | AF20, AG20 | Data Input | PECL |
| A16, NA16 | E19, D19 | Data Input | PECL |
| A17, NA17 | AC19, AD19 | Data Input | PECL |
| A18, NA18 | B19, A19 | Data Input | PECL |
| A19, NA19 | AF19, AG19 | Data Input | PECL |
| A20, NA20 | E18, D18 | Data Input | PECL |
| A21, NA21 | AC18, AD18 | Data Input | PECL |
| A22, NA22 | B18, A18 | Data Input | PECL |
| A23, NA23 | AF18, AG18 | Data Input | PECL |
| A24, NA24 | B17, A17 | Data Input | PECL |
| A25, NA25 | AF17, AG17 | Data Input | PECL |
| A26, NA26 | E16, D16 | Data Input | PECL |
| A27, NA27 | AC16, AD16 | Data Input | PECL |
| A28, NA28 | B16, A16 | Data Input | PECL |
| A29, NA29 | AF16, AG16 | Data Input | PECL |
| A30, NA30 | E15, D15 | Data Input | PECL |
| A31, NA31 | AC15, AD15 | Data Input | PECL |
| A32, NA32 | D13, E13 | Data Input | PECL |
| A33, NA33 | AD13, AC13 | Data Input | PECL |
| A34, NA34 | A12, B12 | Data Input | PECL |
| A35, NA35 | AG12, AF12 | Data Input | PECL |




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| *Signal Name* | *Pin* | *Function* | *Level* |
|---|---|---|---|
| A36, NA36 | D12, E12 | Data Input | PECL |
| A37, NA37 | AD12, AC12 | Data Input | PECL |
| A38, NA38 | A11, B11 | Data Input | PECL |
| A39, NA39 | AG11, AF11 | Data Input | PECL |
| A40, NA40 | A10, B10 | Data Input | PECL |
| A41, NA41 | AG10, AF10 | Data Input | PECL |
| A42, NA42 | D10, E10 | Data Input | PECL |
| A43, NA43 | AD10, AC10 | Data Input | PECL |
| A44, NA44 | A9, B9 | Data Input | PECL |
| A45, NA45 | AG9, AF9 | Data Input | PECL |
| A46, NA46 | D9, E9 | Data Input | PECL |
| A47, NA47 | AD9, AC9 | Data Input | PECL |
| A48, NA48 | A8, B8 | Data Input | PECL |
| A49, NA49 | AG8, AF8 | Data Input | PECL |
| A50, NA50 | D8, E8 | Data Input | PECL |
| A51, NA51 | AD8, AC8 | Data Input | PECL |
| A52, NA52 | A7, B7 | Data Input | PECL |
| A53, NA53 | AG7, AF7 | Data Input | PECL |
| A54, NA54 | D7, E7 | Data Input | PECL |
| A55, NA55 | AD7, AC7 | Data Input | PECL |
| A56, NA56 | D6, E6 | Data Input | PECL |
| A57, NA57 | AD6, AC6 | Data Input | PECL |
| A58, NA58 | A5, B5 | Data Input | PECL |
| A59, NA59 | AG5, AF5 | Data Input | PECL |
| A60, NA60 | D5, E5 | Data Input | PECL |
| A61, NA61 | AD5, AC5 | Data Input | PECL |
| A62, NA62 | A4, B4 | Data Input | PECL |
| A63, NA63 | AG4, AF4 | Data Input | PECL |
| ***High Speed Data Outputs*** | | | |
| Y0, YN0 | F4, F5 | Data Output | PECL |
| Y1, YN1 | F24, F23 | Data Output | PECL |
| Y2, YN2 | F2, F1 | Data Output | PECL |
| Y3, YN3 | F26, F27 | Data Output | PECL |
| Y4, YN4 | G4, G5 | Data Output | PECL |
| Y5, YN5 | G24, G23 | Data Output | PECL |
| Y6, YN6 | G2, G1 | Data Output | PECL |
| Y7, YN7 | G26, G27 | Data Output | PECL |
| Y8, YN8 | H4, H5 | Data Output | PECL |



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| *Signal Name* | *Pin* | *Function* | *Level* |
|---|---|---|---|
| Y9, YN9 | H24, H23 | Data Output | PECL |
| Y10, YN10 | H2, H1 | Data Output | PECL |
| Y11, YN11 | H26, H27 | Data Output | PECL |
| Y12, YN12 | J4, J5 | Data Output | PECL |
| Y13, YN13 | J24, J23 | Data Output | PECL |
| Y14, YN14 | J2, J1 | Data Output | PECL |
| Y15, YN15 | J26, J27 | Data Output | PECL |
| Y16, YN16 | K4, K5 | Data Output | PECL |
| Y17, YN17 | K24, K23 | Data Output | PECL |
| Y18, YN18 | K2, K1 | Data Output | PECL |
| Y19, YN19 | K26, K27 | Data Output | PECL |
| Y20, YN20 | L4, L5 | Data Output | PECL |
| Y21, YN21 | L24, L23 | Data Output | PECL |
| Y22, YN22 | L2, L1 | Data Output | PECL |
| Y23, YN23 | L26, L27 | Data Output | PECL |
| Y24, YN24 | M4, M5 | Data Output | PECL |
| Y25, YN25 | M24, M23 | Data Output | PECL |
| Y26, YN26 | M2, M1 | Data Output | PECL |
| Y27, YN27 | M26, M27 | Data Output | PECL |
| Y28, YN28 | N4, N5 | Data Output | PECL |
| Y29, YN29 | N24, N23 | Data Output | PECL |
| Y30, YN30 | N2, N1 | Data Output | PECL |
| Y31, YN31 | N26, N27 | Data Output | PECL |
| Y32, YN32 | P4, P5 | Data Output | PECL |
| Y33, YN33 | P24, P23 | Data Output | PECL |
| Y34, YN34 | R1, R2 | Data Output | PECL |
| Y35, YN35 | R27, R26 | Data Output | PECL |
| Y36, YN36 | R4, R5 | Data Output | PECL |
| Y37, YN37 | R24, R23 | Data Output | PECL |
| Y38, YN38 | T1, T2 | Data Output | PECL |
| Y39, YN39 | T27, T26 | Data Output | PECL |
| Y40, YN40 | T4, T5 | Data Output | PECL |
| Y41, YN41 | T24, T23 | Data Output | PECL |
| Y42, YN42 | U1, U2 | Data Output | PECL |
| Y43, YN43 | U27, U26 | Data Output | PECL |
| Y44, YN44 | U4, U5 | Data Output | PECL |
| Y45, YN45 | U24, U23 | Data Output | PECL |
| Y46, YN46 | V1, V2 | Data Output | PECL |
| Y47, YN47 | V27, V26 | Data Output | PECL |




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| *Signal Name* | *Pin* | *Function* | *Level* |
|---|---|---|---|
| Y48, YN48 | V4, V5 | Data Output | PECL |
| Y49, YN49 | V24, V23 | Data Output | PECL |
| Y50, YN50 | W1, W2 | Data Output | PECL |
| Y51, YN51 | W27, W26 | Data Output | PECL |
| Y52, YN52 | W4, W5 | Data Output | PECL |
| Y53, YN53 | W24, W23 | Data Output | PECL |
| Y54, YN54 | Y1, Y2 | Data Output | PECL |
| Y55, YN55 | Y27, Y26 | Data Output | PECL |
| Y56, YN56 | Y4, Y5 | Data Output | PECL |
| Y57, YN57 | Y24, Y23 | Data Output | PECL |
| Y58, YN58 | AA1, AA2 | Data Output | PECL |
| Y59, YN59 | AA27, AA26 | Data Output | PECL |
| Y60, YN60 | AA4, AA5 | Data Output | PECL |
| Y61, YN61 | AA24, AA23 | Data Output | PECL |
| Y62, YN62 | AB1, AB2 | Data Output | PECL |
| Y63, YN63 | AB27, AB26 | Data Output | PECL |
| Y64, YN64 | AB4, AB5 | Data Output | PECL |
| ***Serial Programming Port*** | | | |
| SDIN | AG13 | Serial program data input | TTL |
| SCLK | AG14 | Serial programming clock | TTL |
| LOAD | AG15 | Serial input load strobe | TTL |
| CONFIG | AF14 | Switch configuration strobe | TTL |
| READ | AF15 | Programming read/write control | TTL |
| SDOUT | AF13 | Serial data output | TTL |



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| *Signal Name* | *Pin* | *Function* | *Level* |
|---|---|---|---|
| | | ***Power Supplies*** | |
| VCC | A1, A2, A25, A26, A27, A3, AC1, AC2, AC24, AC26, AC27, AC4, AD1, AD2, AD24, AD25, AD26, AD27, AD3, AD4, AE1, AE11, AE14, AE17, AE2, AE24, AE25, AE26, AE27, AE3, AE4, AF1, AF2, AF25, AF26, AF27, AF3, AG1, AG2, AG25, AG26, AG27, AG3, B1, B2, B25, B26, B27, B3, C1, C11, C14, C17, C2, C24, C25, C26, C27, C3, C4, D1, D2, D24, D25, D26, D27, D3, D4, E1, E2, E24, E26, E27, E4 | Power | +3.3V |
| VEE | AC14, AD14, AE10, AE12, AE13, AE15, AE16, AE18, AE19, AE20, AE21, AE22, AE23, AE5, AE6, AE7, AE8, AE9, C10, C12, C13, C15, C16, C18, C19, C20, C21, C22, C23, C5, C6, C7, C8, C9, D14, E14, P1, P2, P26, P27 | Power | GND |
| VEEP0 | F3 | Power for Y0, YN0, Y2, YN2 | GND |
| VEEP1 | F25 | Power for Y1, YN1, Y3, YN3 | GND |
| VEEP2 | G3 | Power for Y4, YN4, Y6, YN6 | GND |
| VEEP3 | G25 | Power for Y5, YN5, Y7, YN7 | GND |
| VEEP4 | H3 | Power for Y8, YN8, Y10, YN10 | GND |
| VEEP5 | H25 | Power for Y9, YN9, Y11, YN11 | GND |
| VEEP6 | J3 | Power for Y12, YN12, Y14, YN14 | GND |
| VEEP7 | J25 | Power for Y13, YN13, Y15, YN15 | GND |
| VEEP8 | K3 | Power for Y16, YN16, Y18, YN18 | GND |

| *Signal Name* | *Pin* | *Function* | *Level* |
|---|---|---|---|
| VEEP9 | K25 | Power for Y17, YN17, Y19, YN19 | GND |
| VEEP10 | L3 | Power for Y20, YN20, Y22, YN22 | GND |
| VEEP11 | L25 | Power for Y21, YN21, Y23, YN23 | GND |
| VEEP12 | M3 | Power for Y24, YN24, Y26, YN26 | GND |
| VEEP13 | M25 | Power for Y25, YN25, Y27, YN27 | GND |
| VEEP14 | N3 | Power for Y28, YN28, Y30, YN30 | GND |
| VEEP15 | N25 | Power for Y29, YN29, Y31, YN31 | GND |
| VEEP16 | P3 | Power for Y32, YN32, Y34, YN34 | GND |
| VEEP17 | P25 | Power for Y33, YN33, Y35, YN35 | GND |
| VEEP18 | R3 | Power for Y36, YN36, Y38, YN38 | GND |
| VEEP19 | R25 | Power for Y37, YN37, Y39, YN39 | GND |
| VEEP20 | T3 | Power for Y40, YN40, Y42, YN42 | GND |
| VEEP21 | T25 | Power for Y41, YN41, Y43, YN43 | GND |
| VEEP22 | U3 | Power for Y44, YN44, Y46, YN46 | GND |
| VEEP23 | U25 | Power for Y45, YN45, Y47, YN47 | GND |
| VEEP24 | V3 | Power for Y48, YN48, Y50, YN50 | GND |
| VEEP25 | V25 | Power for Y49, YN49, Y51, YN51 | GND |
| VEEP26 | W3 | Power for Y52, YN52, Y54, YN54 | GND |
| VEEP27 | W25 | Power for Y53, YN53, Y55, YN55 | GND |
| VEEP28 | Y3 | Power for Y56, YN56, Y58, YN58 | GND |
| VEEP29 | Y25 | Power for Y57, YN57, Y59, YN59 | GND |



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| *Signal Name* | *Pin* | *Function* | *Level* |
|---|---|---|---|
| VEEP30 | AA3 | Power for Y60, YN60, Y62, YN62 | GND |
| VEEP31 | AA25 | Power for Y61, YN61, Y63, YN63 | GND |
| VEEP32 | AB3 | Power for Y64, YN64, Y66, YN66 | GND |
| VTERM0 | AC17, AD17, AF22, AG22 | Termination supply for A0 - AN28 | +2.0V |
| VTERM1 | A22, B22, D17, E17 | Termination supply for A1 - AN31 | +2.0V |
| VTERM2 | AC11, AD11, AF6, AG6 | Termination supply for A34 - NA62 | +2.0V |
| VTERM3 | A6, B6, D11, E11 | Termination supply for A33 - NA63 | +2.0V |
| ***Misc.*** | | | |
| VCOML | E25 | Slicing level for Y1 - YN61 | ANALOG |
| VCOMR | E3 | Slicing level for Y0 - YN64 | ANALOG |




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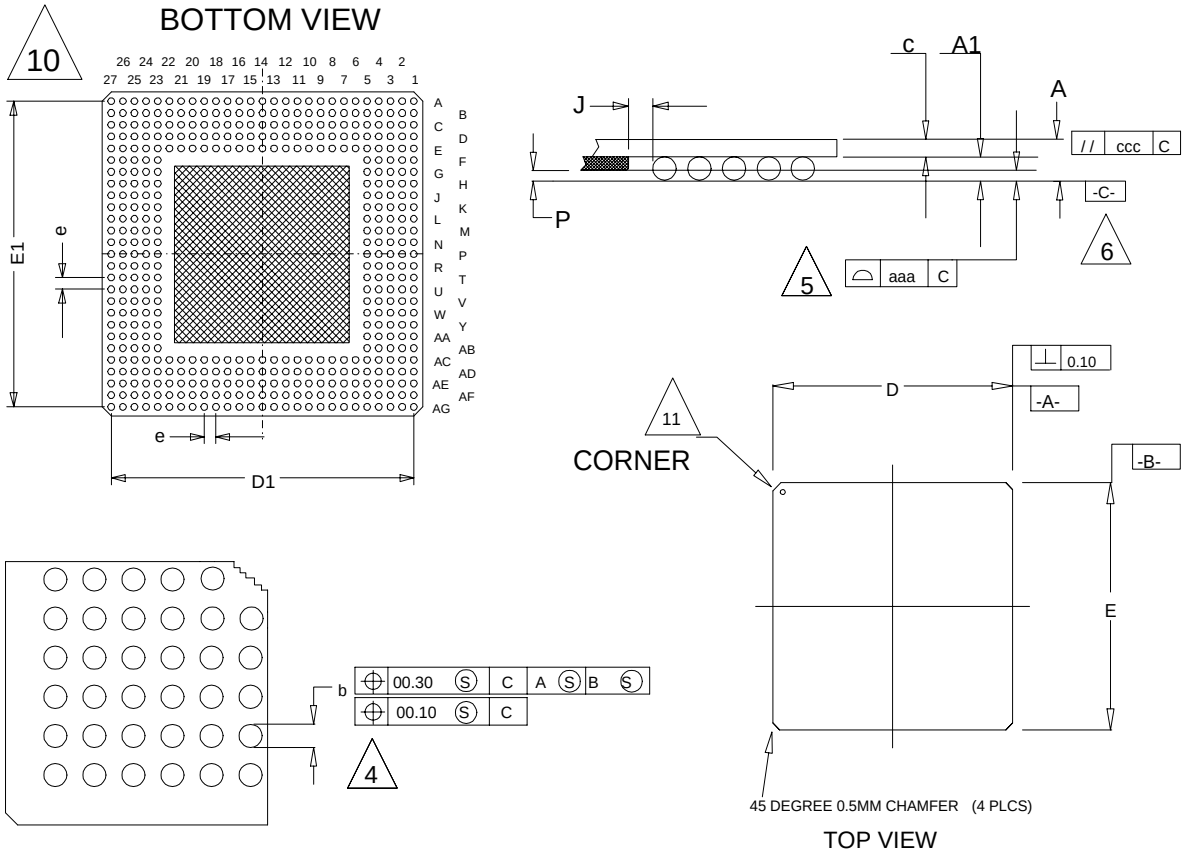
## *Package Information*

**Figure 7: 35mm 440 BGA Package Drawing**




| DIMENSIONAL REFERENCES | | | |
|---|---|---|---|
| REF. | MIN. | NOM. | MAX. |
| A | 1.65 | 1.80 | 1.95 |
| A1 | 0.60 | 0.65 | 0.70 |
| D | 34.80 | 35.00 | 35.20 |
| D1 | | 33.02 (BSC.) | |
| | | | |
| E | 34.80 | 35.00 | 35.20 |
| E1 | | 33.02 (BSC.) | |
| | | | |
| b | 0.65 | 0.75 | 0.85 |
| c | 1.05 | 1.15 | 1.25 |
| | | | |
| M | | 27 | |
| N | | 440 | |
| aaa | | | 0.15 |
| ccc | | | 0.15 |
| e | | 1.27 TYP. | |
| P | | | 0.25 |
| J | 0.25 | | |

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NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. "M" REPRESENTS THE BASIC SOLDER BALL MATRIX SIZE, AND SYMBOL "N" IS THE MAXIMUM ALLOWABLE NUMBER OF BALLS AFTER DEPOPULATING.
4. "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM -C- .
5. DIMENSION "aaa" IS MEASURED PARALLEL TO PRIMARY DATUM -C- .
6. PRIMARY DATUM -C- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. PACKAGE SURFACE SHALL BE NICKEL PLATED.
8. AFTER SURFACE MOUNT ASSEMBLY, SOLDER BALL WILL HAVE 0.15mm(TYP.) COLLAPSE IN "A" DIMENSION.
9. SUBSTRATE MATERIAL BASE IS COPPER.
10. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF PACKAGE BODY
11. 45 DEG. 0.5mm CHAMFER CORNER AND WHITE DOT FOR PIN 1 IDENTIFICATION
12. ENCAPSULANT SIZE MAY VARY WITH DIE SIZE.
13. CAVITY DEPTH C1 VARIOUS WITH DIE THICKNESS.



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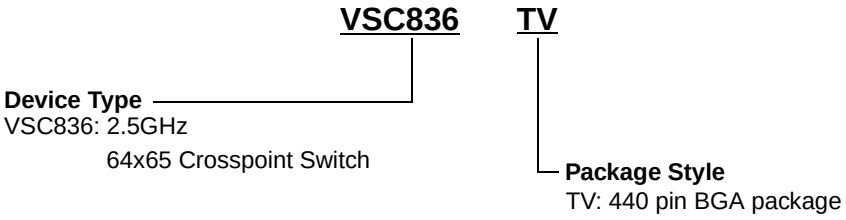
## Ordering Information

The order number for this product is formed by a combination of the device number, and package type.




### Notice

This document contains information about a new product during its fabrication or early sampling phase of development. The information in this document is based on design targets, simulation results or early prototype test results. Characteristic data and other specifications are subject to change without notice. Therefore the reader is cautioned to confirm that this datasheet is current prior to design or order placement.

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