Preliminary **RF3754**

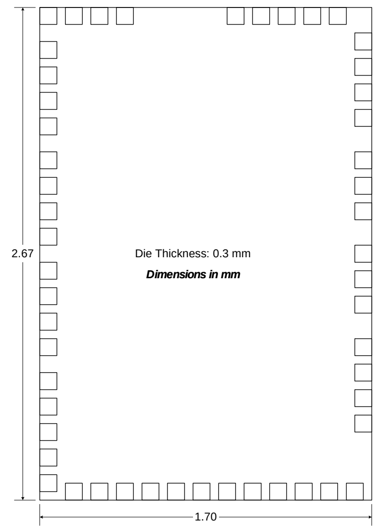
QUAD-CHANNEL VCSEL LASER DRIVER (4x3.125Gbps)

Typical Applications

- Quad-Channel Gigabit and 10Gigabit Ethernet Optical Transceivers
- CWDM/WWDM 4-Channel Parallel Links
- SONET VSR & System Interconnect
- All Fiber Optic Transceiver Applications up to 3.125Gbps Serial Data Rate

Product Description

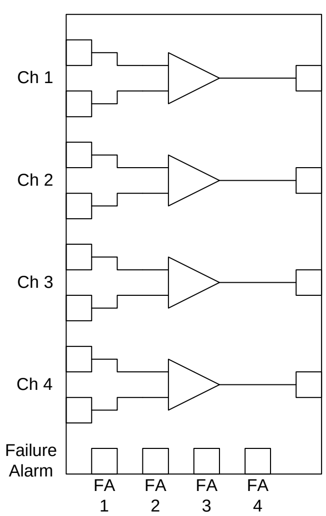
The RF3754 is a quad-channel integrated laser driver intended to drive an 850nm VCSEL. The RF3754 features four differential input and single-ended output optimized for line rates of 2.5Gbps to 3.125Gbps with low power consumption. All four channels operate with +3.3V and 264mΩ quiescent power dissipation. Laser bias is supplied from 2mA to 25mA per channel and modulating currents from 1mA to 18mA per channel. The device may be used in 4-fiber or 4-wavelength quad-channel fiber optic transceiver applications operating up to 3.125Gbps/channel. The RF3754 contains a bias generator, laser modulator, and failure alarm. APC maintains constant average optical output power by adjusting the laser bias current to offset temperature effects and laser aging. The RF3754 is available in bare die configuration.



Package Style: Bare Die

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☑ SiGe HBT
- ☐ Si CMOS
- ☐ GaInP/HBT
- ☐ GaN HEMT
- ☐ SiGe Bi-CMOS



Functional Block Diagram

Features

- +3.3V Supply Voltage, 80mA Quiescent Current
- Common Cathode Laser Driver
- 1mA to 18mA Laser Modulation Current
- 2mA to 25mA Laser Bias Current Control Range

Ordering Information

RF3754 Quad-Channel VCSEL Laser Driver (4x3.125Gbps)

RF Micro Devices, Inc.
7628 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	4	V_{DC}
Input Voltage	4	V_{P-P}
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-65 to +125	°C
Junction Temperature	+125	°C

Note: TA=+25°C unless otherwise noted. Functional operation near or above Maximum Ratings is not implied. Exposure to stress levels at or near maximum ratings for any period of time may affect reliability or cause permanent damage to the devices.

Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Inputs					T=25°C, V_{CC}=3.3V, V_{IN}=500mV$_{P-P}$, Data Rate=3.125Gbps, Single Channel
Data Rate, BR	0.1	3.125	4	Gbps	
Supply Voltage, V	3.0	3.3	3.6	V	
Quiescent Current, I_Q		20	25	mA	
		80		mA	All four channels powered on
Total Current, I_{TOT}	16	30	68	mA	$I_{TOT}=I_Q+I_{BIAS}+I_{MOD}$
Differential Input Impedance, R_{IN}	90	100	110	Ω	
Differential Input V Swing, V_{INDIFF}	50		1500	mV$_{P-P}$	
Outputs					
Laser Bias Current, I_{BIAS}	2		25	mA	Ext R Bias Set
Laser Modulation Current, I_{MOD}	1		18	mA	Ext R Modset
Output Rise/Fall Time, t_{rOUT}, t_{fOUT}		50	70	pS	Electrical Rise and Fall Time at 10%/90%
Output Skew, $dt_{Latency}$		15	20	pS	
Output Random Jitter, RJ_{P-P}		10	20	pS	
Output Undershoot/Overshoot			20	%	
Alarm Out Hi, Alrm		V_{CC}			
Alarm Out Low, Alrm		Gnd			
Time to Enable, T_{ON}		0.005	1	mS	
Time to Disable, T_{OFF}		8	10	uS	
Time to Fault, T_{FAULT}		5	50	uS	
Crosstalk		PASS			Mask test with 20dB adjacent channel to input channel power ratio tolerance.
Current Control					
Laser Bias Current Control Range, R_{BIAS}		2000	20,000	Ω	Ext R Bias Set
Laser Modulation Current Control Range, R_{MOD}	0		10,000	Ω	Ext R Modset

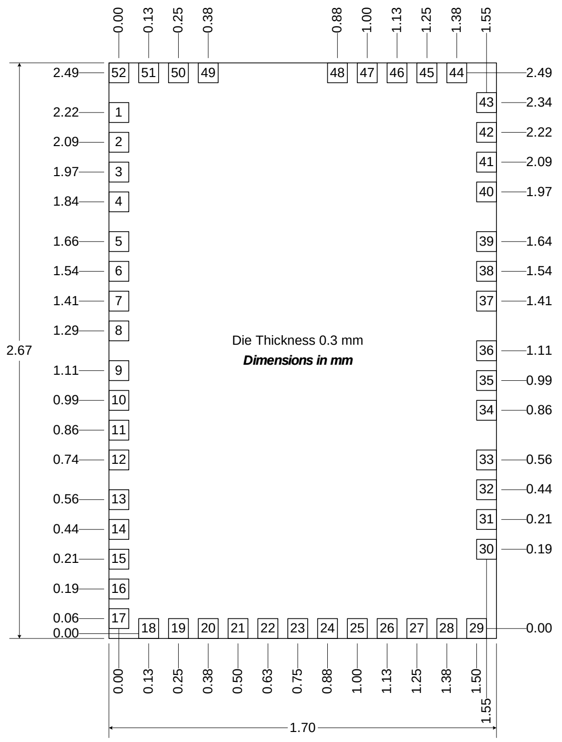
Laser Alarm Table

TX Disable	System State	Alarm Out
0V to 1.3V	Normal	Gnd
0V to 1.3V	Failure of Photo or Laser Diode	V_{CC}
1.4V to V_{CC}	N/A	V_{CC}

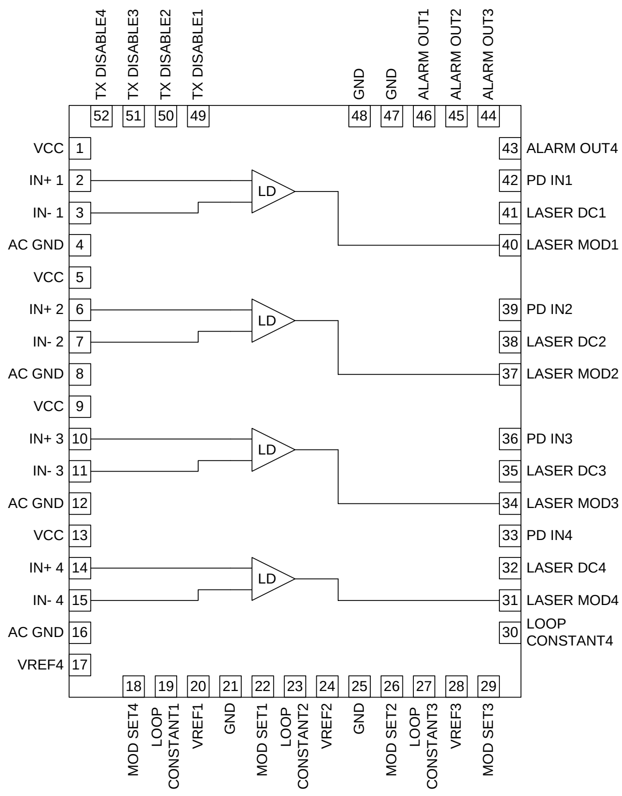
Pin	Function	Description	Bond Pad Center Coordinates (xmm, ymm)
1	VCC	Voltage supply, +3.3V	(0,2.22)
2	IN+ 1	Input pin for channel 1, positive polarity of differential pair.	(0,2.09)
3	IN- 1	Input pin for channel 1, negative polarity of differential pair.	(0,1.97)
4	AC GND	DC voltage is present on this pin. When grounding this pin, a DC blocking capacitor must be used.	(0,1.84)
5	VCC	Voltage supply, +3.3V	(0,1.66)
6	IN+ 2	Input pin for channel 2, positive polarity of differential pair.	(0,1.54)
7	IN- 2	Input pin for channel 2, negative polarity of differential pair.	(0,1.41)
8	AC GND	DC voltage is present on this pin. When grounding this pin, a DC blocking capacitor must be used.	(0,1.29)
9	VCC	Voltage supply, +3.3V	(0,1.11)
10	IN+ 3	Input pin for channel 3, positive polarity of differential pair.	(0,0.99)
11	IN- 3	Input pin for channel 3, negative polarity of differential pair.	(0,0.86)
12	AC GND	DC voltage is present on this pin. When grounding this pin, a DC blocking capacitor must be used.	(0,0.74)
13	VCC	Voltage supply, +3.3V	(0,0.56)
14	IN+ 4	Input pin for channel 4, positive polarity of differential pair.	(0,0.44)
15	IN- 4	Input pin for channel 4, negative polarity of differential pair.	(0,0.31)
16	AC GND	DC voltage is present on this pin. When grounding this pin, a DC blocking capacitor must be used.	(0,0.19)
17	VREF4	On-chip reference voltage for channel 4.	(0,0.06)
18	MOD SET4	Sets laser modulation current for channel 4 by external resistor or potentiometer.	(0.13,0)
19	LOOP CONSTANT1	Control loop capacitor, maintain loop constant on channel 1.	(0.25,0)
20	VREF1	On-chip reference voltage for channel 4.	(0.38,0)
21	GND	Ground connection. For best results, keep traces physically short and connect immediately to ground plane.	(0.50,0)
22	MOD SET1	Sets laser modulation current for channel 1 by external resistor or potentiometer.	(0.63,0)
23	LOOP CONSTANT2	Control loop capacitor, maintain loop constant on channel 2.	(0.75,0)
24	VREF2	On-chip reference voltage for channel 2.	(0.88,0)
25	GND	Ground connection. For best results, keep traces physically short and connect immediately to ground plane.	(1.00,0)
26	MOD SET2	Sets laser modulation current for channel 2 by external resistor or potentiometer.	(1.13,0)
27	LOOP CONSTANT3	Control loop capacitor, maintain loop constant on channel 3.	(1.25,0)
28	VREF3	On-chip reference voltage for channel 3.	(1.38,0)
29	MOD SET3	Sets laser modulation current for channel 3 by external resistor or potentiometer.	(1.50,0)
30	LOOP CONSTANT4	Control loop capacitor, maintain loop constant on channel 4.	(1.55,0.19)
31	LASER MOD4	Laser modulation current for channel 4.	(1.55,0.31)
32	LASER DC4	DC laser bias current for channel 4.	(1.55,0.44)
33	PD IN4	Input from anode of photodiode for control loop for channel 4.	(1.55,0.56)

Pin	Function	Description	Bond Pad Center Coordinates (xmm, ymm)
34	LASER MOD3	Laser modulation current for channel 3.	(1.55,0.86)
35	LASER DC3	DC laser bias current for channel 3.	(1.55,0.98)
36	PD IN3	Input from anode of photodiode for control loop for channel 3.	(1.55,1.11)
37	LASER MOD2	Laser modulation current for channel 2.	(1.55,1.41)
38	LASER DC2	DC laser bias current for channel 2.	(1.55,1.54)
39	PD IN2	Input from anode of photodiode for control loop for channel 2.	(1.55,1.66)
40	LASER MOD1	Laser modulation current for channel 1.	(1.55,1.97)
41	LASER DC1	DC laser bias current for channel 1.	(1.55,2.09)
42	PD IN1	Input from anode of photodiode for control loop for channel 1.	(1.55,2.22)
43	ALARM OUT4	Alarm signal for channel 4.	(1.55,2.34)
44	ALARM OUT3	Alarm signal for channel 3.	(1.38,2.49)
45	ALARM OUT2	Alarm signal for channel 2.	(1.25, 2.49)
46	ALARM OUT1	Alarm signal for channel 1.	(1.13,2.49)
47	GND	Ground connection. For best results, keep traces physically short and connect immediately to ground plane.	(1.00,2.49)
48	GND	Ground connection. For best results, keep traces physically short and connect immediately to ground plane.	(0.88,2.49)
49	TX DISABLE1	Disables laser driver channel 1 output.	(0.38,2.49)
50	TX DISABLE2	Disables laser driver channel 2 output.	(0.25,2.49)
51	TX DISABLE3	Disables laser driver channel 3 output.	(0.13,2.49)
52	TX DISABLE4	Disables laser driver channel 4 output.	(0,2.49)
Pkg Base	GND	Ground connection. For best results, keep traces physically short and connect immediately to ground plane.	

Die Package Drawing



Detailed Functional Block Diagram



Theory of Operation and Application Information

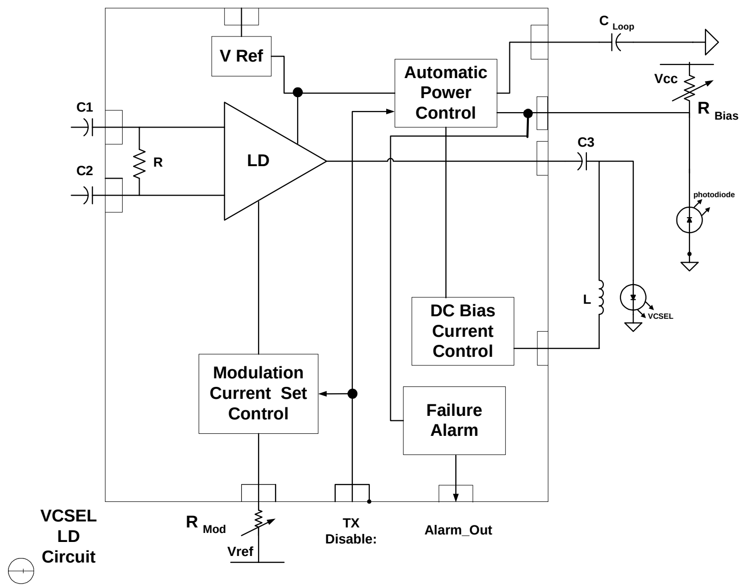


Figure 1. Functional Block Diagram for Single Channel

General Description of IC

Bias and Modulation Current Settings

Bias current supply to the laser diode is generated on-chip and controlled by an Automatic Power Control (APC) loop. The APC loop uses the photodiode current in the feedback loop to adjust the laser bias current. This maintains average optical power over temperature and aging of the laser.

The bias current is fed to the anode of the laser diode through a ferrite inductor (L). This current level is adjusted via an external resistor, R_{BIAS}, which is connected between V_{CC} and the cathode of the photodiode (PD). The potential at the PD cathode is fixed at 0.66*V_{CC} at normal operation. So, the photocurrent is related to R_{BIAS} as,

$$I_{PH} = 0.34 \cdot \frac{V_{CC}}{R_{BIAS}}$$

From the photo diode's responsivity and laser diode's L-I (light vs. current) curves, the appropriate level of laser diode bias current (I_{BIAS}), or average optical power, can be adjusted. The chip design allows a maximum bias current of 25mA to allow for thermal extremes.

An external resistor, R_{MOD}, programs the amplitude of the laser diode's modulation current. The voltage supply of this resistor is generated by an on-chip band-gap circuitry to stabilize the output over temperature. The I_{MOD} range is from 1mA to 18mA for a 50Ω laser diode dynamic resistance. Chart 1 and Chart 2 will aid in selection of R_{MOD} for different laser diode dynamic resistance and working temperature.

The transient LD current is swinging between I_{BIAS}+(I_{MOD}/2) and I_{BIAS}-(I_{MOD}/2). (See Figure 4.)

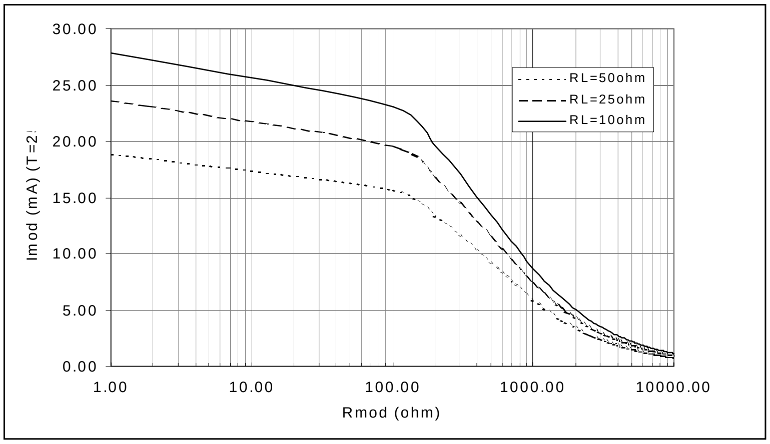


Figure 2. I_{MOD} versus R_{MOD} versus RL

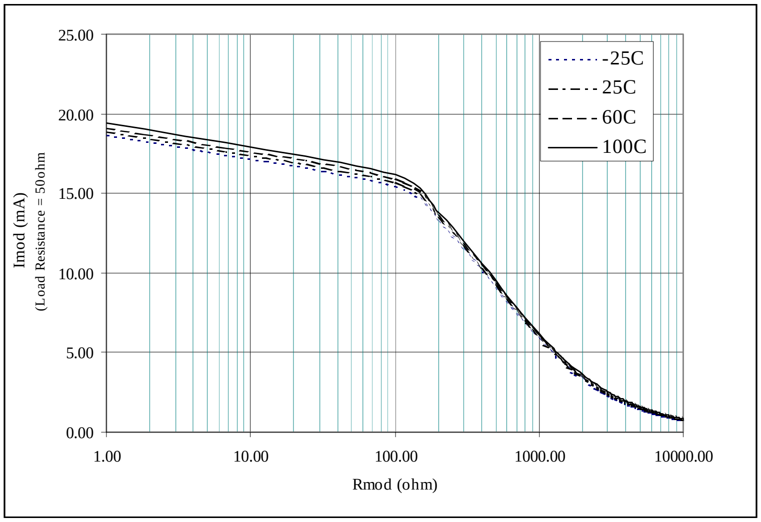


Figure 3. I_{MOD} versus R_{MOD} versus Temperature

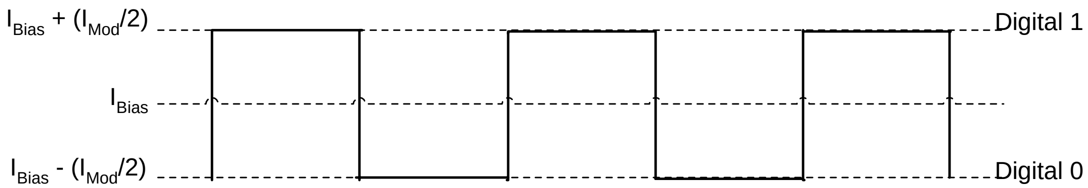


Figure 4. Transient Current of Laser Diode

Automatic Power Control Loop (APC)

The APC loop works to maintain an average optical power over temperature by forcing the laser diode to generate a constant photocurrent through the photodiode. The user selects R_{BIAS} to set the appropriate output optical power. The loop constant capacitor (C_{LOOP}) is required to set the loop bandwidth.

Alarm/Fault Detection

A voltage reading is taken from the cathode side of the photodiode and compared within a window comparator. The Alarm will go high when there is a failure, such as laser/photo diode shorted or open.

Disable Functionality

When the TX_DISABLE pin is high, it turns off both the I_{MOD} and I_{BIAS} so there is no light output from the laser. When TX_DISABLE is set low, the IC will start normal operation.

TX_DISABLE	Laser Current
0V~1.3V	Enabled
1.4V ~V_{CC}	Off

Laser Diode Selection

The chip is configured for a common cathode type of laser with AC coupling of I_{MOD}. For 3.125Gb/s operation, the rise/fall time of the laser diode itself should be less than 100ps. The AC modulation current is in the range of 1mA to 18mA. The bias current ranges from 2mA to 25mA. The photodiode is assumed to output 0.1mA to 1.0mA photocurrent within the laser diodes normal operating range.

The VCSEL LD driver can interface with most packaged common cathode and bare die VCSELs.

General Description of Application Schematic

The differential inputs of the RF3754 are internally balanced 50Ω to ground, 100Ω from pin to pin the single-ended output is 50Ω. Additional circuitry surrounding the RF3754 requires judicious selection regarding component value. Please refer to the Evaluation Schematic (Figure 5) and the Bill of Materials for the evaluation board (Table 1) and the recommended values.

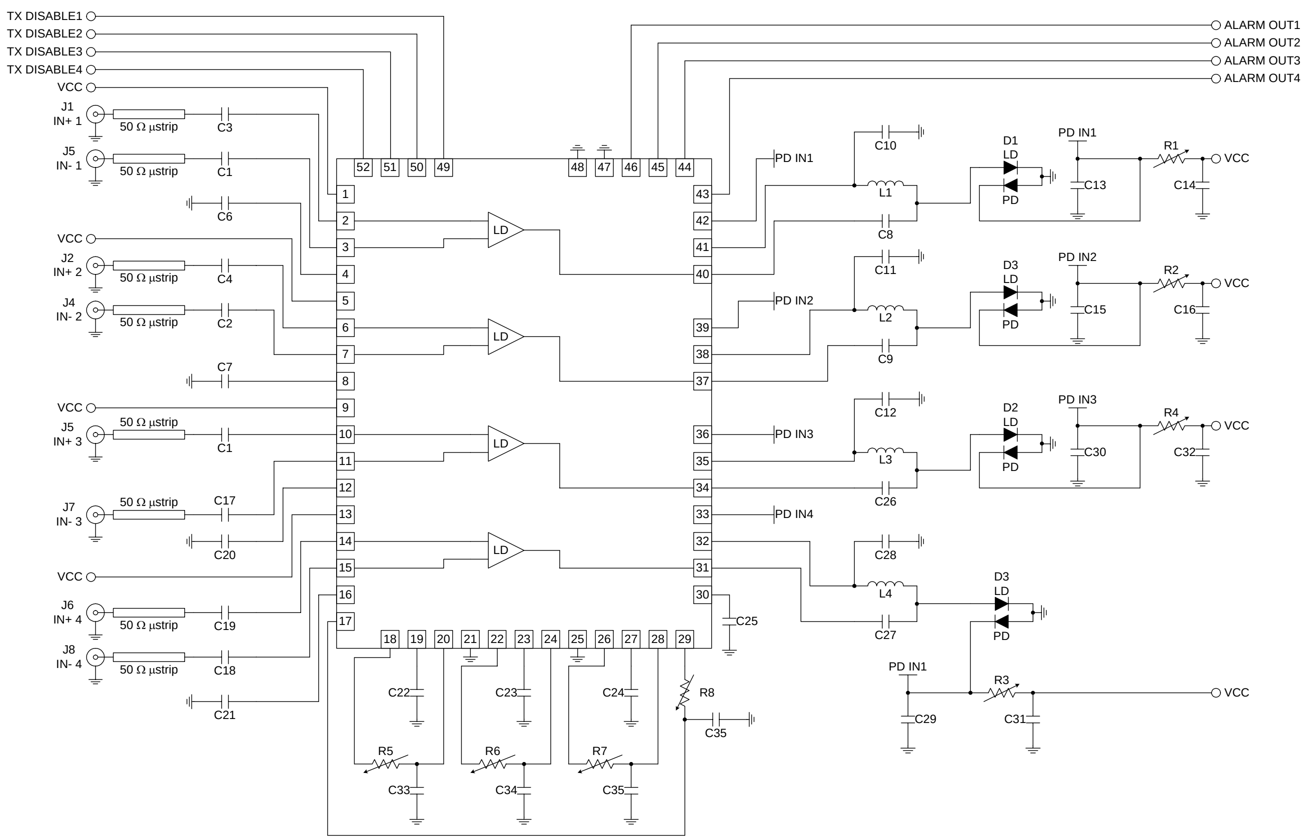


Figure 5. Evaluation Board for TO Packaged Laser

Table 1. Evaluation Board Component List

Designator	Value	Footprint	Description
C1, C2, C3, C4, C5, C17, C18, C19	10nF	0402	DC-blocking capacitor of IN+, IN-.
C22, C23, C24, C25	1μF	0603	Loop constant capacitor, should be as close to IC as possible.
C10, C11, C12, C13, C14, C15, C16, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40	10nF	0402	Bypass capacitor.
C6, C7, C20, C21	10nF	0402	DC-blocking capacitor for AC ground.
C8, C9, C26, C27	10nF	0402	DC-blocking capacitor for laser input, should be as close to IC as possible.
D1, D2, D3, D4	N/A	TO-46	EMCORE 8585-8312 VCSEL. Common cathode laser. TO can is laid on its side and slid over board.
J1, J2, J3, J4, J5, J6, J7, J8	N/A	N/A	SMA connector for data inputs.
L1, L2, L3, L4	Ferrite	0603	RF choke, should be as close to the laser diode pin as possible.
R1, R2, R3, R4	20kΩ	N/A	Adjusting this potentiometer will adjust the bias current to the laser.
R5, R6, R7, R8	10kΩ	N/A	Adjusting this potentiometer will adjust the modulation current to the laser.
U1	RF3754	2.7mm X 1.7mm die	RF Micro Devices' Quad VCSEL driver.

Because there is a DC voltage present on the input of the amplifier, external DC-blocking capacitors are required (C3 and C4). Since this device is optimized for use at 0.1Gbps to 4.0Gbps, a value of 10nF was chosen to provide the best coupling across all data rates.

The output of the VCSEL driver is also AC-coupled, allowing more voltage headroom for the Laser Diode. The value chosen for the DC-blocking capacitor must also be chosen to have the least affect the intended data rate. Choosing a value too low will cause a high frequency cut-off in the circuit response (see Equation 1). If DC-coupling is used and the amount of headroom on the voltage is too low, the output response could have excessive jitter.

$$f_c = \frac{1}{(R \cdot C)} = \frac{1}{(50\Omega \cdot 10nF)} = 2MHz \quad \text{Eq. 1}$$

An RF Choke is used when applying DC bias in order to present constant high impedance to the diode. The frequency response and parasitic capacitance of the choke must be taken into account when making this choice. Because of the wide bandwidth of the laser driver, the choke could cause roll-off at high or low frequencies. Large value inductors (on the order of 870nH) will achieve better low frequency response, but can have large parasitic capacitances that can cause a high frequency roll-off. There is a negative impact on circuit density as large values are typically only available in very large footprints (0805 or larger). Choosing a ferrite bead instead of an inductor can help minimize the high frequency impact since these typically have high impedance at higher frequencies. Ferrites are also available in smaller package sizes minimizing circuit density.

The magnitude of the modulation and bias currents supplied to the VCSEL can be adjusted using external variable resistors. The RF3754 evaluation board is populated with two potentiometers, a 20kΩ pot for bias control and a 10kΩ pot for modulation control. In production, fixed resistor values would program I_{MOD} and I_{BIAS}.

Setting APC Loop Bandwidth

The Loop Capacitor sets the APC loop bandwidth. Increasing this value will increase the time constant of the APC loop, causing the loop lock at a longer time period. Decreasing this value will cause the loop to turn on faster, but could cause the circuit to oscillate. To achieve loop stability and maintain reasonable turn on times, a value in the 1uF range will achieve a time constant of 1mS.

Laser Diode Selection Criteria

When testing the functionality of the RF3754 driver, it is also necessary to examine to performance of the VCSEL diode. Specifications such as rise and fall time should be measured, as this could be a limiting factor in the overall system design. Also, as mentioned earlier, the Forward Voltage of the diode can limit the performance of the laser driver if AC coupling is not utilized.

Previous discussions have assumed the use of a VCSEL and a monitor photodiode contained in a TO Can header (see Figure 3 for application schematic). This allows the photocurrent to be monitored for the internal APC loop. For applications using a bare die VCSEL and no photodiode, the APC loop will not be functional. For this application, the photocurrent can be controlled externally via the LoopC pin (see Figure 6 for application schematic). When using this set-up, the 2kΩ potentiometer needs to be initially set to 0Ω.

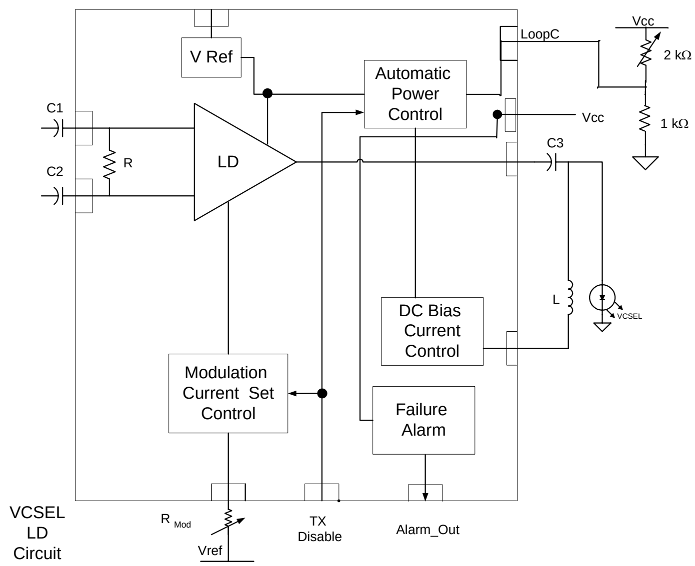


Figure 6. Application Schematic for External Bias Control With a Bare Die VCSEL for a Single Channel

Along with the input V_{CC} and TX_DISABLE pin, an Alarm output pin is also available to monitor any deviations from normal operation. The TX_DISABLE pin is an active high circuit and should be tied to ground. If the driver is disabled or the VCSEL or photodiode cease to function the alarm signal will go HI (V_{CC}).

Disable	System State	Alarm State
0V~1.3V	Normal	Ground
0V~1.3V	Failure of Photo or Laser Diode	V_{CC}
1.4V ~V_{CC}	N/A	V_{CC}

Evaluation Board Layout Considerations

In order to achieve circuit density and have isolation between signal paths and RF paths, a multilayer evaluation board is used (see Table 2). For the evaluation board provided by RFMD, an 18mil microstrip line on 8mil Rogers RO4003 material will achieve the desired 50Ω impedance. For this application, the Rogers RO4003 material was used due to the tightly toleranced dielectric constant. Another common board material used, FR-4, can vary its dielectric constant by as much as ±10 percent depending on the manufacturer. The line width and core material thickness and dielectric constant are critical to maintain controlled line impedances.

Table 2. Evaluation Board Layer Stack Up

Lyr 1 (Signal)	--		0.5oz CU+Plating	0.002"
	Core	Rogers RO4003		0.008"±0.0015"
Lyr 2 (Solid Ground Plane)	--		1.0oz CU	0.0014"
	PrePreg	FR4 or Alternative		0.020"
Lyr 3 (Solid Plane, unused)	--		1.0oz CU	0.0014"
	Core	FR4 or Alternative		0.008"
Lyr 4 (Signal)	--		0.5oz CU+Plating	0.002"

It is also necessary to match the electrical lengths of the balanced inputs and outputs as close as possible. Having unbalanced path lengths can cause the output eye diagram to have slower rise and/or fall times, increased jitter, and ripple on the one or zero.

Also, transitions from the connector to the trace and from the trace to the package pin are critical when considering high frequency evaluation board design. Any changes in the trace width can cause a mismatch, thus affecting performance. In order to avoid this, the pad for the SMA center pin and the package pads have the same width as the microstrip traces. If the package pins, SMA pins, and microstrip traces cannot be the same width, then tapering, or other compensation techniques, should be used at all transitions to minimize mismatch.

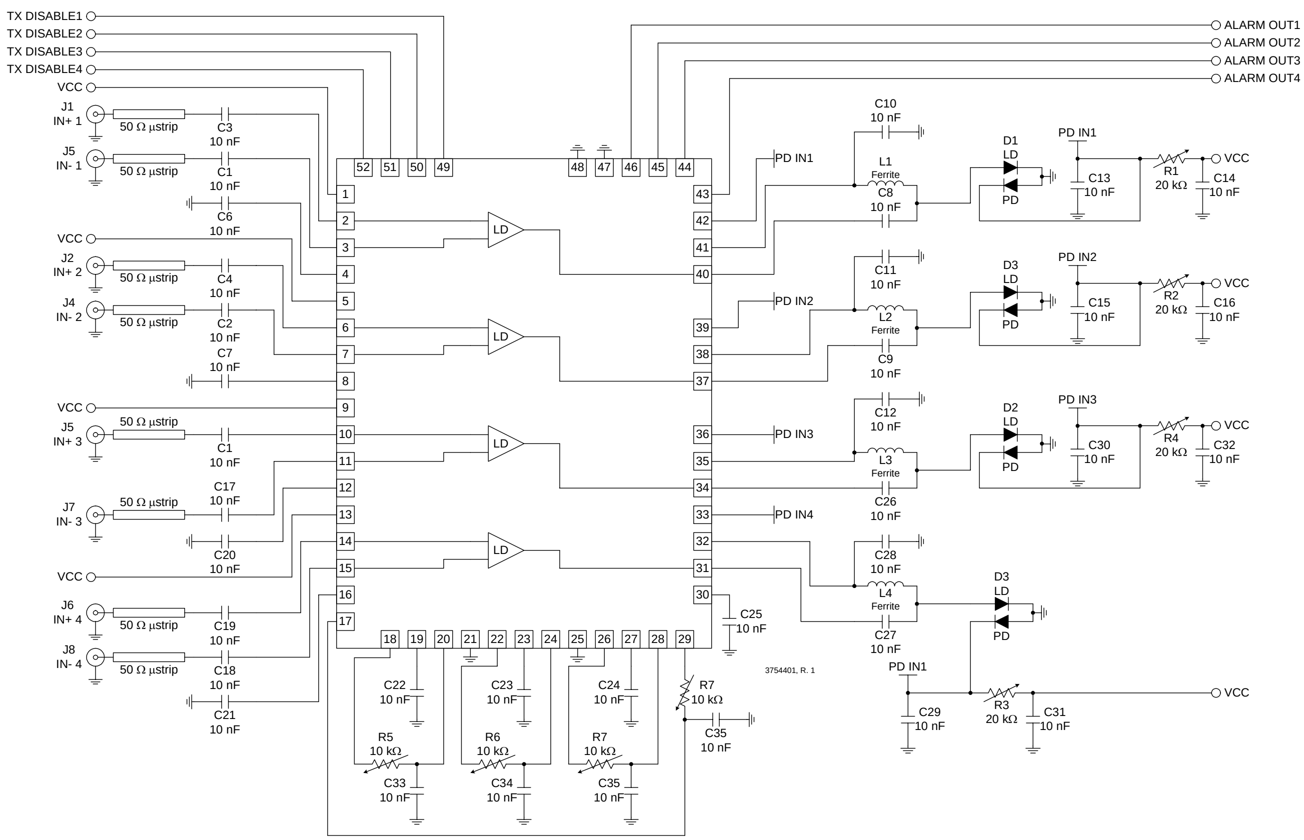
In order to minimize the amount of noise on the V_{CC} circuitry, it is important to place any bypass capacitors as close to the IC as possible.

The most critical microstrip line on the entire board is the output trace on the 'Laser Mod' pin. This path provides the modulated current to the VCSEL diode; therefore any errors introduced in this path will directly affect the quality of the output eye diagram. This trace needs to be as physically short as possible and 50Ω. Keeping an electrically short distance will alleviate the negative effects of a non-perfectly matched transmission line. The DC-blocking capacitor should be placed close to the package, and the bias choke should be close to the laser. It may be necessary to use broadband capacitors on for the DC block if the performance is not satisfactory at all frequencies.

On the RFMD evaluation board, the VCSEL used is in a TO-46 can package. In order to place this close to the RF3754, the TO can is on it’s side and 'slid' over the side of the PCB. The pins of the EMCORE 8585-8312 VCSEL diode are approximately 12.5mm, but have been cut down to 1.5mm.

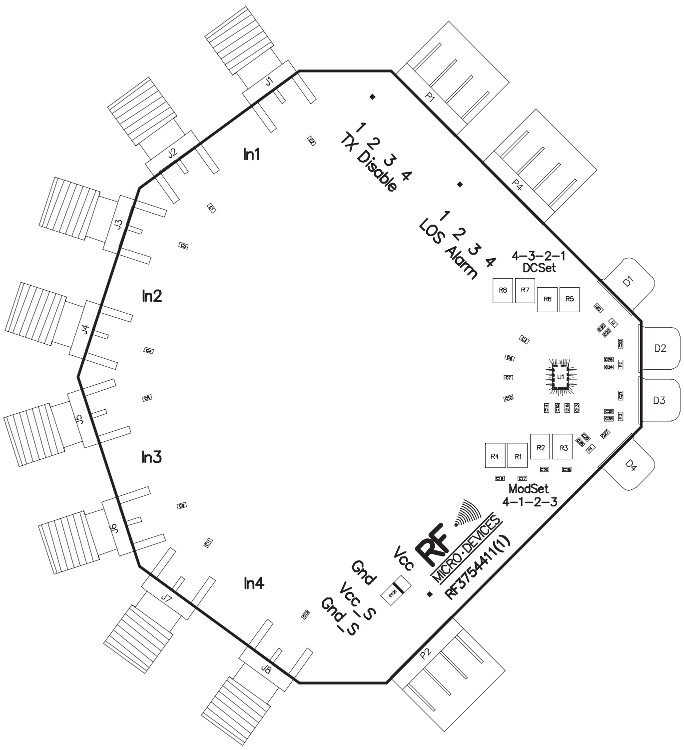
Evaluation Schematic - Optical

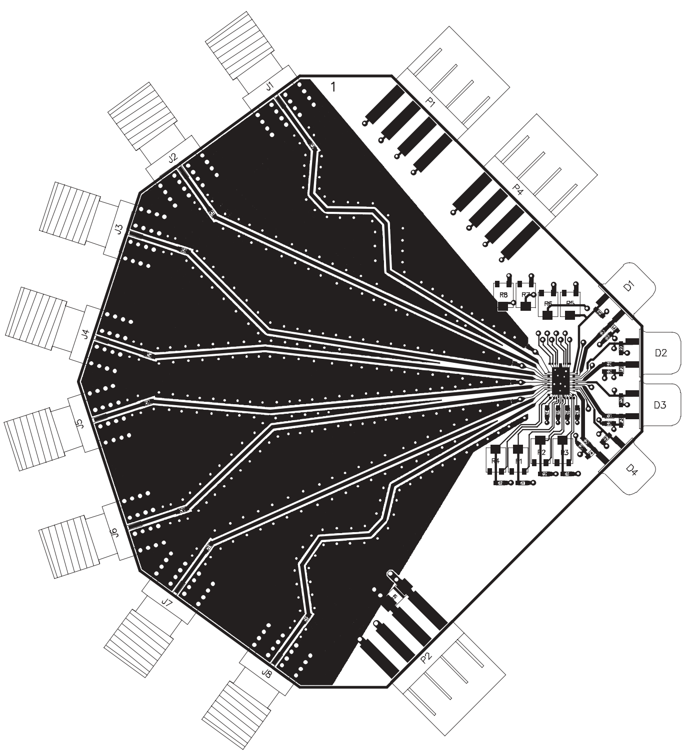
(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout - Optical
Board Size 63.5mm x 68.5mm

Board Thickness 0.042”, Board Material Rogers RO4003 and FR-4, Multi-Layer





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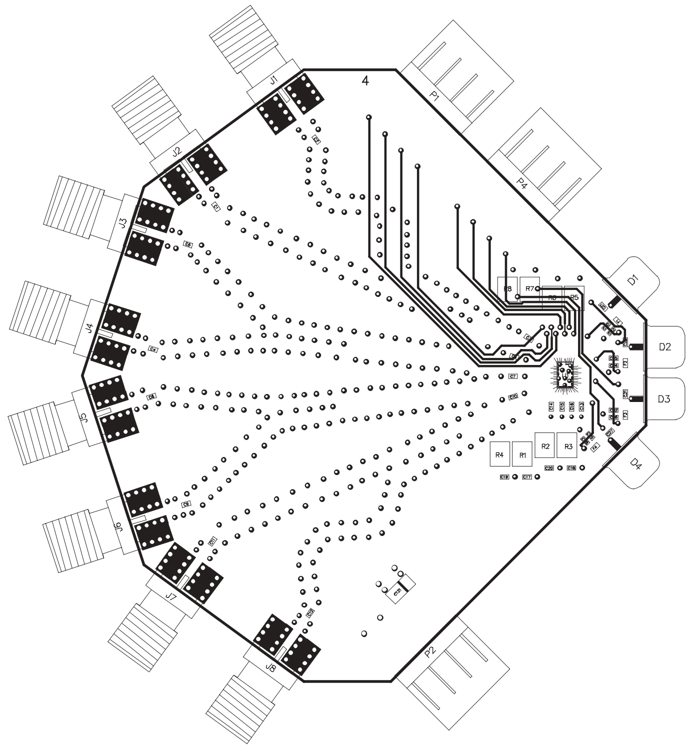
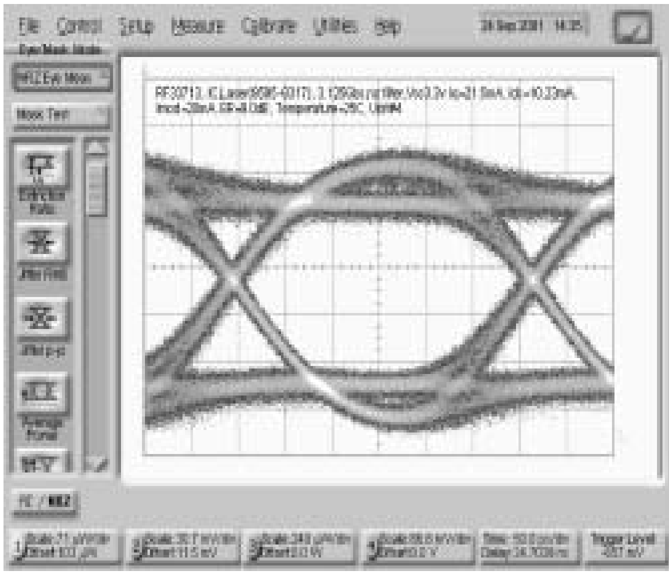
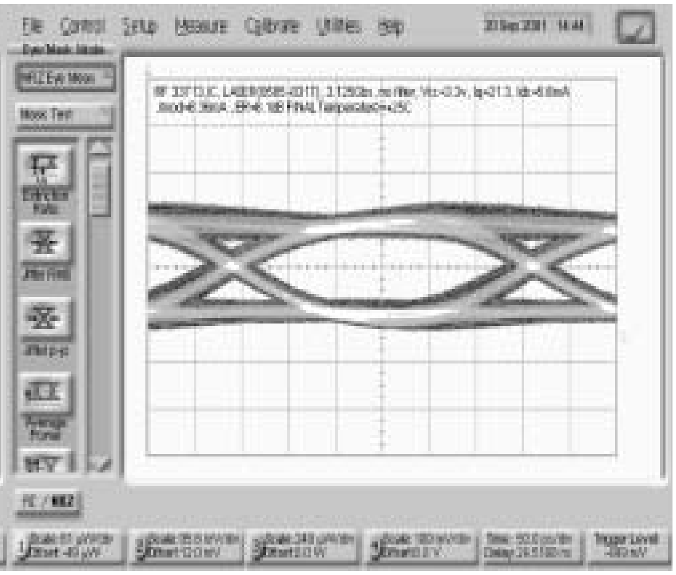
OPTICAL COMMUNICATIONS


J1
J2
J3
J4
J5
J6
J7
J8
P1
P2
P4
D1
D2
D3
D4
R1
R2
R3
R4
R7
R8
4

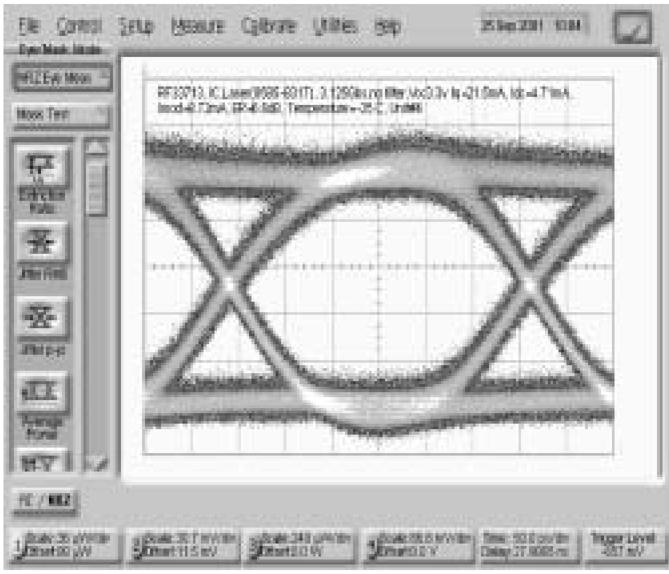
25°C



#2 25°C



-25°C



80°C