

M5M27C201P,FP,J,VP,RV-12,-15

2097152-BIT(262144-WORD BY 8-BIT)
CMOS ONE TIME PROGRAMMABLE ROM

DESCRIPTION

The Mitsubishi M5M27C201P,FP,J,VP,RV are high-speed 2097152-bit one time programmable read only memories. They are suitable for microprocessor programming applications where rapid turn-around is required. The M5M27C201P, FP, J, VP, RV are fabricated by N-channel double polysilicon gate for Memory and CMOS technology for peripheral circuits, and are available in 32 pin plastic packages (DIP, SOP, PLCC) and 40 pin plastic packages (TSOP).

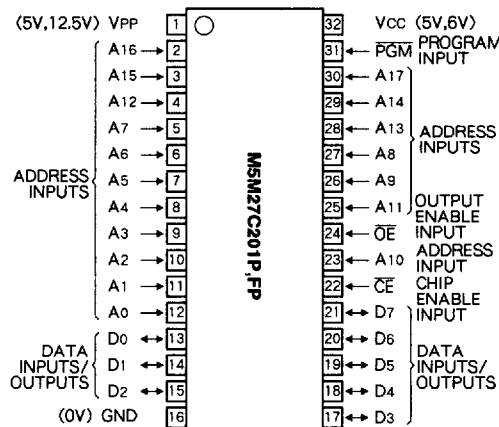
FEATURES

- 262114 word × 8 bit organization
- Package DIP.....M5M27C201P
SOP (525mil)M5M27C201FP
PLCC.....M5M27C201J
TSOPM5M27C201VP
TSOP (Reverse).....M5M27C201RV
- Access time M5M27C201P-12.....120ns (max.)
M5M27C201P-15.....150ns (max.)
- Two line control $\overline{OE}$, $\overline{CE}$
- Low power current (I_{CC}): Active30mA (max.)
(I_{SB2}): Stand-by.....0.1mA (max.)
- Single 5V power supply (read operation)
- Programming voltage.....12.5V
- 3 State output buffer
- Input and output TTL-compatible in read and program mode
- Standard 32 pin DIP, PLCC, Pin-compatible with 2Mbit EPROM
- Byte programming algorithm
- Page programming algorithm

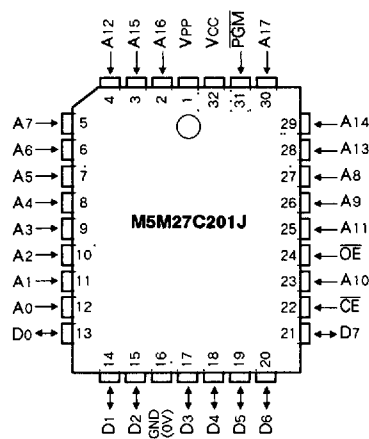
APPLICATION

Microcomputer systems and peripheral equipment

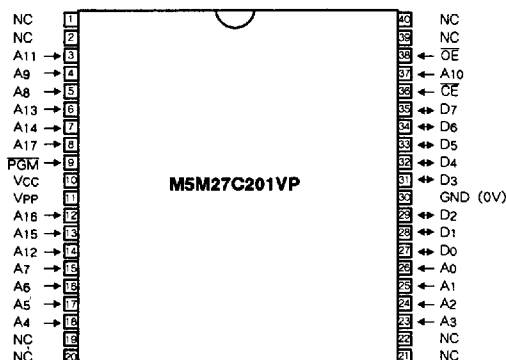
PIN CONFIGURATION (TOP VIEW)



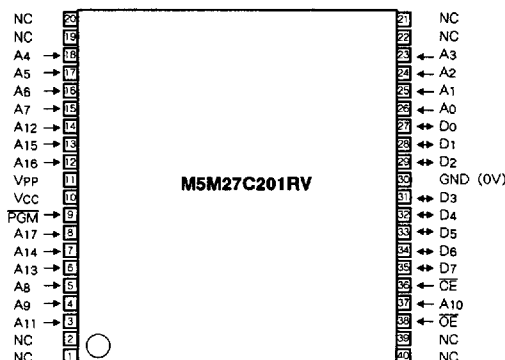
Outline 32P4 (DIP: P)
32P2M-A (SOP: FP)



Outline 32P0 (PLCC: J)



Outline 40P3J-A (TSOP: VP)



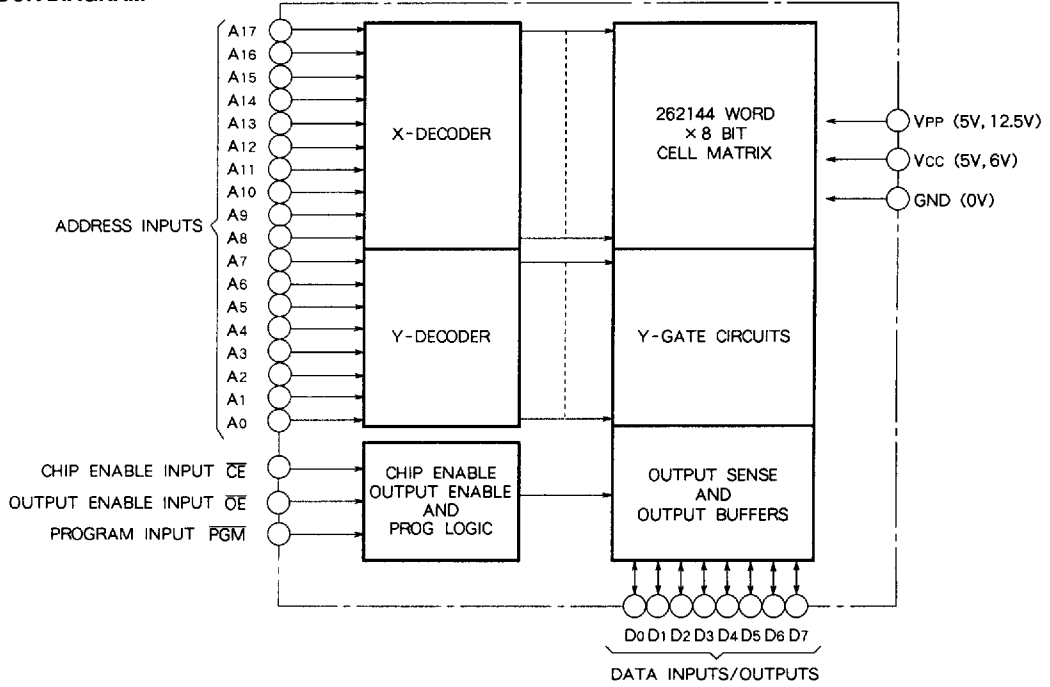
Outline 40P3J-B (TSOP: RV)

NC: NO CONNECTION

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BLOCK DIAGRAM



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FUNCTION

Read

Set the $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low level). Low level input to $\overline{CE}$ and $\overline{OE}$ and address signals to the address inputs ($A_0 \sim A_{17}$) make the data contents of the designated address location available at the data input/output ($D_0 \sim D_7$). When the $\overline{CE}$ or $\overline{OE}$ signal is high, data input/output are in a floating state.

When the $\overline{CE}$ signal is high, the device is in the stand by mode or power-down mode.

Programming

(Byte programming algorithm)

The M5M27C201P, FP, J, VP, RV enter the byte programming mode when 12.5V is supplied to the V_{PP} power supply input, $\overline{CE}$ is at low level and $\overline{OE}$ is at high level. A location is designated by address signals ($A_0 \sim A_{17}$), and the data to be programmed must be applied at 8-bits in parallel to the data inputs ($D_0 \sim D_7$). In this state, byte programming is completed when $\overline{PGM}$ is at low level.

(Page programming algorithm)

Page programming feature of the M5M27C201P, FP, J, VP, RV allows 4 bytes of data to be simultaneously programmed. The destination addresses for a page programming operation must reside on the same page; that is, A_2 through A_{17} must not change. At first, the M5M27C201P, FP, J, VP, RV enter the page data latch mode when $V_{PP} = 12.5V$, $\overline{CE} = "H"$, $\overline{OE} = "L"$ and $\overline{PGM} = "H"$. The four locations in same page are designated by address signals (A_0, A_1 change) and the data to be programmed must be applied to each location at 8-bits in parallel to the data inputs ($D_0 \sim D_7$). In this state, the data (4-bytes) latch is completed. Then the M5M27C201P, FP, J, VP, RV enter the page programming mode when $\overline{OE} = "H"$. In this state, page (4-bytes) programming is completed when $\overline{PGM} = "L"$.

Erase

The M5M27C201P, FP, J, VP, RV cannot be erased, because they are packaged in plastic without transparent lid.

MODE SELECTION

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Data I/O
Read	V_{IL}	V_{IL}	X*	5V	5V	Data out
Output disable	V_{IL}	V_{IH}	X*	5V	5V	Floating
Stand-by (Power down)	V_{IH}	X*	X*	5V	5V	Floating
Byte program	V_{IL}	V_{IH}	V_{IL}	12.5V	6V	Data in
Program verify	V_{IL}	V_{IL}	V_{IH}	12.5V	6V	Data out
Page data latch	V_{IH}	V_{IL}	V_{IH}	12.5V	6V	Data in
Page program	V_{IH}	V_{IH}	V_{IL}	12.5V	6V	Floating
Program inhibit	V_{IL}	V_{IL}	V_{IL}	12.5V	6V	Floating
	V_{IL}	V_{IH}	V_{IH}	12.5V	6V	
	V_{IH}	V_{IL}	V_{IL}	12.5V	6V	
	V_{IH}	V_{IH}	V_{IH}	12.5V	6V	

* : X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Conditions	Ratings	Unit
V_{I1}	All input or output voltage except V_{PP}, A_8	With respect to Ground	- 0.6~7	V
V_{I2}	V_{PP} supply voltage		- 0.6~14.0	V
V_{I3}	A_8 supply voltage		- 0.6~13.5	V
T_{opr}	Operating temperature		- 10~80	°C
T_{stg}	Storage temperature		- 65~150	°C

Note 1 : Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

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READ OPERATION

DC ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{PP} = V_{CC}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input leakage current	$V_{IN} = 0 \sim V_{CC}$			10	μA
I_{LO}	Output leakage current	$V_{OUT} = 0 \sim V_{CC}$			10	μA
I_{PP1}	V_{PP} current read/stand-by	$V_{PP} = V_{CC} = 5.5V$		1	100	μA
I_{SB1}	V_{CC} current stand-by	$\overline{CE} = V_{IH}$			1	mA
I_{SB2}		$\overline{CE} = V_{CC}$		1	100	μA
I_{CC1}	V_{CC} current active	$\overline{CE} = \overline{OE} = V_{IL}$, DC, $I_{OUT} = 0\text{mA}$			30	mA
I_{CC2}		$\overline{CE} = V_{IL}$, $f = 8.3\text{MHz}$, $I_{OUT} = 0\text{mA}$			30	mA
V_{IL}	Input low voltage		-0.1		0.8	V
V_{IH}	Input high voltage		2.2		$V_{CC} + 1$	V
V_{OL}	Output low voltage	$I_{OL} = 2.1\text{mA}$			0.45	V
V_{OH}	Output high voltage	$I_{OH} = -400\mu\text{A}$	2.4			V

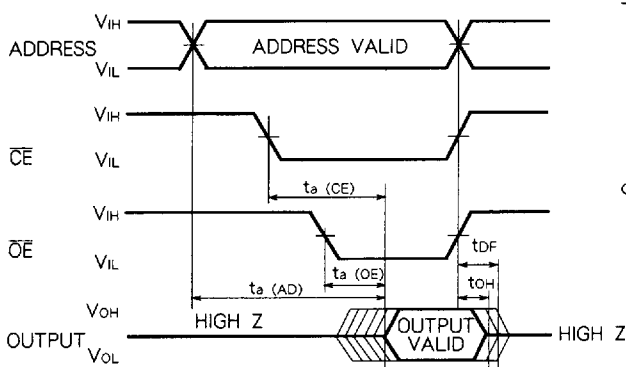
Note 2: Typical values are at $T_a = 25^\circ\text{C}$ and normal supply voltages

AC ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{PP} = V_{CC}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits				Unit
			M5M27C201P-12		M5M27C201P-15		
			Min	Max	Min	Max	
t _a (AD)	Address to output delay	$\overline{CE} = \overline{OE} = V_{IL}$		120		150	ns
t _a (CE)	$\overline{CE}$ to output delay	$\overline{OE} = V_{IL}$		120		150	ns
t _a (OE)	Output enable to output delay	$\overline{CE} = V_{IL}$		60		60	ns
t _{DF}	Output enable high to output float	$\overline{CE} = V_{IL}$	0	50	0	50	ns
t _{OH}	Output hold from $\overline{CE}$, $\overline{OE}$ or address		0		0		ns

Note 3: V_{CC} must be applied simultaneously V_{PP} and removed simultaneously V_{PP}

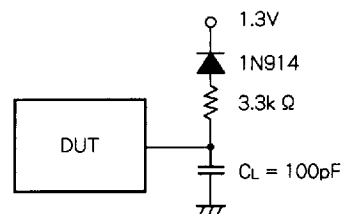
AC WAVEFORMS



Test conditions for A.C. characteristics
Input voltage : $V_{IL} = 0.45V$, $V_{IH} = 2.4V$
Input rise and fall times : $\leq 10\text{ns}$
Reference voltage at timing measurement : 1.5V

Output load : 1TTL gate + CL (100pF)

or



CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input capacitance (Address, $\overline{CE}$, $\overline{OE}$, PGM)	$T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$, $V_i = V_o = 0V$			15	pF
C_{OUT}	Output capacitance				15	pF

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PROGRAM OPERATION**BYTE PROGRAMMING ALGORITHM**

First set $V_{CC} = 6V$, $V_{PP} = 12.5V$ and then set an address to first address to be programmed. After applying 0.2ms program pulse (PGM) to the address, verify is performed. If the output data of that address is not verified correctly, apply one more 0.2ms program pulse. The programmer continues 0.2ms pulse-then-verify routines until the device verify correctly or twenty five of these pulse-then-verify routines have been completed. The programmer also maintains its total

number of 0.2ms pulse applied to that address in register X. And then applied a program pulse X times of 0.2ms width as an overprogram pulse. When the programming procedure above is finished, step to the next address and repeat this procedure till last address to be programmed. When the entire addresses have been programmed completely, all addresses should be verified with $V_{CC} = V_{PP} = 5V$.

DC ELECTRICAL CHARACTERISTICS ($T_a = 25 \pm 5^\circ C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input leakage current	$V_{IN} = 0 \sim V_{CC}$			10	μA
V_{OL}	Output low voltage (verify)	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	Output high voltage (verify)	$I_{OH} = -400 \mu A$	2.4			V
V_{IL}	Input low voltage		-0.1		0.8	V
V_{IH}	Input high voltage		2.2		V_{CC}	V
I_{CC}	V_{CC} supply current				30	mA
I_{PP}	V_{PP} supply current	PGM = V_{IL}			30	mA

AC ELECTRICAL CHARACTERISTICS ($T_a = 25 \pm 5^\circ C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$, unless otherwise noted)

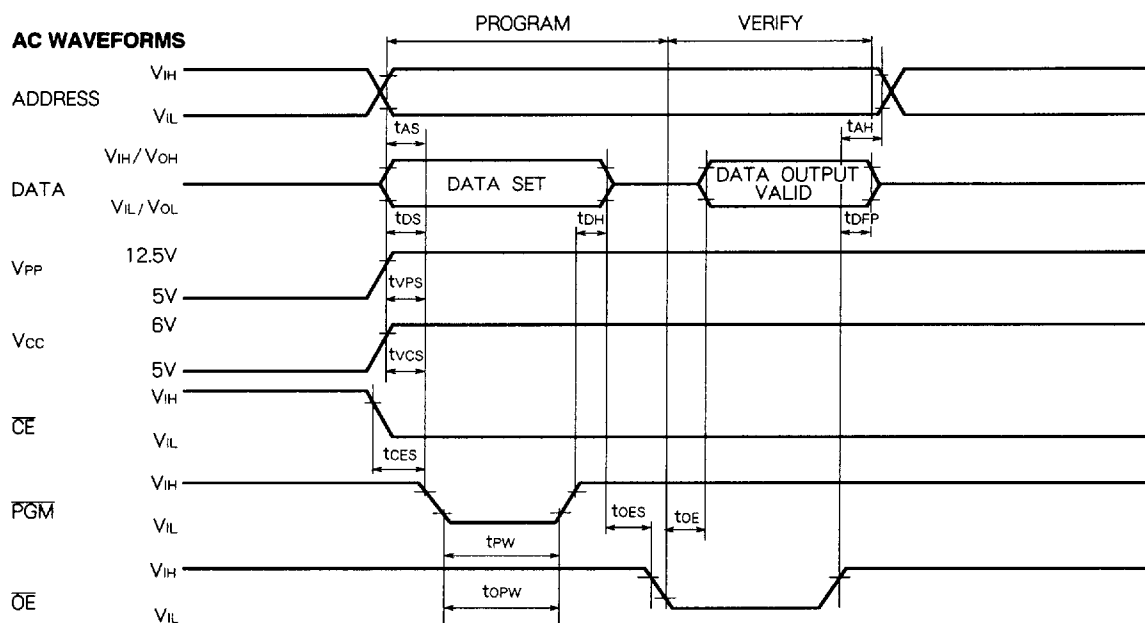
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$ setup time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DFP}	Chip enable to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			μs
t_{VPS}	V_{PP} setup time		2			μs
t_{PW}	PGM initial program pulse width		0.19	0.2	0.21	ms
t_{OPW}	PGM over program pulse width		0.19		5.25	ms
t_{CES}	$\overline{CE}$ setup time		2			μs
t_{OE}	Data valid from $\overline{OE}$				150	ns

Note 4: V_{CC} must be applied simultaneously V_{PP} and removed simultaneously V_{PP} .

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AC WAVEFORMS



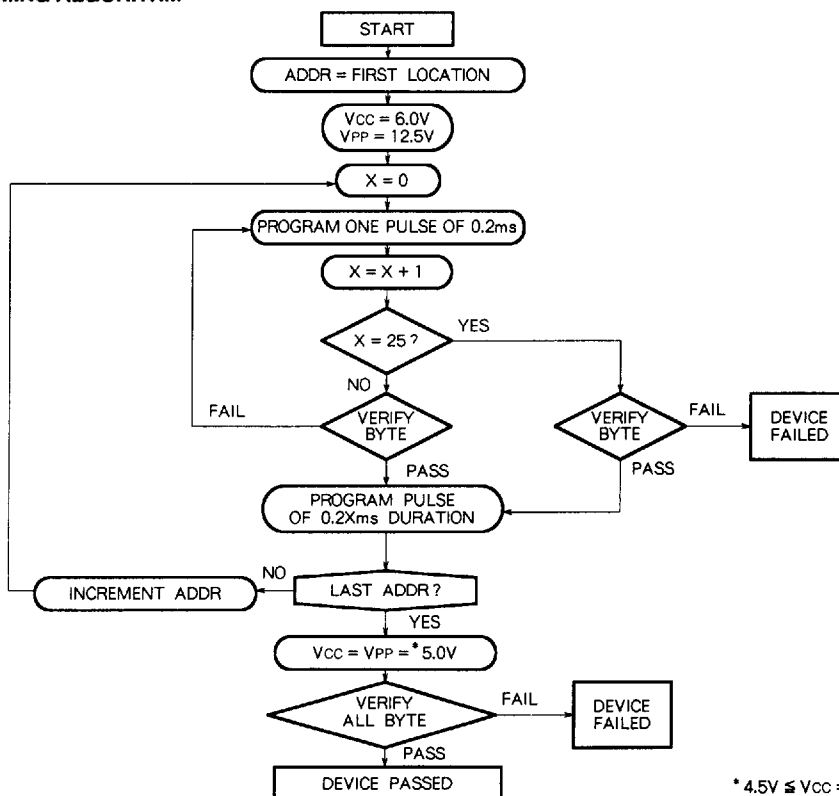
Test conditions for A.C. characteristics

Input voltage : $V_{IL} = 0.45V$, $V_{IH} = 2.4V$

Input rise and fall time : (10%~90%) : $\leq 20\text{ns}$

Reference voltage at timing measurement: Input, Output
 "L" = 0.8V, "H" = 2V

BYTE PROGRAMMING ALGORITHM FLOW CHART



* $4.5V \leq V_{CC} = V_{PP} \leq 5.5V$

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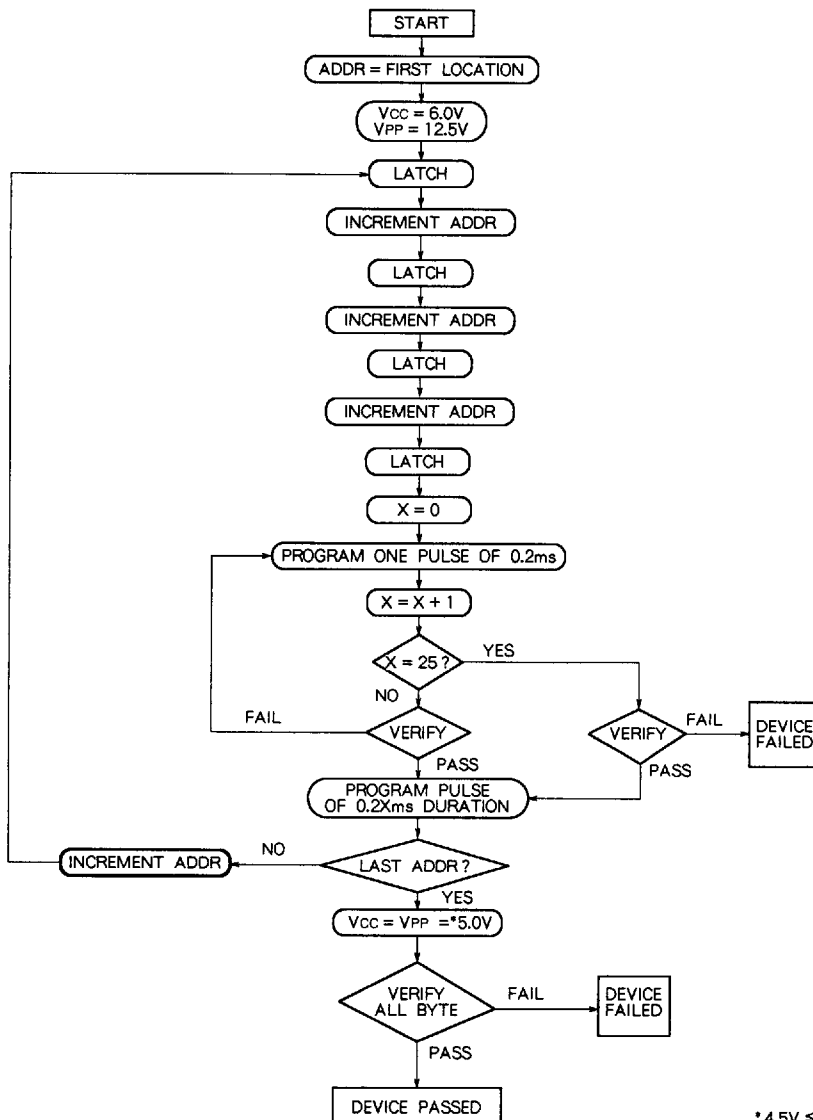
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PAGE PROGRAMMING ALGORITHM

First set $V_{CC} = 6V$, $V_{PP} = 12.5V$ and then set an address to first page address to be programmed. After data of 4 bytes are latched, these latch data are programmed simultaneously by applying 0.2ms program pulse. Then a verify is performed. If each output data is not verified correctly, apply one more 0.2ms program pulse. The programmer continues 0.2ms pulse - then - verify routines until each output data is verified correctly or twenty five of these pulse-then-verify routines have been completed. The programmer also maintains its total

number of 0.2ms pulse applied to that page addresses in register X. And then applied a program pulse X times of 0.2 ms width as an overprogram pulse. When the programming procedure above is finished, step to the next page address and repeat this procedure till last page address to be programmed. When the entire page addresses have been programmed completely, all addresses should be verified with $V_{CC} = V_{PP} = 5V$.

**PAGE PROGRAMMING ALGORITHM
FLOW CHART**



* $4.5V \leq V_{CC} = V_{PP} \leq 5.5V$

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DC ELECTRICAL CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$, unless otherwise noted)

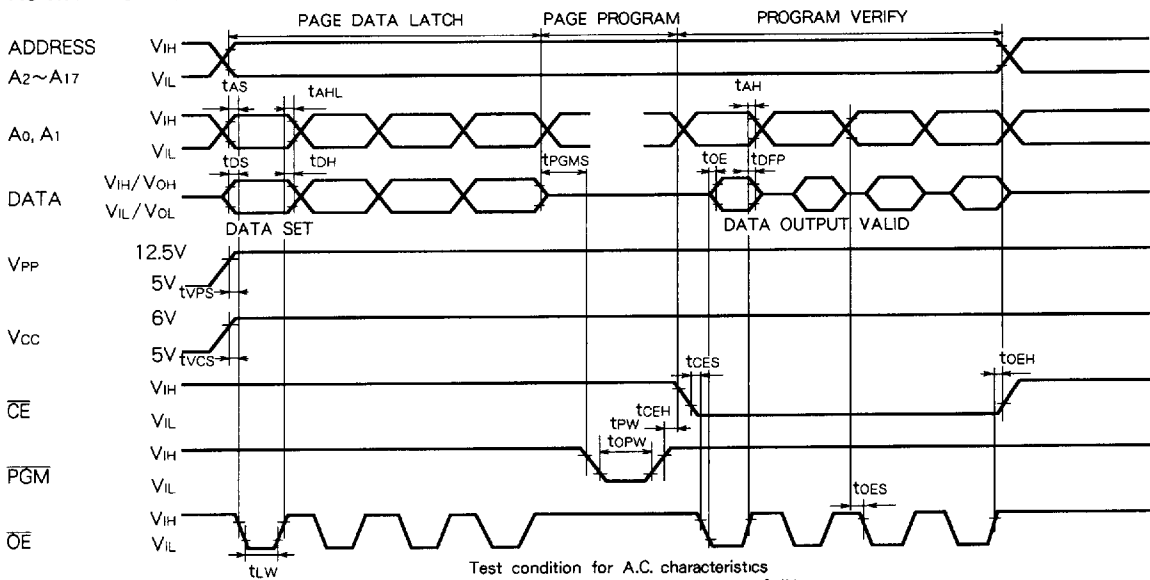
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input leakage current	$V_{IN} = 0V \sim V_{CC}$			10	μA
V_{OL}	Output low voltage (verify)	$I_{OL} = 2.1\text{mA}$			0.45	V
V_{OH}	Output high voltage (verify)	$I_{OH} = -400\mu\text{A}$	2.4			V
V_{IL}	Input low voltage		-0.1		0.8	V
V_{IH}	Input high voltage		2.2		V_{CC}	V
I_{CC}	V_{CC} supply current				30	mA
I_{PP}	V_{PP} supply current	$PGM = V_{IL}$			100	mA

AC ELECTRICAL CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$, unless otherwise noted)

symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$ setup time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{AHL}			2			μs
t_{DH}	Data hold time		2			μs
t_{DFP}	$\overline{OE}$ to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			μs
t_{VPS}	V_{PP} setup time		2			μs
t_{PW}	PGM initial program pulse width		0.19	0.2	0.21	ms
t_{OPW}	PGM over program pulse width		0.19		5.25	ms
t_{CES}	$\overline{CE}$ setup time		2			μs
t_{OE}	Data valid from $\overline{OE}$				150	ns
t_{LW}	Data latch time		1			μs
t_{PGMS}	PGM setup time		2			μs
t_{CEH}	$\overline{CE}$ hold time		2			μs
t_{OEH}	$\overline{OE}$ hold time		2			μs

Note 5: V_{CC} must be applied simultaneously V_{PP} and removed simultaneously V_{PP} .

AC WAVEFORMS



Test condition for A.C. characteristics
Input voltage : $V_{IL} = 0.45V$, $V_{IH} = 2.4V$
Input rise and fall time : (10%~90%) : $\leq 20\text{ns}$
Reference voltage at timing measurement : Input, Output "L" = 0.8V, "H" = 2V

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DEVICE IDENTIFIER MODE

The Device Identifier Mode allows the reading of a binary code from the OTP ROM that identifies the manufacturer and device type.

The PROM Programmer reads the manufacturer code and the device code and automatically selects the corresponding programming algorithm.

M5M27C201P, FP, J, VP, RV DEVICE IDENTIFIER CODE

Code \ Pin	A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Hex Data
Manufacturer code	V _{IL}	0	0	0	1	1	1	0	0	1C
Device code	V _{IH}	1	0	0	0	1	0	1	0	8A

Note 6: A₉ = 12.0 ± 0.5V

A₁~A₈, A₁₀~A₁₇, $\overline{CE}$, $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}
V_{CC} = V_{PP} = 5V ± 10%.

RECOMMENDED SCREENING CONDITION

The following screening test is recommended before using.

