# SMC82C51AC

## CMOS PROGRAMMABLE COMMUNICATION INTERFACE

- **Synchronous/Asynchronous Receiver/Transmitter**
- **Baud Rate -- DC to 64Kbps**
- **Low Power**

### ■DESCRIPTION

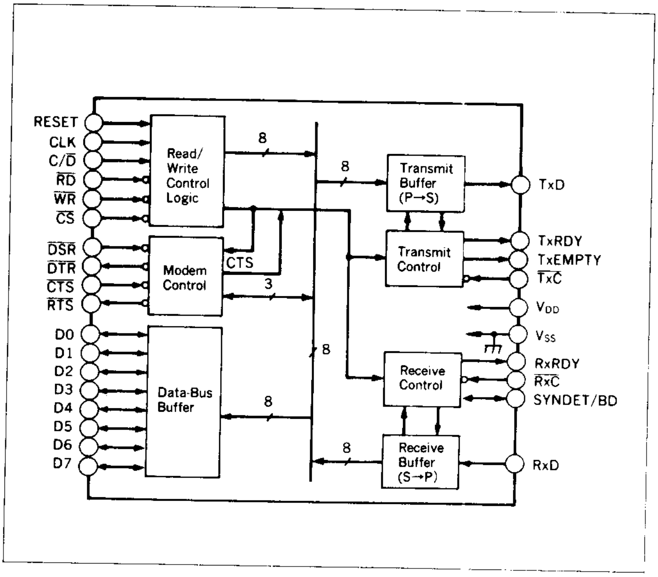
The SMC82C51AC is the enhanced CMOS version of the industry standard Universal Synchronous/Asynchronous Receiver/Transmitter (USART) designed for data communications.

### ■FEATURES

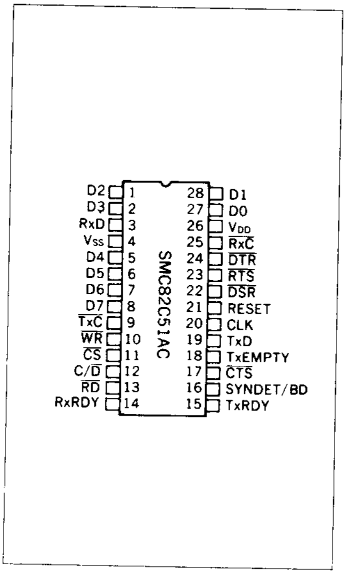
- Synchronous 5 to 8-bit character operation
  - Internal or external character synchronization
  - Automatic SYNC character insertion
  - Synchronous baud rate : DC to 64K baud
- Asynchronous 5 to 8-bit character operation
  - Clock rate of 1, 16, or 64 times baud rate
  - 1, 1.5 or 2 stop bits
  - False start bit detection
  - Automatic break detection and handling
- Baud rate : DC to 64K Baud
- Full-duplex, double-buffered transmitter and receiver
- Error detection : parity, overrun and framing
- Single 5V (±10%) power supply
- Package··························28-pin DIP
  28-pin SOP*

*Under development

### ■BLOCK DIAGRAM




### ■PIN CONFIGURATION



## ■ABSOLUTE MAXIMUM RATINGS

($V_{SS}$=0V, Ta=25°C)

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | With respect to $V_{SS}$ | −0.3 to 7 | V |
| Input voltage | $V_I$ | With respect to $V_{SS}$ | −0.3 to $V_{DD}$+0.3 | V |
| Output voltage | $V_O$ | With respect to $V_{SS}$ | −0.3 to $V_{DD}$+0.3 | V |
| Operating temperature | $T_{opr}$ | — | −20 to 75 | °C |
| Storage temperature | $T_{stg}$ | — | −65 to 150 | °C |
| Soldering temperature and time | $T_{sol}$ | — | 260°C, 10s (at lead) | — |

## ■RECOMMENDED OPERATING CONDITIONS

(Ta=−20 to 75°C, unless otherwise noted.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | — | 4.5 | 5 | 5.5 | V |
| Power-supply voltage | $V_{SS}$ | — | — | 0 | — | V |

## ■ELECTRICAL CHARACTERISTICS

### ●DC Electrical Characteristics

(Ta=−20to75°C, $V_{DD}$=5V±10%, $V_{SS}$=0V, unless otherwise noted.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | — | 2 | — | $V_{DD}$+0.3 | V |
| Low-level input voltage | $V_{IL}$ | — | −0.3 | — | 0.8 | V |
| High-level output voltage | $V_{OH}$ | $I_{OH}$=−400μA | 2.4 | — | — | V |
| Low-level output voltage | $V_{OL}$ | $I_{OL}$=2.2mA | — | — | 0.45 | V |
| Supply current from $V_{DD}$ | $I_{DD}$ | — | — | — | 5 | mA |
| High-level input current | $I_{IH}$ | $V_I$=$V_{DD}$ | −10 | — | 10 | μA |
| Low-level input current | $I_{IL}$ | $V_I$=0V | −10 | — | 10 | μA |
| Off-state input current | $I_{OZ}$ | $V_{SS}$=0V, $V_I$=0V to $V_{DD}$ | −10 | — | 10 | μA |
| Input capacitance | $C_I$ | $V_{DD}$=$V_{SS}$, f=1MHz, 25m$V_{rms}$, Ta=25°C | — | — | 10 | pF |
| Input/output capacitance | $C_{I/O}$ | $V_{DD}$=$V_{SS}$, f=1MHz, 25m$V_{rms}$, Ta=25°C | — | — | 20 | pF |

### ●AC Electrical Characteristics

#### ○ Timing Requirements

(Ta=−20 to 75°C, $V_{DD}$=5V±10%, $V_{SS}$=0V, unless otherwise noted.)

| Parameter | | Symbol | Alternative Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Clock cycle time *1, 2 | | $t_{C(\phi)}$ | $t_{CY}$ | | 320 | — | 1350 | ns |
| Clock high pulse width | | $t_{W(\phi)}$ | $t_{\phi}$ | | 120 | — | $t_{C(\phi)}-90$ | ns |
| Clock low pulse width | | $t_{W(\bar{\phi})}$ | $t_{\bar{\phi}}$ | | 90 | — | — | ns |
| Clock rise time | | $t_r$ | $t_R$ | | — | — | 20 | ns |
| Clock fall time | | $t_f$ | $t_F$ | | — | — | 20 | ns |
| Transmitter input clock frequency | 1X baud rate | $f_{TX}$ | $f_{TX}$ | | DC | — | 64 | kHz |
| | 16X baud rate | | $f_{TX}$ | | DC | — | 310 | kHz |
| | 64X baud rate | | $f_{TX}$ | | DC | — | 615 | kHz |
| Transmitter input clock low pulse width | 1X baud rate | $t_{W(TPWL)}$ | $t_{TPW}$ | | 12 | — | — | $t_{C(\phi)}$ |
| | 16X,64X baud rate | | $t_{TPW}$ | | 1 | — | — | $t_{C(\phi)}$ |
| Transmitter input clock high pulse width | 1X baud rate | $t_{W(TPWH)}$ | $t_{TPD}$ | | 15 | — | — | $t_{C(\phi)}$ |
| | 16X,64X baud rate | | $t_{TPD}$ | | 3 | — | — | $t_{C(\phi)}$ |
| Receiver input clock frequency | 1X baud rate | $f_{RX}$ | $f_{RX}$ | | DC | — | 64 | kHz |
| | 16X baud rate | | $f_{RX}$ | | DC | — | 310 | kHz |
| | 64X baud rate | | $f_{RX}$ | | DC | — | 615 | kHz |
| Receiver input clock low pulse width | 1X baud rate | $t_{W(RPWL)}$ | $t_{RPW}$ | | 12 | — | — | $t_{C(\phi)}$ |
| | 16X,64X baud rate | | $t_{RPW}$ | | 1 | — | — | $t_{C(\phi)}$ |
| Receiver input clock high pulse width | 1X baud rate | $t_{W(RPWH)}$ | $t_{RPD}$ | | 15 | — | — | $t_{C(\phi)}$ |
| | 16X,64X baud rate | | $t_{RPD}$ | | 3 | — | — | $t_{C(\phi)}$ |
| Address setup time before read ($\overline{CS}$, C/$\overline{D}$) *3 | | $t_{SU(A-R)}$ | $t_{AR}$ | | 0 | — | — | ns |
| Address hold time after read ($\overline{CS}$, C/$\overline{D}$) *3 | | $t_{h(R-A)}$ | $t_{RA}$ | | 0 | — | — | ns |

| Parameter | Symbol | Alternative Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Read pulse width | $t_{W(R)}$ | $t_{RR}$ | | 200 | — | — | ns |
| Address setup time before write | $t_{SU(A-W)}$ | $t_{AW}$ | | 0 | — | — | ns |
| Address hold time after write | $t_{h(W-A)}$ | $t_{WA}$ | | 0 | — | — | ns |
| Write pulse width | $t_{W(W)}$ | $t_{WW}$ | | 200 | — | — | ns |
| Data setup time before write | $t_{SU(DQ-W)}$ | $t_{DW}$ | | 100 | — | — | ns |
| Data hold time after write | $t_{h(W-DQ)}$ | $t_{WO}$ | | 0 | — | — | ns |
| E•SYNDET setup time before $\overline{RxC}$ | $t_{SU(ESD-RxC)}$ | $t_{ES}$ | | 18 | — | — | $t_{C(\phi)}$ |
| Control setup time before read | $t_{SU(C-R)}$ | $t_{CR}$ | | 20 | — | — | $t_{C(\phi)}$ |
| Write recovery time between writes *4 | $t_{RV}$ | $t_{RV}$ | | 6 | — | — | $t_{C(\phi)}$ |
| RxD setup time before internal sampling pulse | $t_{SU(RxD-IS)}$ | $t_{SRx}$ | | 2 | — | — | $\mu s$ |
| RxD hold time after internal sampling pulse | $t_{h(IS-RxD)}$ | $t_{HRx}$ | | 2 | — | — | $\mu s$ |

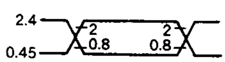
*1 The $\overline{TxC}$ and $\overline{RxC}$ frequencies have the following limitations with respect to CLK. For 1X baud rate $f_{TX}$, $f_{RX} \leqq 1/(30t_{C(\phi)})$. For 16X, 64X baud rate $f_{TX}$, $f_{RX} \leqq 1/(4.5t_{C(\phi)})$
*2 Reset pulse width $= 6t_{C(\phi)}$ minimum. System clock must be running during reset.
*3 $\overline{CS}$,C/$\overline{D}$ are considered as address.
*4 This recovery time is for mode initialization only. Write data is allowed only when TxRDY=1. Recovery time between writes for asynchronous mode is $8t_{C(\phi)}$, and that for synchronous mode is $16t_{C(\phi)}$.

## ○ Switching Characteristics

(Ta = −20 to 75°C, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.)

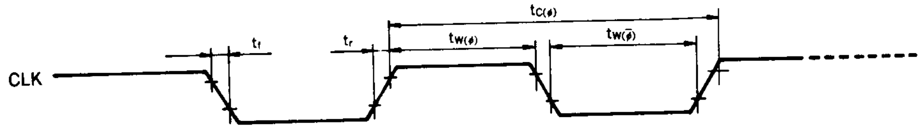
| Parameter | Symbol | Alternative symbol | Conditions *7 | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Output data enable time after read *5 | $t_{PZV(R-DQ)}$ | $t_{RD}$ | $C_L = 150pF$ | — | — | 170 | ns |
| Output data disable time after read | $t_{PVZ(R-DQ)}$ | $t_{DF}$ | | 10 | — | 100 | ns |
| TxD enable time after falling edge of $\overline{TxC}$ | $t_{PZV(TxC-TxD)}$ | $t_{CTx}$ | | — | — | 1 | $\mu s$ |
| Propagation time from center of last bit to TxRDY clear *6 | $t_{PLH(CLB-TxR)}$ | $t_{TxRDY}$ | | — | — | 8 | $t_{C(\phi)}$ |
| Propagation time from write data to TxRDY *6 | $t_{PHL(W-TxR)}$ | $t_{TxRDY CLEAR}$ | | — | — | 400 | ns |
| Propagation time from center of last bit to RxRDY *6 | $t_{PLH(CLB-RxR)}$ | $t_{RxRDY}$ | | — | — | 26 | $t_{C(\phi)}$ |
| Propagation time from read data to RxRDY clear *6 | $t_{PHL(R-RxR)}$ | $t_{RxRDY CLEAR}$ | | — | — | 400 | ns |
| Propagation time from rising edge of $\overline{RxC}$ to internal SYNDET *6 | $t_{PLH(RxC-SYD)}$ | $t_{IS}$ | | — | — | 26 | $t_{C(\phi)}$ |
| Propagation time from center of last bit to TxEMPTY *6 | $t_{PLH(CLB-TxE)}$ | $t_{TxEMPTY}$ | | 20 | — | — | $t_{C(\phi)}$ |
| Propagation time from rising edge of $\overline{WR}$ to control *6 | $t_{PHL(W-C)}$ | $t_{WC}$ | | 8 | — | — | $t_{C(\phi)}$ |

*5 Assumes that address is vaild before falling edge of $\overline{RD}$.
*6 Status-up data can have a maximum delay of 28 clock periods from the event affecting the status.
*7 Input pulse level 0.45 to 2.4V
Input pulse rise time 20ns
Input pulse fall time 20ns
Reference level Input $V_{IH} = 2V$, $V_{IL} = 0.8V$
Output $V_{OH} = 2V$, $V_{OL} = 0.8V$

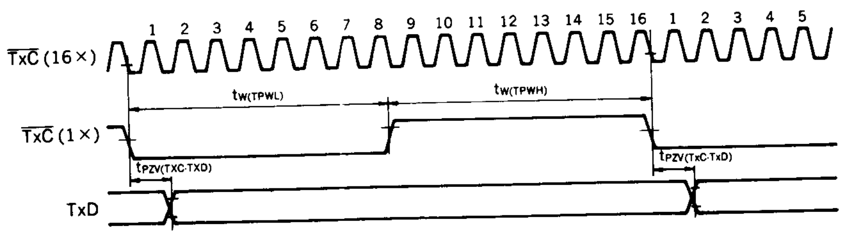


## ●Timing Chart

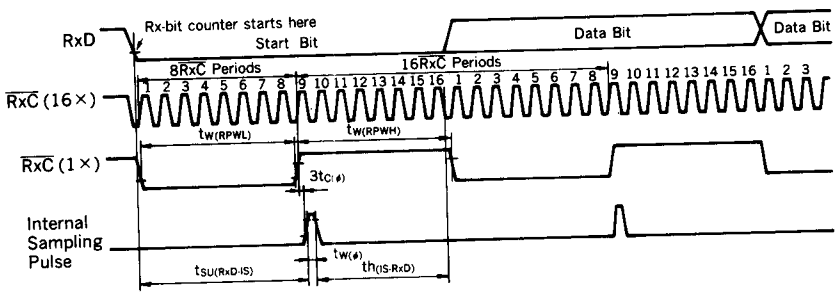
○System clock (CLK)



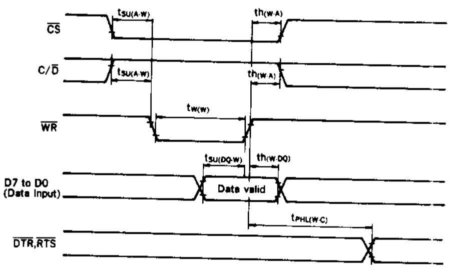

○Transmitter clock & data



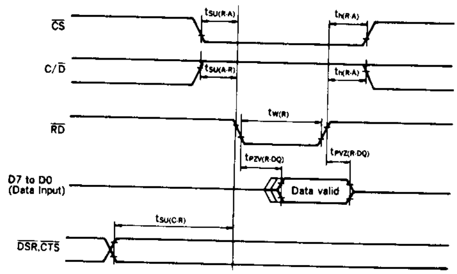

○Receiver clock & data



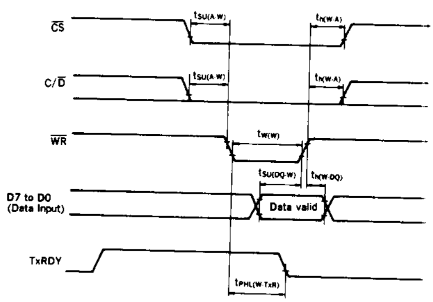
○ Write control cycle (CPU → USART)



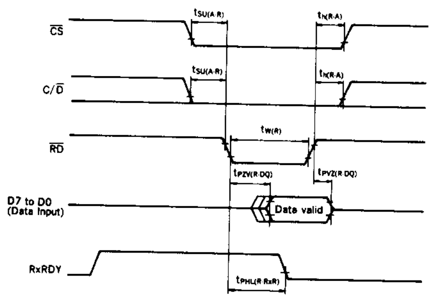

○ Read control cycle (USART → CPU)



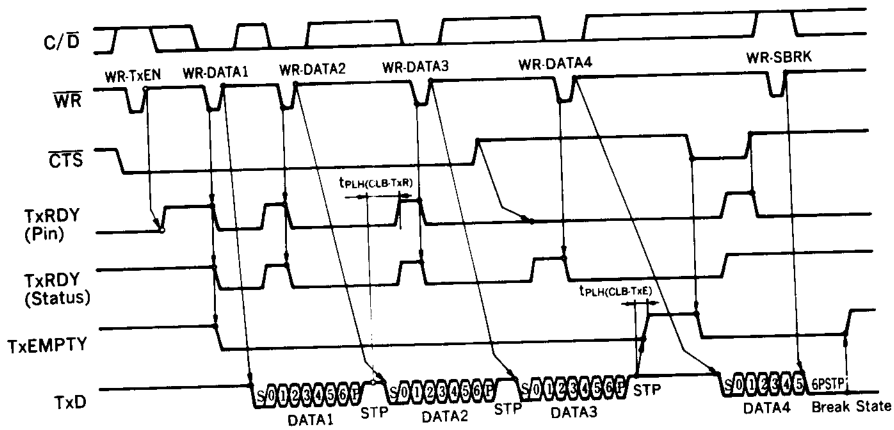

○ Write data cycle (CPU → USART)




○ Read data cycle (USART → CPU)

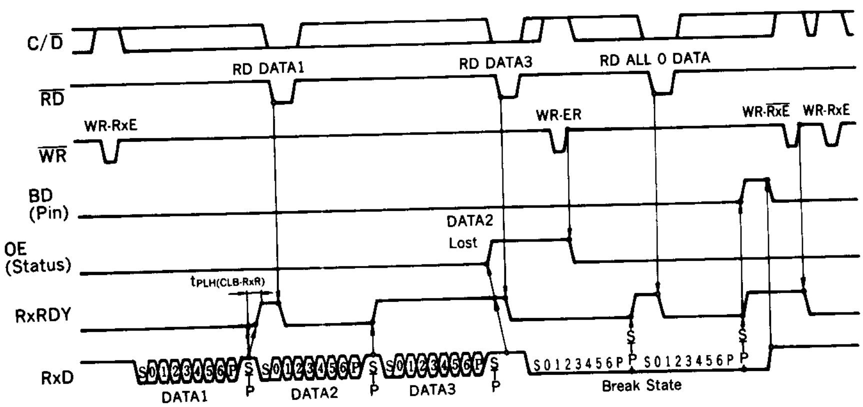


○Transmitter control & flag timing (async mode)



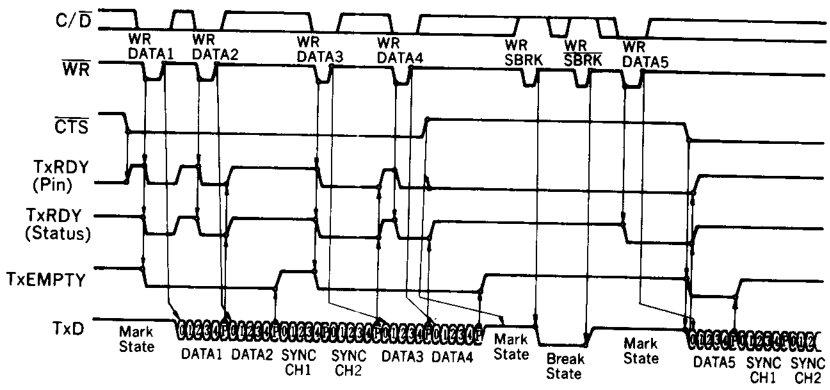

* 8 Example format = 7 bits/character with parity & 2 stop bits
* 9 TxRDY(pin) = 1 ← (Transmit-data buffer is empty)·(TxEN = 1)·($\overline{CTS}$ = L) = 1
* 10 TxRDY(status) = 1 ← (Transmit-data buffer is empty) = 1

○Receiver control & flag timing (async mode)



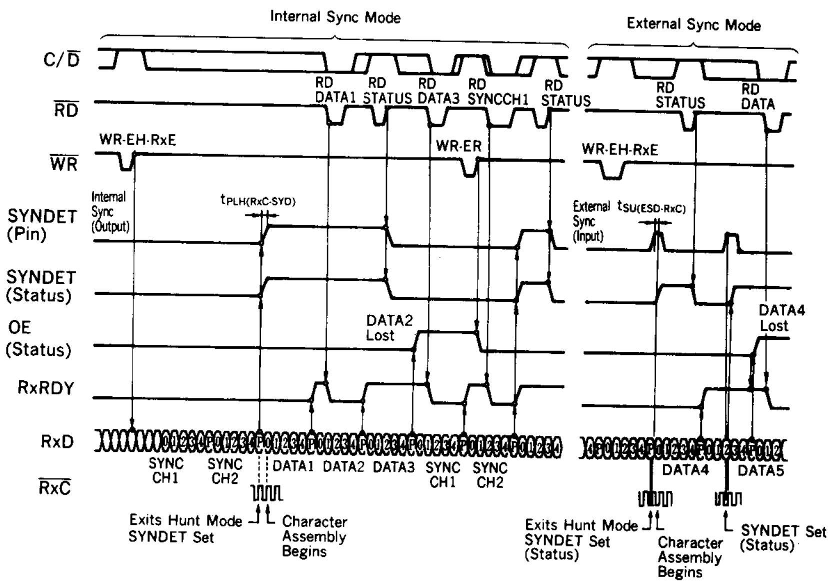

* 11 Example format = 7 bits/character with parity

○Transmitter control & flag timing (sync mode)




* Example format = 5 bits/character with parity, bi-sync characters.

○Receiver control & flag timing (sync mode)




* Example format = 5 bits/character with parity, bi-sync characters.

## ■FUNCTIONS

The SMC 82C51AC is used as a peripheral device and programmed to interface a CPU with virtually all serial data transmission techniques presently in use. Including IBM's "bi-sync". The SMC82C51AC can accept data characteristics from the CPU in parallel format, convert the data into a serial stream and transmit the data via the TxD pin. It can also receive data in a serial stream via the RxD pin, convert the data into a parallel format and transmit the data to the CPU. The SMC82C51AC, upon receipt of parallel or serial data, will flag the CPU using the TxRDY or RxRDY signals. The CPU can also poll the SMC82C51AC status with C/$\overline{D}$=1. The status which may be read contains Information such as data transmission error, parity error, overrun error or frame error.

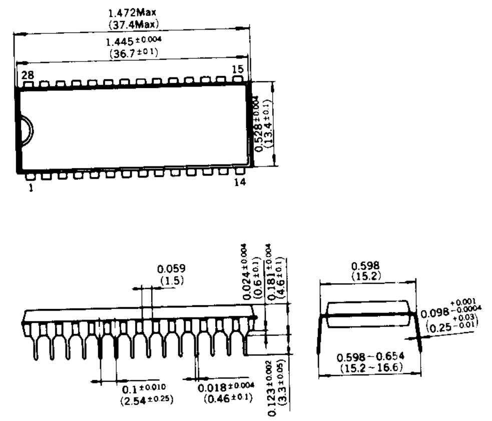
## ■APPLICATIONS

In 8-bit microcomputer applications, modem control of data communications.

Control of CRT, TTY and other terminal equipment.

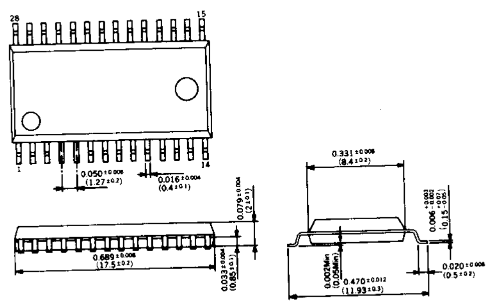
## ■PACKAGE DIMENSIONS

C28-8 28-pin DIP




unit : inch
(mm)

M28-8 28-pin SOP




unit : inch
(mm)