

# MN74HC4002/MN74HC4002S

## Dual 4-Input NOR Gates

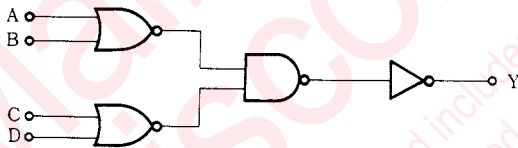
### ■ Outline

The MN74HC4002/MN74HC4002S consists of 4-input positive logic NOR gates, and has two built-in circuits in one chip.

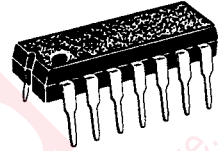
Owing to the silicon gate CMOS process, these NOR gates have realized low power consumption and high noise immunity equivalent to those of a standard CMOS and the operation speed as high as of an LS TTL. The buffer added to each gate output improves the input/output transfer characteristic and minimizes the propagation delay time fluctuation caused by the load capacity increase. The respective output can directly drive ten LS TTL inputs.

To protect the input and output against electrostatic breakdown, a resistor and a diode are used for the  $V_{CC}$  and the GND. The pin configuration and the function are the same as those of the standard CMOS logic 4000 family.

### ■ Logic Diagram

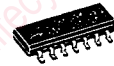


P-1



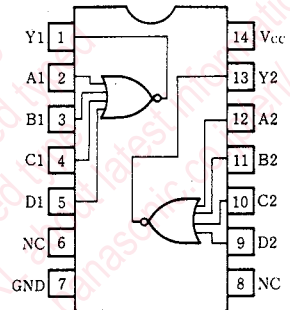
14-pin plastic DIL package

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14-pin PANAFLAT package (SO-14D)

### Pin Configuration



### ■ Absolute Maximum Ratings

Item		Symbol	Rating	Unit
Supply voltage		$V_{CC}$	$-0.5 \sim +7.0$	V
Input output voltage		$V_I, V_O$	$-0.5 \sim V_{CC} + 0.5$	V
Input protective diode current		$I_{IK}$	$\pm 20$	mA
Output parasitic diode current		$I_{OK}$	$\pm 20$	mA
Output current		$I_O$	$\pm 25$	mA
Supply current		$I_{CC}, I_{GND}$	$\pm 50$	mA
Storage temperature		$T_{stg}$	$-65 \sim +150$	$^{\circ}\text{C}$
Power dissipation	MN74HC4002	$T_a = -40 \sim +60^{\circ}\text{C}$	400	mW
		$T_a = +60 \sim +85^{\circ}\text{C}$	Decrease to 200mW at the rate of 8mW/ $^{\circ}\text{C}$	
	MN74HC4002S	$T_a = -40 \sim +60^{\circ}\text{C}$	275	mW
		$T_a = +60 \sim +85^{\circ}\text{C}$	Decrease to 200mW at the rate of 3.8mW/ $^{\circ}\text{C}$	

### ■ Recommended Operating Conditions

Item	Symbol	V <sub>CC</sub> (V)	Rating	Unit
Operating power supply voltage	V <sub>CC</sub>		1.4~6.0	V
Input output voltage	V <sub>I</sub> , V <sub>O</sub>		0~V <sub>CC</sub>	V
Operating temperature	T <sub>A</sub>		-40~+85	°C
Input rise, fall time	t <sub>r</sub> , t <sub>f</sub>	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

### ■ DC Characteristics (GND=0V)

Item	Symbol	V <sub>CC</sub> (V)	Test Condition		Temperature					Unit	
			V <sub>I</sub>	I <sub>O</sub>	T <sub>a</sub> =25°C			T <sub>a</sub> =-40~+85°C			
					Unit	min.	typ.	max.	min.		max.
Input voltage high level	V <sub>IH</sub>	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input voltage low level	V <sub>IL</sub>	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output voltage high level	V <sub>OH</sub>	2.0		-20.0	μA	1.9	2.0		1.9		V
		4.5		-20.0	μA	4.4	4.5		4.4		
		6.0	V <sub>IH</sub>	-20.0	μA	5.9	6.0		5.9		
		4.5		-4.0	mA	3.92			3.84		
		6.0		-5.2	mA	5.48			5.34		
Output voltage low level	V <sub>OL</sub>	2.0		20.0	μA	0.0	0.1		0.1		V
		4.5	V <sub>IH</sub>	20.0	μA	0.0	0.1		0.1		
		6.0	or	20.0	μA	0.0	0.1		0.1		
		4.5	V <sub>IL</sub>	4.0	mA			0.26		0.33	
		6.0		5.2	mA			0.26		0.33	
Input leakage current	I <sub>I</sub>	6.0	V <sub>I</sub> =V <sub>CC</sub> or GND					±0.1		μA	
Static supply current	I <sub>CC</sub>	6.0	V <sub>I</sub> =V <sub>CC</sub> or GND, I <sub>O</sub> =0					2.0		20.0	μA

### ■ AC Characteristics (GND=0V, Input transition time ≤ 6ns, C<sub>L</sub>=50pF)

Item	Symbol	V <sub>CC</sub> (V)	Test Condition	Temperature					Unit
				T <sub>a</sub> =25°C			T <sub>a</sub> =-40~+85°C		
				min.	typ.	max.	min.	max.	
Output rise time	t <sub>TLH</sub>	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t <sub>THL</sub>	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time (L→H)	t <sub>PLH</sub>	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Propagation time (H→L)	t <sub>PHL</sub>	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	

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