

# 5-bit multiplexed/1-bit latched 6-bit I<sup>2</sup>C EEPROM

# PCA9559

## FEATURES

- 5-bit 2-to-1 multiplexer, 1-bit latch
- 6-bit internal non-volatile register
- Internal non-volatile register programmable and readable via I<sup>2</sup>C bus
- Override input forces all outputs to logic 0
- 5 open drain multiplexed outputs
- 1 open drain non-multiplexed (latched) output
- 5V and 2.5V tolerant inputs
- Useful for 'jumperless' configuration of PC motherboards
- 2 address pins, allowing up to 4 devices on the I<sup>2</sup>C bus

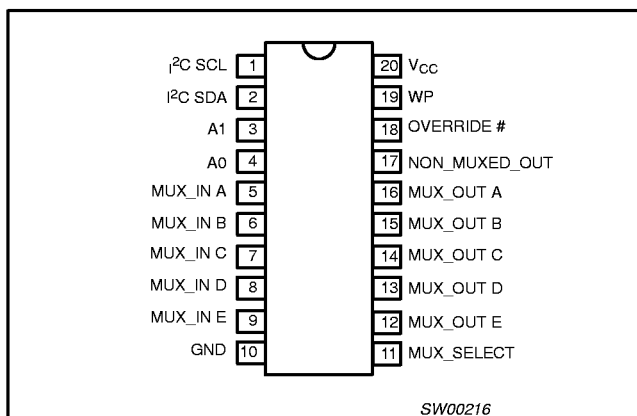
## DESCRIPTION

The primary function of the 5-bit multiplexer, 1-bit latch is to enable system configuration.

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
20-Pin Plastic TSSOP	0°C to +70°C	PCA9559 PW DH	SOT360-1

## PIN CONFIGURATION



## FUNCTIONAL DESCRIPTION

When the MUX\_SELECT signal is logic 0, the multiplexer will select the data from the non-volatile register to drive on the MUX\_OUT pins. When the MUX\_SELECT signal is logic 1, the multiplexer will select the MUX\_IN lines to drive on the MUX\_OUT pins. The MUX\_SELECT signal is also used to latch the NON\_MUXED\_OUT signal which outputs data from the non-volatile register. The NON\_MUXED\_OUT signal latch is transparent when MUX\_SELECT is in a logic 0 state, and will latch data when MUX\_SELECT is in a logic 1 state. When the active-LOW OVERRIDE# signal is set to logic 0 and the MUX\_SELECT signal is at a logic 0, all outputs will be driven to logic 0. This information is summarized in Table 1.

The Write Protect (WP) input is used to control the ability to write the contents of the 6-bit non-volatile register. If the WP signal is logic 0, the I<sup>2</sup>C bus will be able to write the contents of the non-volatile register. If the WP signal is logic 1, data will not be allowed to be written into the non-volatile register.

The factory default for the contents of the non-volatile register are all logic 0. These stored values can be read or written using the I<sup>2</sup>C bus (described in the next section).

The OVERRIDE#, WP, MUX\_IN, and MUX\_SELECT signals have internal pullup resistors. See the DC and AC Characteristics for hysteresis and signal spike suppression figures.

## FUNCTION TABLE

OVERRIDE#	MUX_SELECT	MUX_OUT OUTPUTS	NON_MUXED_OUT OUTPUT
0	0	All 0's	All 0's
0	1	MUX_IN inputs	Latched NON_MUXED_OUT <sup>1</sup>
1	0	From non-volatile register	From non-volatile register
1	1	MUX_IN inputs	From non-volatile register

### NOTE:

1. NON\_MUXED\_OUT state will be the value present on the output at the time of the MUX\_SELECT input transitioned from a logic 0 to a logic 1 state.

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## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	I <sup>2</sup> C SCL	Serial I <sup>2</sup> C bus clock
2	I <sup>2</sup> C SDA	Serial bi-directional I <sup>2</sup> C bus data
3	A1 Address	A1
4	A0 Address	A0
5	MUX_IN A	External inputs to multiplexer
6	MUX_IN B	
7	MUX_IN C	
8	MUX_IN D	
9	MUX_IN E	
10	GND	Ground
11	MUX_SELECT	Selects MUX_IN inputs or register contents for MUX_OUT outputs
12	MUX_OUT E	Open drain multiplexed outputs
13	MUX_OUT D	
14	MUX_OUT C	
15	MUX_OUT B	
16	MUX_OUT A	
17	NON_MUXED_OUT	Open drain outputs from non-volatile memory
18	OVERRIDE#	Forces all outputs to logic 0
19	WP	Non-volatile register write-protect
20	V <sub>CC</sub>	Positive voltage rail

## I<sup>2</sup>C INTERFACE

Communicating with this device is initiated by sending a valid address on the I<sup>2</sup>C bus. The address format (see Figure 1) has 5 fixed bits and two user-programmable bits followed by a 1-bit read/write value which determines the direction of the data transfer.

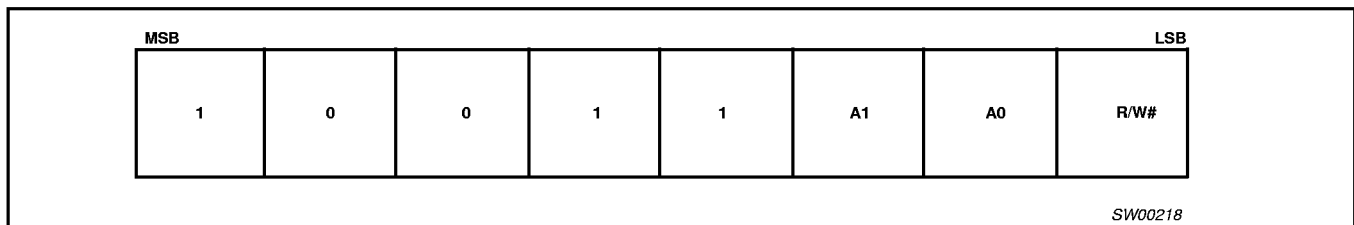


Figure 1. I<sup>2</sup>C Address Byte

Following the address and acknowledge bit are 8 data bits which, depending on the read/write bit in the address, will read data from or write data to the non-volatile register. Data will be written to the register if the read/write bit is logic 0 and the WP input is logic 0. Data will be read from the register if the bit is logic 1. The four high-order bits are latched outputs, while the four low order bits are multiplexed outputs (Figure 2).

### NOTE:

- To ensure data integrity, the non-volatile register must be internally write protected when V<sub>CC</sub> to the I<sup>2</sup>C bus is powered down or V<sub>CC</sub> to the component is dropped below normal operating levels.

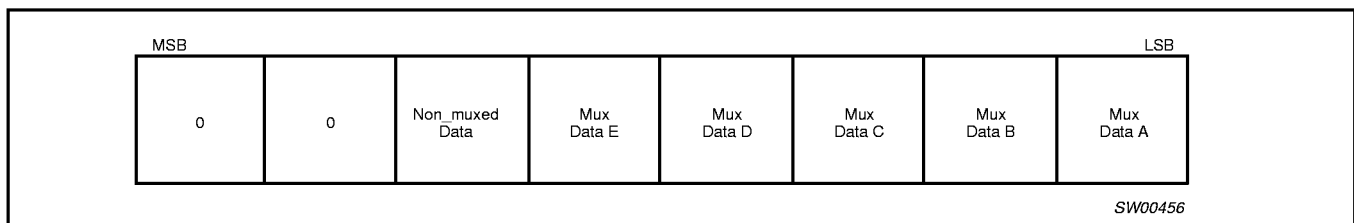
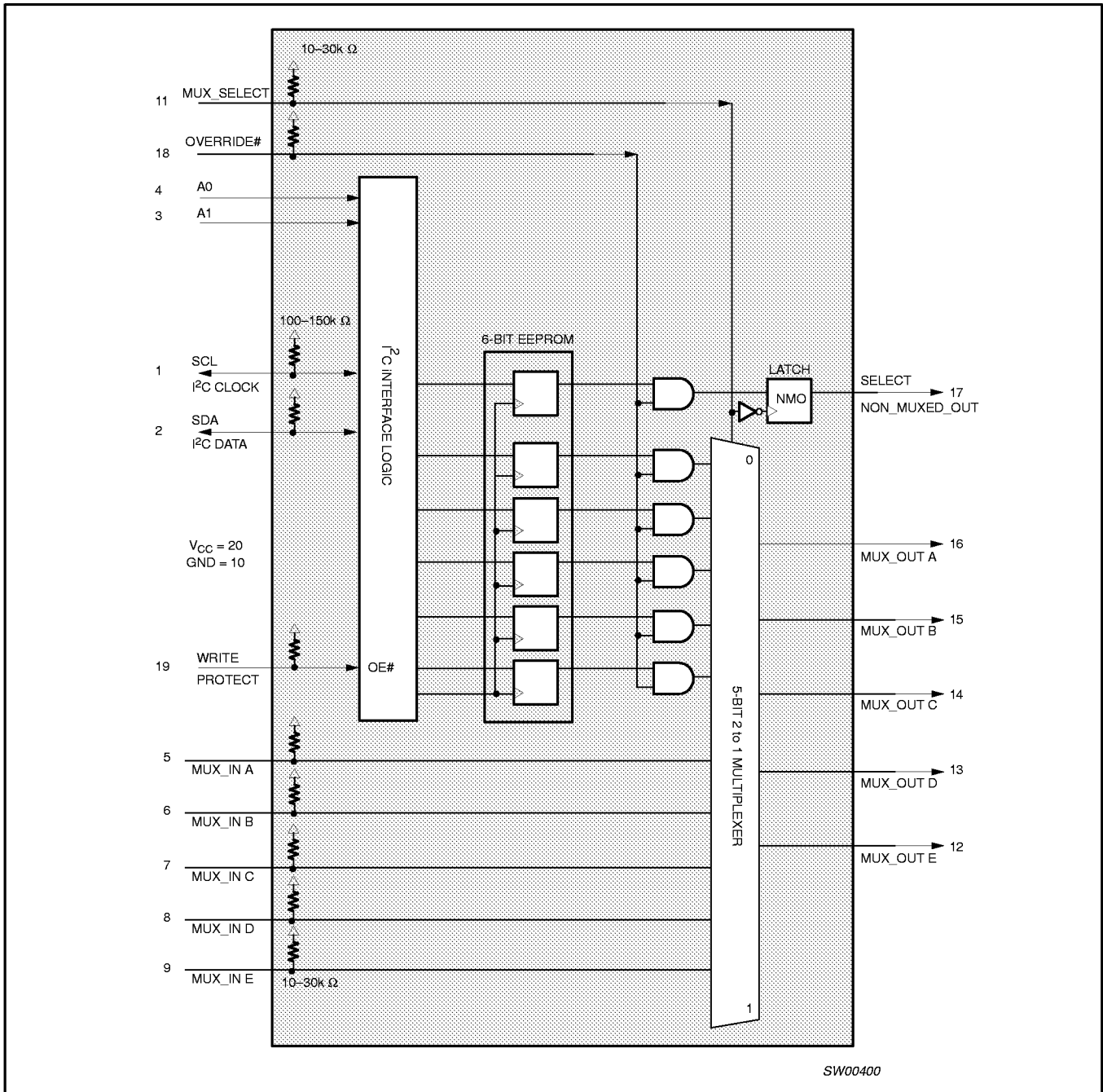


Figure 2. I<sup>2</sup>C Data Byte

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## BLOCK DIAGRAM



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## ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

In accordance with the Absolute Maximum Rating System (IEC 134)  
 Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5 to +4.6	V
V <sub>I</sub>	DC input voltage	Note 3	-1.5 to V <sub>CC</sub> +1.5	V
V <sub>OUT</sub>	DC output voltage	Note 3	-0.5 to V <sub>CC</sub> +0.5	V
T <sub>stg</sub>	Storage temperature range		-60 to +150	°C

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V <sub>CC</sub>	DC supply voltage		3.0	3.6	V
SCL, SDA	V <sub>IL</sub>	I <sub>OL</sub> = 3 mA	-0.5	0.9	V
	V <sub>IH</sub>	I <sub>OL</sub> = 3 mA	2.7	4.0	V
	V <sub>OL</sub>	I <sub>OL</sub> = 3 mA		0.4	V
	V <sub>OL</sub>	I <sub>OL</sub> = 6 mA		0.6	V
OVERRIDE#, MUX_IN, MUX_SELECT	V <sub>IL</sub>		-0.5	0.8	V
	V <sub>IH</sub>		2.0	4.0	V
MUX_OUT, NON_MUXED_OUT	I <sub>OL</sub>			8	mA
	I <sub>OH</sub>			100	µA
dt/dv	Input transition rise or fall time		0	10	ns/V
T <sub>amb</sub>	Operating temperature		0	70	°C

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## DC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN.	TYP.	MAX.	
<b>Supply</b>						
V <sub>CC</sub>	Supply Voltage		3		3.8	V
I <sub>CCL</sub>	Supply Current	Operating mode ALL inputs = 0 V			10	mA
I <sub>CCH</sub>	Supply Current	Operating mode ALL inputs = V <sub>CC</sub>			600	μA
<b>Input SCL: Input/Output SDA</b>						
V <sub>IL</sub>	Low Level Input Voltage		-0.5		0.8	V
V <sub>IH</sub>	High Level Input Voltage		2		V <sub>CC</sub> + 0.5	V
I <sub>OL</sub>	Low Level Output Current	V <sub>OL</sub> = 0.4	3			mA
I <sub>OL</sub>	Low Level Output Current	V <sub>OL</sub> = 0.6	6			mA
I <sub>IH</sub>	Leakage Current High	V <sub>I</sub> = V <sub>CC</sub>	-1.5		-12	μA
I <sub>IL</sub>	Leakage Current Low	V <sub>I</sub> = GND	-7		-32	μA
C <sub>I</sub>	Input Capacitance				10	pF
<b>Override #, WP, Mux_Select</b>						
I <sub>IH</sub>	Leakage Current High	V <sub>I</sub> = V <sub>CC</sub>	-20		-100	μA
I <sub>IL</sub>	Leakage Current Low	V <sub>I</sub> = GND	-86		-267	μA
C <sub>I</sub>	Input Capacitance				10	pF
<b>Mux A → E</b>						
I <sub>IH</sub>	Leakage Current High	V <sub>I</sub> = V <sub>CC</sub>	-0.166		-0.75	mA
I <sub>IL</sub>	Leakage Current Low	V <sub>I</sub> = GND	-0.72		-2	mA
C <sub>I</sub>	Input Capacitance				10	pF
<b>A0, A1 Inputs</b>						
I <sub>IH</sub>	Leakage Current High	V <sub>I</sub> = V <sub>CC</sub>	-1		1	μA
I <sub>IL</sub>	Leakage Current Low	V <sub>I</sub> = GND	-1		1	μA
C <sub>I</sub>	Input Capacitance				10	pF
<b>Mux Outputs</b>						
V <sub>OL</sub>	Low Level Output Current	(I <sub>OL</sub> = 100 μA)			0.4	V
V <sub>OL</sub>	Low Level Output Current	(I <sub>OL</sub> = 2 mA)			0.7	V
<b>Non_Mux_Output</b>						
V <sub>OL</sub>		(I <sub>OL</sub> = 100 μA)			0.4	V
V <sub>OL</sub>		(I <sub>OL</sub> = 2 mA)			0.7	V

**NOTES:**

- V<sub>HYS</sub> is the hysteresis of Schmitt-Trigger inputs

## NON-VOLATILE STORAGE SPECIFICATIONS

PARAMETER	SPECIFICATION
Memory cell data retention	10 years min
Number of memory cell write cycles	3,000 cycles min

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## AC CHARACTERISTICS

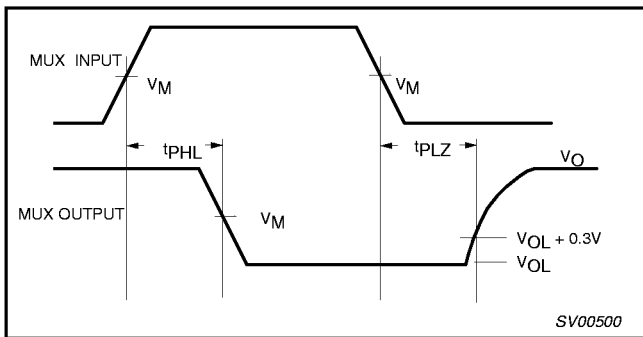
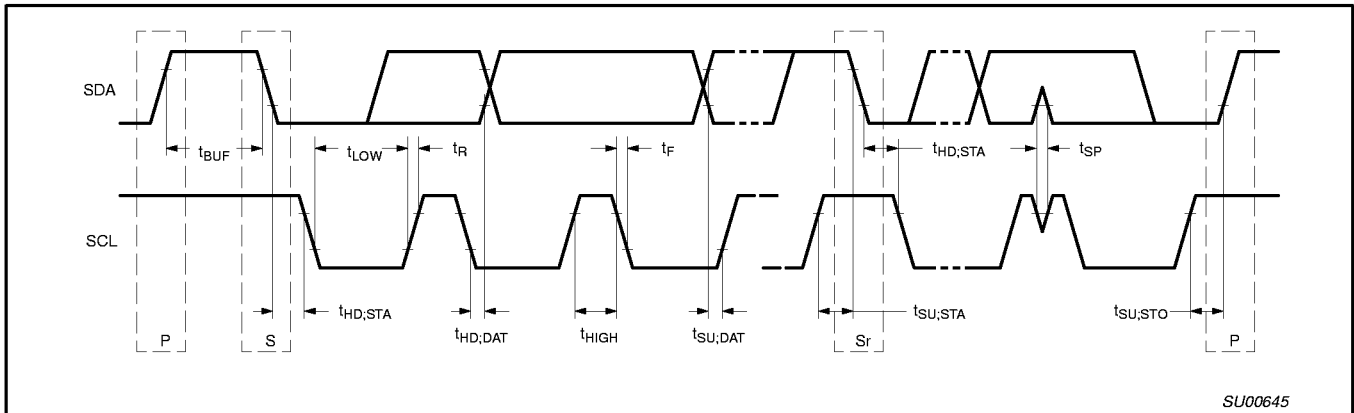
SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP.	MAX.	
<b>MUX_in ⇒ MUX_out</b>					
T <sub>plh</sub>			28	37	nS
T <sub>phl</sub>			16	21	nS
<b>Select ⇒ MUX_out</b>					
T <sub>plh</sub>			30	39	nS
T <sub>phl</sub>			17	22	nS
<b>Override ⇒ Non-MUX_out</b>					
T <sub>plh</sub>			34	43	nS
T <sub>phl</sub>			19	25	nS
<b>Override ⇒ MUX_out</b>					
T <sub>plh</sub>			31	41	nS
T <sub>phl</sub>			21	27	nS
T <sub>R</sub>	Output rise time	1.0		3	ns/V
T <sub>F</sub>	Output fall time	1.0		3	ns/V
P <sub>F</sub>	Pull-up resistor for outputs	1.0			ns/V
C <sub>L</sub>	Test load capacitance on outputs				pF
<b>I<sup>2</sup>C Bus</b>					
t <sub>SCL</sub>	SCL clock frequency	10		400	kHz
t <sub>BUF</sub>	Bus free time between a STOP and a START condition	1.3			μs
t <sub>HD:STA</sub>	Hold time (repeated) START condition. After this period, the first clock pulse is generated	600			ns
t <sub>LOW</sub>	LOW period of SCL clock	1.3			μs
t <sub>HIGH</sub>	HIGH period of SCL clock	600		-12	ns
t <sub>SU:STA</sub>	Set-up time for a repeated START condition	600		-32	ns
t <sub>HD:DAT</sub>	Data hold time	0		10	ns
t <sub>SU:DAT</sub>	Data set-up time	100		-100	ns
t <sub>SP</sub>	Data spike time	0		50	ns
t <sub>SU:STO</sub>	Set-up time for STOP condition	600		10	ns
t <sub>R</sub>	Rise time for both SDA and SCL signals (10 – 400 pF bus)	20		300	ns
t <sub>f</sub>	Fall time for both SDA and SCL signals (10 – 400 pF bus)	20		300	ns
C <sub>L</sub>	Capacitive load for each bus line			400	pF
T <sub>W</sub>	Write cycle time <sup>1</sup>		15		mS

## NOTE:

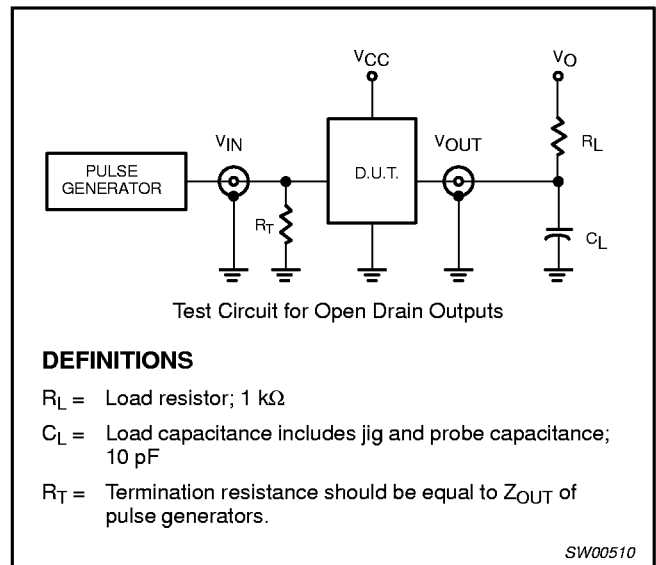
1. WRITE CYCLE time can only be measured indirectly during the write cycle. During this time, the device will not acknowledge its I<sup>2</sup>C Address.

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Waveform 1. Open drain output enable and disable times



DEFINITIONS

- $R_L$  = Load resistor; 1 k $\Omega$
- $C_L$  = Load capacitance includes jig and probe capacitance; 10 pF
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

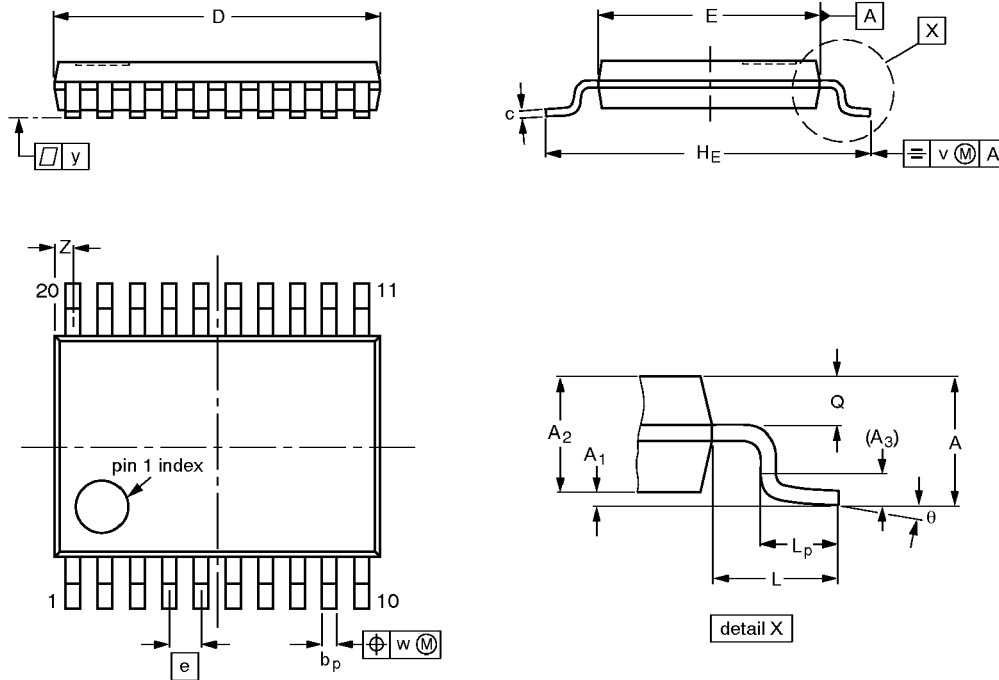
SW00510

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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				-93-06-16 95-02-04