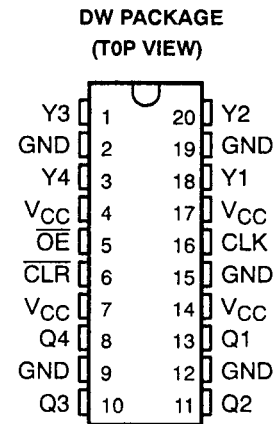


SN74ABT337 CLOCK DRIVER WITH 3-STATE OUTPUTS

SCB3003 D3657, JANUARY 1991

- State-Of-The-Art EPIC-IIIB™ BiCMOS Design Significantly Reduces Power Dissipation
- Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications
- Four Outputs Toggle at the Clock Frequency, Four Outputs Switch at One-Half the Clock Frequency
- Advanced BiCMOS Design With TTL-Compatible Inputs and Outputs
- $f_{max} = 80$ MHz
- High-Drive Outputs Eliminate the Need for External Buffering
- Distributed V_{CC} and Ground Pins Reduce Switching Noise
- Packaged in Plastic “Small Outline” Package



description

The 'ABT337 contains four buffered outputs that switch at the clock frequency and four divide-by-two outputs that switch at one-half the clock frequency. When the output-enable (\overline{OE}) input is low and the clear (\overline{CLR}) input is high, the Y outputs follow the clock (CLK) input and the Q outputs switch on the low-to-high transition of CLK.

This clock driver is specifically designed for applications requiring synchronized output signals at both the clock frequency and one-half the clock frequency. Taking \overline{CLR} low asynchronously sets the Q outputs to a low level. High-drive outputs (± 48 mA) eliminate the need for external buffering of output signals.

The SN74ABT337 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUTS	
\overline{OE}	\overline{CLR}	CLK	Y1–Y4	Q1–Q4
H	X	X	Z	Z
L	L	L	L	L
L	L	H	H	L
L	H	L	L	Q_0
L	H	H	H	Q_0
L	H	\uparrow	\uparrow	$\overline{Q_0}$

Q_0 = the level of the Q outputs before the indicated steady-state input conditions were established.

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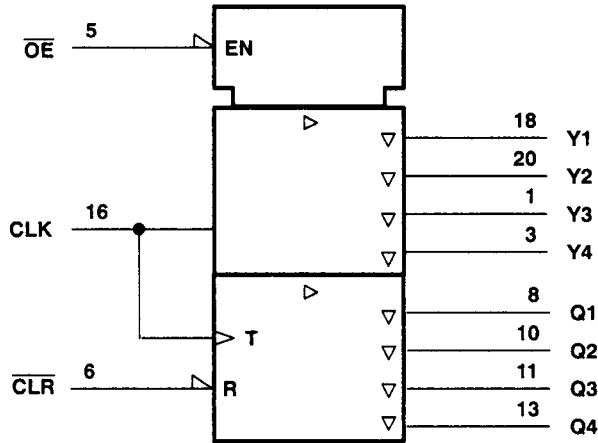
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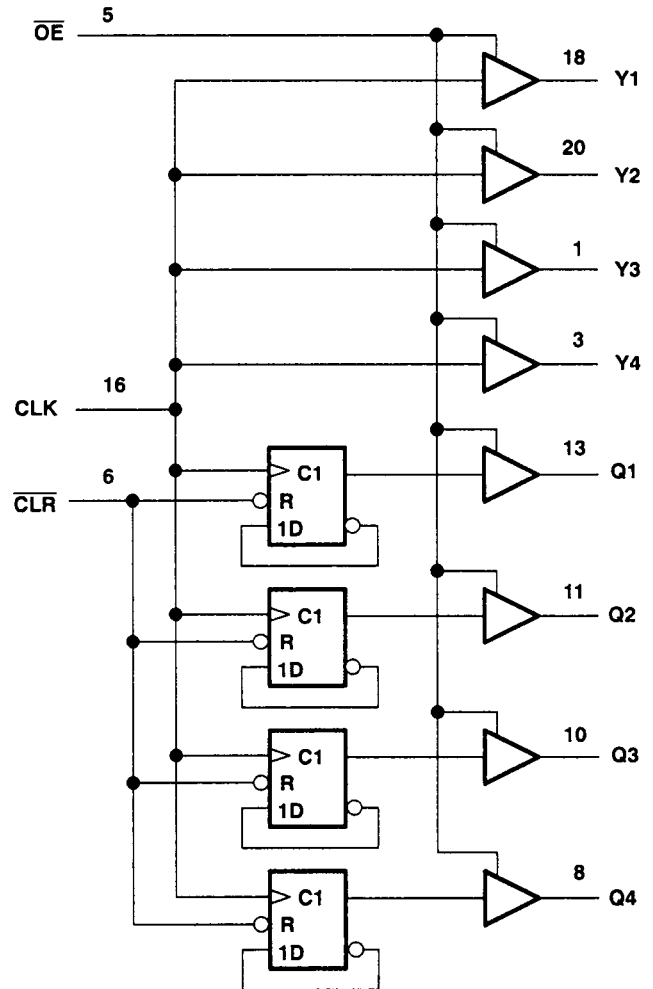
SN74ABT337 CLOCK DRIVER WITH 3-STATE OUTPUTS

logic symbol †



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) ‡

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state, V_O	-0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O	96 mA
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

SN74ABT337 CLOCK DRIVER WITH 3-STATE OUTPUTS

recommended operating conditions

		SN74ABT337		UNIT
		MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	V
V _{IH}	High-level input voltage	2		V
V _{IL}	Low-level input voltage		0.8	V
V _I	Input voltage	0	V _{CC}	V
I _{OH}	High-level output current		-48	mA
I _{OL}	Low-level output current		48	mA
T _A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN74ABT337			UNIT
		MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2	V
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -48 mA	3.5			V
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 48 mA			0.5	V
I _{OZ}	V _{CC} = 5.5 V				μA
I _I	V _{CC} = 5.5 V				μA
I _{CC}	V _{CC} = 5.5 V, V _I = V _{CC} or GND, I _O = 0	Outputs high			mA
		Outputs low			
		Outputs disabled			
C _i	V _I = 2.5 V or 0.5 V		5.5		pF
C _o	V _O = 2.5 V or 0.5 V				pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

timing requirements over recommended operating free-air temperature range

		SN74ABT337		UNIT
		MIN	MAX	
f _{clock}	Clock frequency	0	80	MHz
t _w	Pulse duration	CLR low		ns
		CLK high or low		
t _{su}	Setup time, CLR inactive before CLK↑			ns

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switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT337		UNIT
			MIN	MAX	
f_{max}			80		MHz
t_{PLH}	CLK	Any Y or Q			ns
t_{PHL}					
t_{PHL}	\overline{CLR}	Any Q			ns
t_{PZH}	\overline{OE}	Any Y or Q			ns
t_{PZL}					
t_{PHZ}	OE	Any Y or Q			ns
t_{PLZ}					
$t_{sk(o)}$	CLK	Any Y or Q			ns
$t_{sk(p)}$					

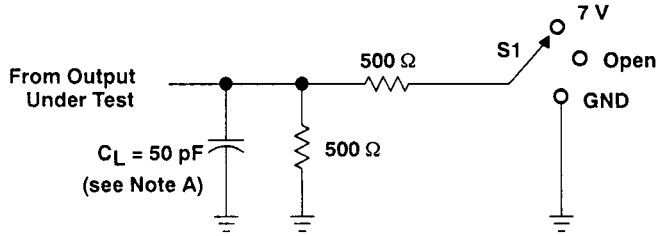
- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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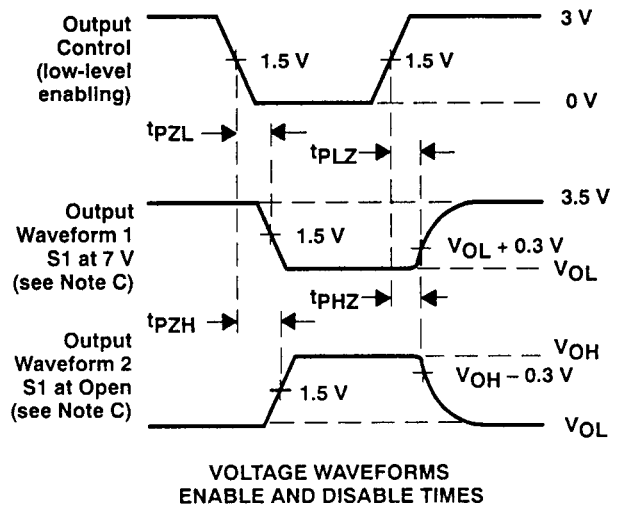
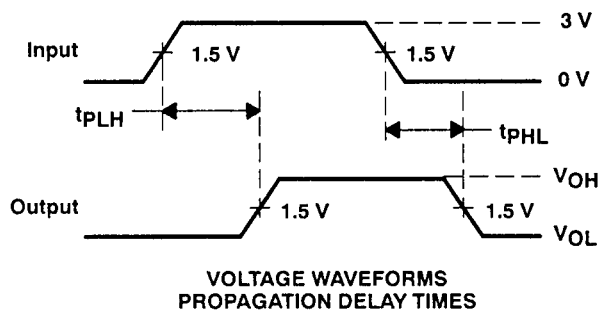
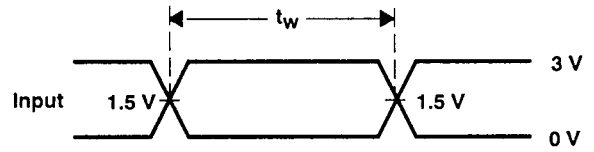
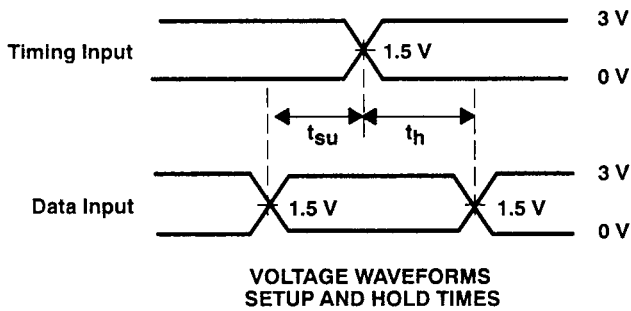


PARAMETER MEASUREMENT INFORMATION



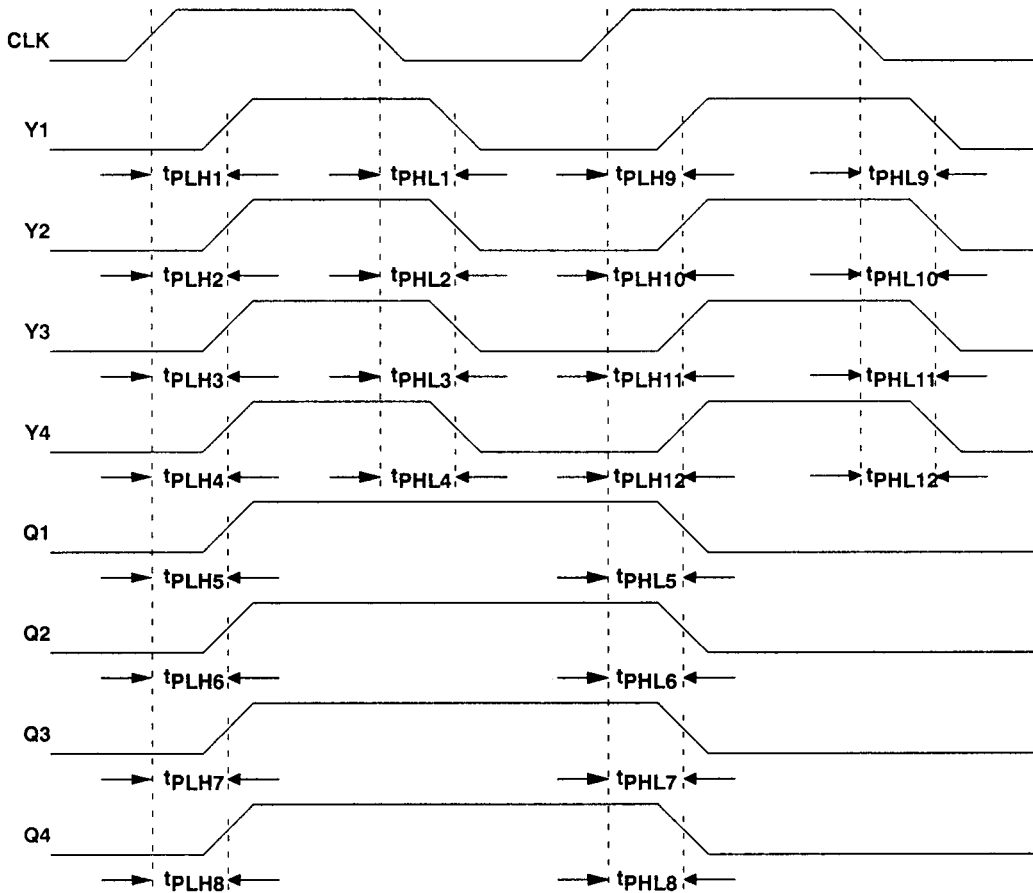
LOAD CIRCUIT FOR OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



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WAVEFORMS FOR CALCULATION OF $t_{sk(o)}$, $t_{sk(p)}$



Output skew, $t_{sk(o)}$, is calculated as the greater of:

- a) the difference between the fastest and slowest of t_{PLHn} ($n = 1, 2, \dots, 8$),
- b) the difference between the fastest and slowest of t_{PHLn} ($n = 1, 2, 3, 4$),
- c) the difference between the fastest and slowest of t_{PHLn} ($n = 9, 10, 11, 12$), and
- d) the difference between the fastest and slowest of t_{PLHn} ($n = 9, 10, 11, 12$) and t_{PHLn} ($n = 5, 6, 7, 8$).

Pulse skew, $t_{sk(p)}$, is calculated as the greater of $|t_{PLHn} - t_{PHLn}|$ ($n = 1, 2, \dots, 12$).

Figure 2. Skew Waveforms and Calculations