M-986-2A1 MF Transceiver

- **Direct A-Law or μ-Law PCM digital input**
- **2.048 Mb/s clocking**
- **Operates with standard codecs for analog interfacing**
- **Microprocessor read/write interface**
- **Binary or 2-of-6 data formats**
- **Dual-channel**
- **5 volt power**
- **Applications include: test equipment, trunk adapters, paging terminals, traffic recorders, PBXs**

The M-986-2A1 dual channel MF Transceiver contains all the logic necessary to transmit and receive (North American) CCITT Region 1 multifrequency signals on one integrated circuit (IC).

Operating with a 20.48 MHz crystal, the M-986 is capable of providing a direct digital interface to a μ-law or A-law encoded PCM digital input. Each channel can be connected to an analog source using a coder-decoder (codec) as shown in Figure 1.

The M-986 is configured and controlled through an integral coprocessor port.

Functional Description

The M-986-2A1 can be set up for various modes of operation by writing two configuration bytes to the coprocessor port. The format of the two configuration bytes is shown in Table 1 and the configuration options are described in the following paragraphs.

Configuration Options

External/Internal Codec Clock (ECLK): If external codec clocking is selected, an external clocking source provides an 8 kHz transmit framing clock and an 8 kHz receive framing clock. It also provides a serial bit clock with a frequency that is a multiple of 8 kHz between 216 kHz and 2.496 MHz for exchange of data via the serial ports. When internal codec clocking is selected, the M-986-2A1 provides an 8 kHz framing clock and a 2.048 MHz serial bit clock.

2 of 6/Binary Input/Output (IOM): When the 2-of-6 input/output is selected, the M-986-2A1 encodes the received R1 MF tone pair into a 6-bit format, where each bit represents one of the six possible frequencies. A logic high level indicates the presence of a frequency. The digital input to the M-986-2A1 that selects the transmitted R1 MF tone pair must also be coded in the 2-of-6 format. See Table 2.

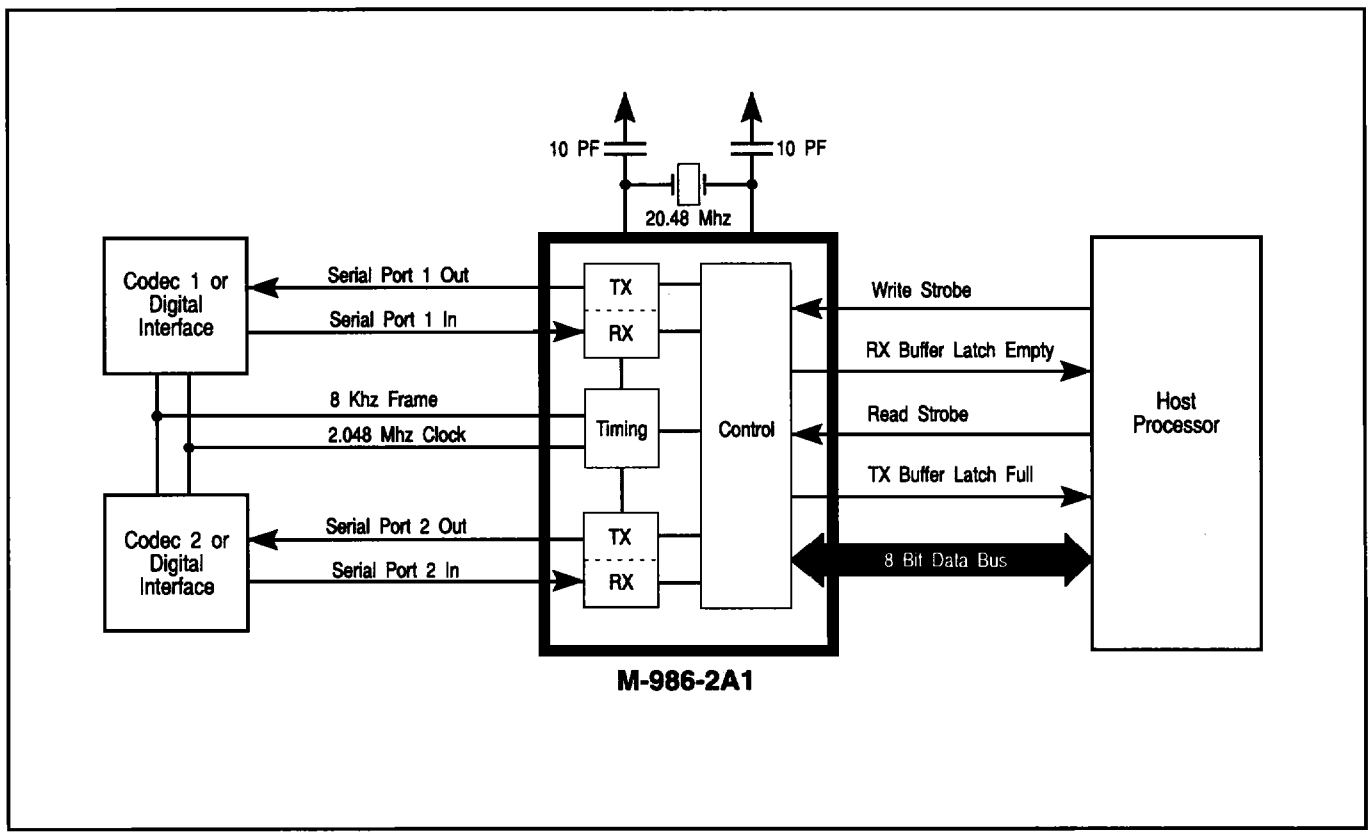


Figure 1 Block Diagram

When binary input/output is selected, the M-986-2A 1encodes the received R1 MF tone pair into a 4 bit binary format. The digital input to the M-986-2A1 that selects the transmitted R1 MF tone pair must also be coded in a 4 bit binary format. See Table 3.

Enable/Disable Channel (ENC): When a channel is disabled, the receiver does not process its codec input for R1 MF tones, and the transmitter does not respond to transmit commands. If a transmit command is given while the channel is enabled, the "tone off" command must be given before the channel is disabled. Disabling the channel does not automatically shut off the transmitter. When a channel is enabled, the receiver and transmitter for that channel function normally.

Long/Short KP Tone Detection Time (KPL): When long KP tone detection is selected, the minimum on time for the KP tone to be detected is 55 milliseconds. When short KP tone detection is selected, the minimum on time for the KP tone to be detected is 30 milliseconds (the same as the minimum on time for the rest of the MF tones).

Enable MF Tone Detection After Reception of KP (KPEN): When this feature is enabled, MF tone detection is enabled after reception of the KP tone, and disabled after reception of ST, ST1, ST2, or ST3 tones. When this feature is disabled, MF tone detection is always enabled. Select A or μ-law input/output (AMU) for A-law encoding, this bit is set to a 1, for μ-law encoding it is set to 0.

Initial Configuration: The configuration of the M-986-2A1 immediately after a reset will be as follows:

- channel disabled
- 2-of-6 input/output
- external serial and serial frame clocks.

Also, the M-986-2A1 will place a 00 hex on the coprocessor port to indicate to the host processor that it is working.

Transmit Tone Command

The transmit tone command allows the host processor to transmit any two of the 6 R1 MF frequencies. The format of the command depends on whether the M-986 is configured for binary format or 2-of-6 format. See Tables 2 and 3.

Received Tone Detection

When a tone is detected by the M-986, the $\overline{\text{TBLF}}$ output goes low, indicating reception of the tone to the host processor. The host processor can determine which tone was detected and which channel the tone was detected on by reading data from the M-986 coprocessor port. The M-986 will return a single byte indicating the tone received and the channel that the tone was received on. The format of the returned byte depends on whether the M-986 is configured for binary or 2-of-6 coding. See Tables 2 and 3.

Coprocessor Port

Commands are written to the M-986 via the coprocessor port, and data indicating the received R1 MF tone is read from the coprocessor port.

Writing to the Coprocessor Port: The following sequence describes writing a command to the M-986.

(1) The $\overline{\text{WR}}$ signal is driven low by the host processor.

(2) The $\overline{\text{RBLE}}$ (receive buffer latch empty) signal transitions to a logic high level.

(3) Data is written from D7-D0 to the receive buffer latch (D7-D0) when the $\overline{\text{WR}}$ signal goes high.

(4) The $\overline{\text{RBLE}}$ signal transitions to a logic low level after the M-986 reads the data. This signals the host processor that the receive buffer is empty.

Note: The $\overline{\text{RBLE}}$ should be low before writing to the coprocessor.

Table 1 Configuration Bytes

Configuration Byte 1							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	0	ECLK	IOM	ENCI	KPL1	KPEN1	0

ECLK	Channels 1 & 2	1 = External codec clock; 0 = Internal codec clock
IOM	Channels 1 & 2	1 = Binary input/output; 0 = 2-of-6 input/output
ENC1	Channel 1	1 = Enable channel; 0 = Disable channel
KPL1	Channel 1	1 = 55 ms detection time for KP; 0 = 30 ms detection time for KP
KPEN1	Channel 1	1 = Enable MF tone detection after KP detection; 0 = MF tone detection always on

Configuration Byte 2							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	1	0	AMU	ENC2	KPL2	KPEN2	0

AMU	Channels 1 & 2	1 = A-law Encoding, 0 = μ-law Encoding
ENC2	Channel 2	1 = Enable channel; 0 = Disable channel
KPL2	Channel 2	1 = 55 ms detection time for KP; 0 = 30 ms detection time for KP
KPEN2	Channel 2	1 = Enable MF tone detection after KP detection; 0 = MF tone detection always

Reading the Coprocessor Port: The following sequence describes reading received tone information from the coprocessor port.

(1) The $\overline{\text{TBLF}}$ (transmit buffer latch full) port pin on the M-986 goes low indicating the reception of a tone.

(2) The host processor detects the low logic level on the $\overline{\text{TBLF}}$ pin either by polling a connected port pin or by an interrupt.

(3) The host processor drives the $\overline{\text{RD}}$ signal low.

(4) The $\overline{\text{TBLF}}$ (transmit buffer latch full) signal transitionto a logic high level.

(5) Data is driven onto D7-D0 by the M-986 until the $\overline{\text{RD}}$ signal is driven high by the host processor.

Clock Characteristics and Timing

Internal Clock Option: The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN. The frequency of CLKOUT is one-fourth the crystal fundamental frequency. The crystal should be 20.48 MHz, fundamental mode, and parallel resonant, with an effective series resistance of 30 ohms, a power dissipation of 1 mW, and be specified at a load capacitance of 20 pF.

External Clock Option: An external frequency source can be used by injecting the frequency directly in X2/CLKIN with X1 left unconnected. The external frequency injected must conform to the specifications listed in Table 8.

Flammability/Reliability Specifications

Reliability:	185 FITS failures/billion hours
Flammability:	Passes UL 94 V-0 tests

Ordering Information

M-986-2A1P	40-pin plastic DIP
M-986-2A1PL	44-pin PLCC

Table 2 2 of 6 Coding Format

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit tone command	1	CHN	F6	F5	F4	F3	F2	F1
Receive tone return	0	CHN	F6	F5	F4	F3	F2	F1

CHN: 1 = channel 2; 0 = channel 1

R1 MF Frequencies:

Bit name	Frequency (Hz)	Bit name	Frequency (Hz)
F6	1700	F3	1100
F5	1500	F2	900
F4	1300	F1	700

Table 3 Binary Coding Format

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit tone command	1	CHN	0	0	A	B	C	D
Receive tone return	0	CHN	0	0	A	B	C	D

CHN: 1 = channel 2; 0 = channel 1

R1 MF Frequencies:

ABCD	Frequencies (Hz)	Name	ABCD	Frequencies (Hz)	Name
0 0 0 0	Tone off	—	1 0 0 0	900 & 1500	Digit 8
0 0 0 1	700 & 900	Digit 1	1 0 0 1	1100 & 1500	Digit 9
0 0 1 0	700 & 1100	Digit 2	1 0 1 0	1300 & 1500	Digit 0
0 0 1 1	900 & 1100	Digit 3	1 0 1 1	700 & 1700	ST3
0 1 0 0	700 & 1300	Digit 4	1 1 0 0	900 & 1700	ST1
0 1 0 1	900 & 1300	Digit 5	1 1 0 1	1100 & 1700	KP
0 1 1 0	1100 & 1300	Digit 6	1 1 1 0	1300 & 1700	ST2
0 1 1 1	700 & 1500	Digit 7	1 1 1 1	1500 & 1700	ST

Table 4 Signal Descriptions

Signal	Pin	I/O/Z	Description
D15-D8	18-11	I/O/Z	Unused. Leave open.
D7-D0	19-26	I/O/Z	8-bit coprocessor latch.
$\overline{TBLF}$	40	O	Transmit buffer latch full flag.
$\overline{RBLE}$	1	O	Receive buffer latch empty flag.
HI/$\overline{LO}$	2	I	Latch byte select pin. Tie low.
$\overline{BIO}$	9	I	Unused. Leave open.
$\overline{RD}$	32	I/O	Used by the external processor to read from the coprocessor latch by driving the $\overline{RD}$ line active (low), thus enabling the output latch to drive the latched data. When the data has been read, the external device must bring the $\overline{RD}$ line high.
$\overline{EXINT}$	5	I	Unused. Leave open.
MC	3	I	Microcomputer mode select pin. Tie low.
MC/$\overline{PM}$	27	I	Coprocessor mode select pin. Tie low.
$\overline{RS}$	4	I	Reset input for initializing the device. When an active low is placed on $\overline{RS}$ pin for a minimum of five clock cycles, $\overline{RD}$ and $\overline{WR}$ are forced high, and the data bus (LD7 through LD0) goes to a high impedance state. The serial port clock and transmit outputs also go to the high impedance state.
$\overline{WR}$	31	I/O	Used by the external processor to write data to the coprocessor port. To write data the external processor drives the $\overline{WR}$ line low, places data on the data bus, and then drives the $\overline{WR}$ line high to clock the data into the on-chip latch.
XF	28	O	Watchdog signal. Toggles at least once every 10 milliseconds when the processor is functioning properly. If the pin is not toggled at least once every 10 ms, the processor is lost and should be reset.
CLKOUT	6	O	System clock output (one-fourth crystal/CLKIN frequency, nominally 5.12 MHz).
V_{SS}	10	I	Ground pin.
V_{CC}	30	I	5V supply pin.
X1	7	O	Crystal output pin for internal oscillator. If the internal oscillator is not used, this pin should be left unconnected.
X2/CLKIN	8	I	Input pin to the internal oscillator (X2) from the crystal. Alternatively, an input pin for the external oscillator (CLKIN).
DR1 & DR0	33 & 29	I	Serial-port receive-channel inputs. 2.048 MHz serial data is received in the receive registers via these pins. DR0 = channel 1; DR1 = channel 2.
FR	37	O	8 kHz internal serial-port framing output. If internal clocking is selected, serial-port transmit and receive operations occur simultaneously on an active (high) FR framing pulse.
DX1 & DX0	36 & 35	O	Serial-port transmit-channel outputs. 2.048 MHz serial data is transmitted from the transmit registers on these pins. These outputs are in the high-impedance state when not transmitting. DX0 = channel 1; DX1 = channel 2.
$\overline{FSR}$	39	I	8 kHz external serial-port receive-framing input. If external clocking is selected, data is received via the receive pins (DR1 and DR0) on the active (low) FSR input. The falling edge of FSR initiates the receive process, and the rising edge causes the M-986 to process the data.
SCLK	34	I/O/Z	2.048 MHz serial-port clock. Master clock for transmitting and receiving serial-port data. Configured as an input in external clocking mode or output in internal clocking mode. Reset ($\overline{RS}$) forces SCLK to the high-impedance state.
$\overline{FSX}$	38	I	8 kHz external serial-port transmit-framing input. If external clocking is enabled, data is transmitted on the transmit pins (DX1, DX0) on the active (low) input. The falling edge of FSX initiates the transmit process, and the rising edge causes the M-986 to internally load data for the next cycle.

Table 5 Absolute Maximum Ratings Over Specified Temperature Range5

Supply voltage range, V_{CC}	-0.3 V to 7 V
Input voltage range	-0.3 V to 15 V
Output voltage range	-0.3 V to 15 V
Ambient air temperature range	0° to 150°C
Storage temperature range	-45°C to 150°C

Table 6 Serial Port Timing

Parameter		Min	Nom	Max	Unit
t_d (CH-FR)	Internal framing delay from SCLK rising edge			70	ns
t_d (DX1-CL)	DX bit 1 valid before SCLK falling edge	20			ns
t_d (DX2-CL)	DX bit 2 valid before SCLK falling edge	20			ns
t_h (DX)	DX hold time after SCLK falling edge	244			ns
t_{su} (DR)	DR setup time before SCLK falling edge	20			ns
t_h (DR)	DR hold time after SCLK falling edge	20			ns
t_c (SCLK)	Serial port clock cycle time	399	488.28	4770	ns
t_f (SCLK)	Serial port clock fall time			30	ns
t_r (SCLK)	Serial port clock rise time			30	ns
t_w (SCLKL)	Serial port clock low-pulse duration*	220	244.14	2500	ns
t_w (SCLKH)	Serial port clock high-pulse duration*	220	244.14	2500	ns
t_{su} (FS)	$\overline{FSX}/\overline{FSR}$ setup time before SCLK falling edge	100			ns
* The duty cycle of the serial port clock must be within 45% to 55%.					

Table 7 Electrical Characteristics/Temperature Range

Parameter			Test Conditions		Min	Typ	Max	Unit
I_{CC}	Supply current		f = 20.5 MHz, V_{CC} = 5.5V, T_A = 0° to 70 °C			50	75	mA
V_{OH}	High-level output voltage		I_{OH} = MAX		2.4	3		V
			I_{OH} = 20 µ A		V_{CC} -0.4			V
V_{OL}	Low-level output voltage		I_{OL} = MAX			0.3	0.6	V
I_{OZ}	Off-state output current		V_{CC} = MAX	V_O = 2.4 V			20	µA
				V_O = 0.4 V			-20	µA
I_I	Input current		V_I = V_{SS} to V_{CC}	Except CLKIN			±20	µA
				CLKIN			±50	µA
C_I	Input capacitance	Data bus	f = 1 MHz, all other pins 0 V			25		pF
		All others				15		pF
C_O	Output capacitance	Data bus				25		pF
		All others				10		pF

Table 8 External Frequency Specifications

Parameter		Min	Nom	Max	Unit
$t_{C(MC)}$	Master clock cycle time	48.818	48.828	48.838	ns
$t_{r(MC)}$	Rise time master clock input		5	10	ns
$t_{f(MC)}$	Pulse duration master clock	20			ns

Table 9 Recommended Operating Conditions

Parameter			Min	Nom	Max	Unit
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	All inputs except CLKIN	2			V
		CLKIN	3			V
		MC/PM	2.2			V
V_{IL}	Low-level input voltage	All inputs except MC/$\overline{MP}$			0.8	V
		MC/$\overline{MP}$			0.6	V
I_{OH}	High-level output current (all outputs)				-300	µA
I_{OL}	Low-level output current (all outputs)				2	mA
T_A	Operating free-air temperature		0		70	°C

Table 10 Coprocessor Interface Timing

Parameter		Min	Nom	Max	Unit
$t_{d(R-A)}$	RD low to $\overline{TBLF}$ high			75	ns
$t_{d(W-A)}$	$\overline{WR}$ low to $\overline{RBLE}$ high			75	ns
$t_{a(RD)}$	RD low to data valid			80	ns
$t_{h(RD)}$	Data hold time after $\overline{RD}$ high	25			ns
$t_{su(WR)}$	Data setup time prior to $\overline{WR}$ high	30			ns
$t_{h(WR)}$	Data hold time after $\overline{WR}$ high	25			ns
$t_{w(RDL)}$	$\overline{RD}$ low-pulse duration	80			ns
$t_{w(WRL)}$	$\overline{WR}$ low-pulse duration	60			ns
$t_{wr(RBLE)}$	$\overline{RBLE}\downarrow$ to $\overline{RBLE}\uparrow$			1	ms

Table 11 Reset (RS) Timing

Parameter		Test Conditions	Min	Max	Unit
$t_{dis(R)}$	Data bus disable time after $\overline{RS}$	R_L = 825 Ω, C_L = 100 pF		75	ns
t_{d12}	Delay time from $\overline{RS}\downarrow$ to high-impedance SCLK			200	ns
t_{d13}	Delay time from $\overline{RS}\downarrow$ to high-impedance DX1, DX0			200	ns
tsu(R)	Reset ($\overline{RS}$) setup time prior to CLKOUT		50		ns
tw(R)	RS pulse duration		245		ns

Table 12 CLKOUT Timing Parameters

Parameter		Test Conditions	Min	Nom	Max	Unit
$t_{c(C)}$	CLKOUT cycle time	R_L = 825 Ω, C_L = 100 pF	195.27	195.31	195.35	ns
$t_{r(C)}$	CLKOUT rise time			10		ns
$t_{f(C)}$	CLKOUT fall time			8		ns
$t_{d(MCC)}$	Delay time CLKIN$\uparrow$ to CLKOUT$\downarrow$		25		60	ns
$t_{d\,8}$	Delay time CLKOUT $\downarrow$ to data bus OUT valid				¼ $t_{c(C)}$+75	ns

Table 13 Transmitter Characteristics

	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{OS}	Frequency offset	From nominal			±1	Hz
TW	Twist	High/low			±0.5	dB
A_S	Signal amplitude	Per component	-7.40	-7.00	-6.60	dBm0
T_S	Time skew	Between components			0	ms
P_{hi}	Power due to extraneous components				-30	dB

Table 14 Receiver Characteristics

	Parameter	Test Conditions	Min	Max	Unit
A_d	Detect amplitude	Per frequency	-30	-5	dBm0
A_{nd}	No-detect amplitude	Per frequency	-40	-30	dBm0
F_d	Detect with frequency offset	From nominal	±1.5% +5Hz		Hz
TW_d	Detect with twist	High tone/low tone	±6		dB
T_{on}	Tone time	Reject	10		ms
T_{int}	Interrupted tone time	Reject	10		ms
Ti	Tone interpulse time		25		ms
KPL_d	KP long tone detect time	Long detect time enabled	55		ms
KP_d	KP short tone detect time	Long detect time disabled	30		ms
T_d	Tone detect time		30		ms
N_t	Noise tolerance	≤ 1 error in 25,000 digits		-20	dB
N_i	Impulse noise	≤ 1 error in 25,000 digits		-12	dB
P_{60}	60 Hz tolerance	≤ 1 error in 25,000 digits		81	dBrnc0
T_{180}	180 Hz tolerance	≤ 1 error in 25,000 digits		68	dBrnc0
M_t	Modulation products tolerance	2A-B and 2B-A products		-28	dB

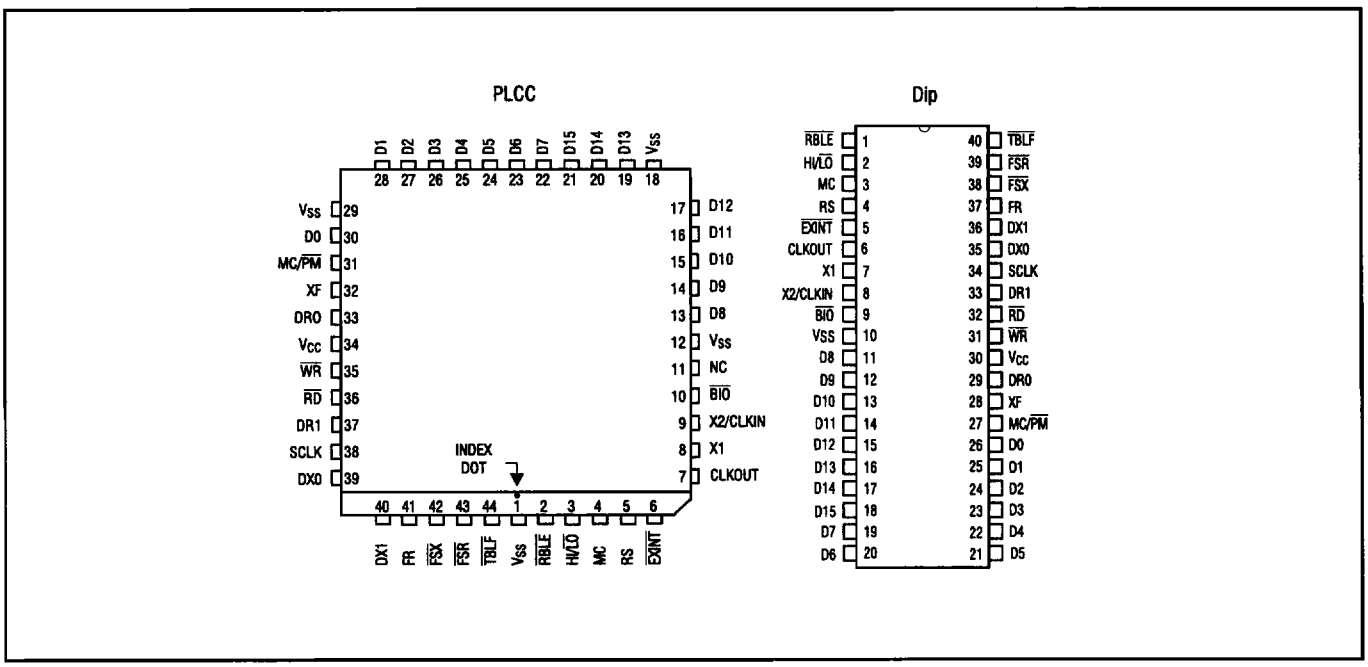
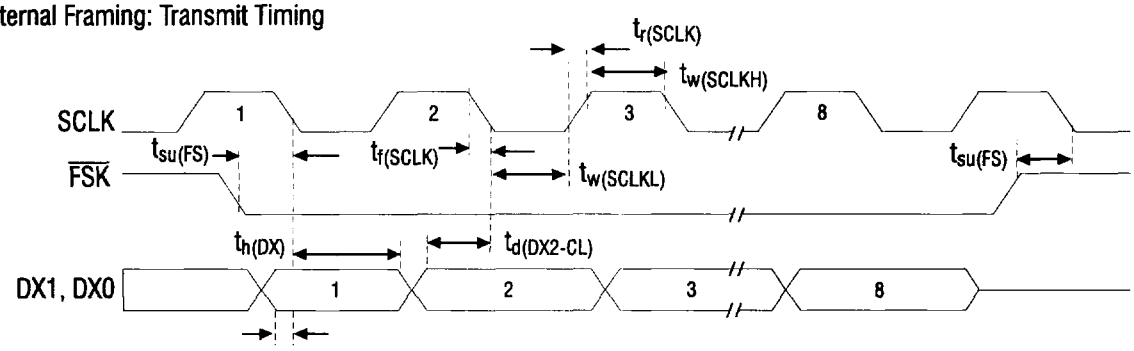


Figure 2 Pin Assignments

External Framing: Transmit Timing



NOTES: Data valid on transmit outputs until SCLK rises.
The most significant bit is shifted first.

External Framing: Receive Timing

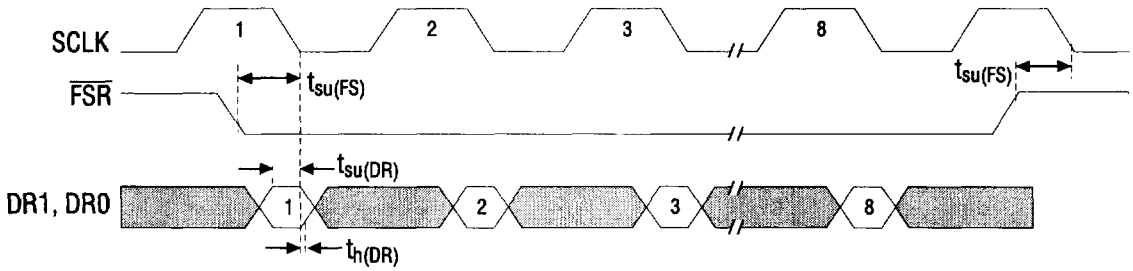
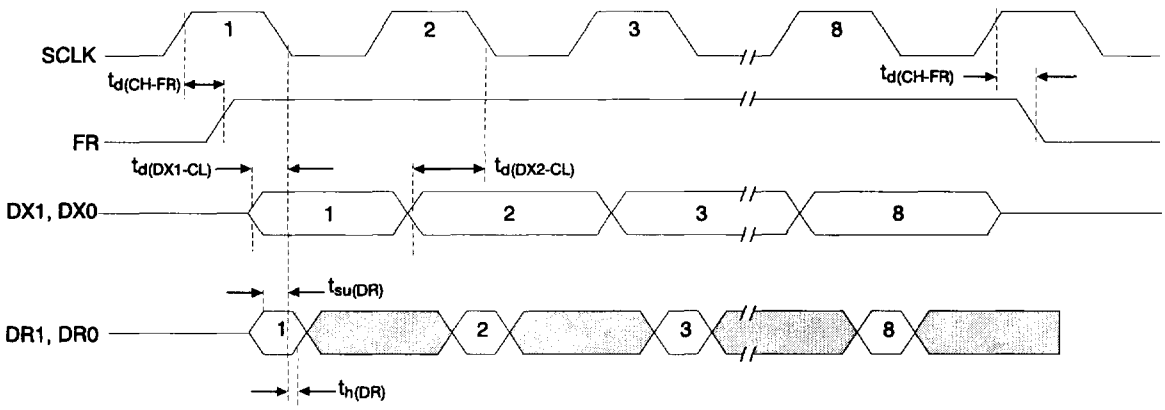


Figure 3 External Framing Timing Diagrams

Internal Framing



Note: The most significant bit is shifted first.

Figure 4 Internal Framing Timing

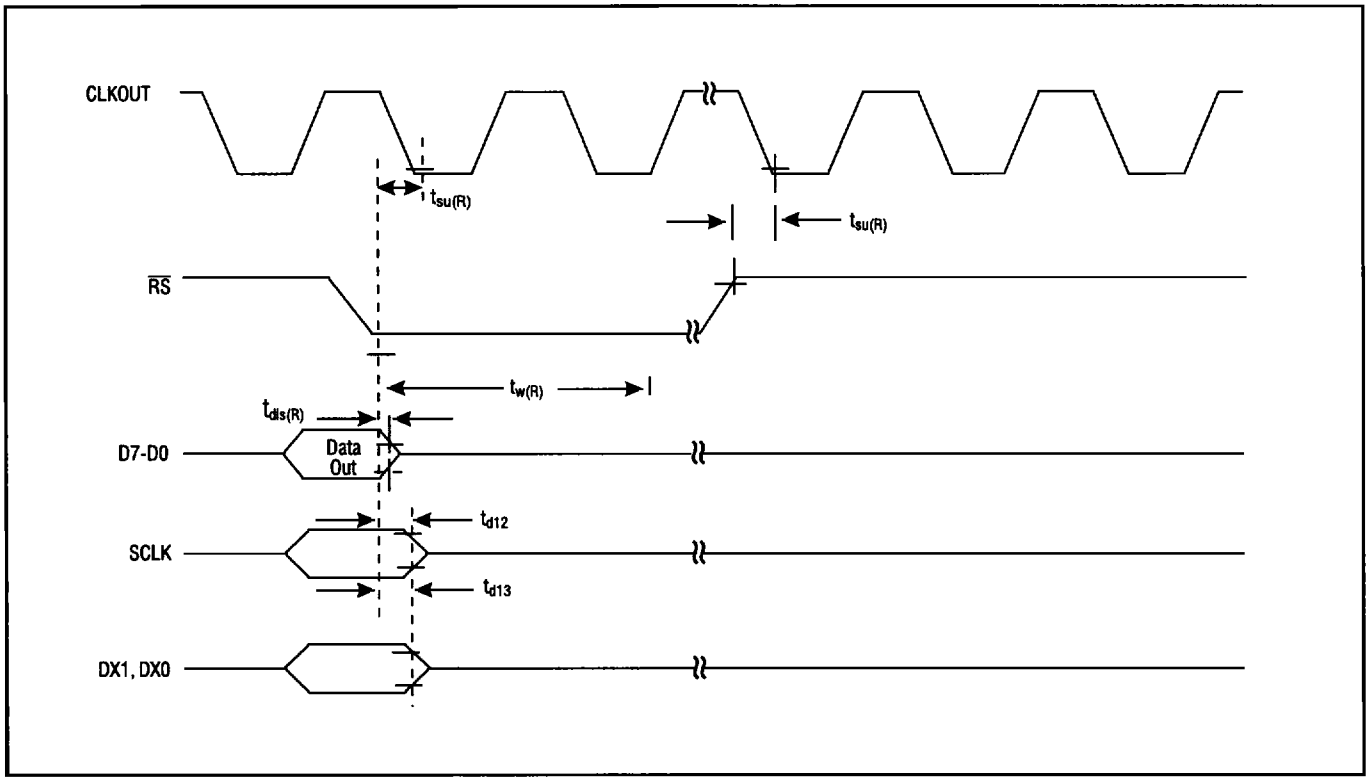


Figure 5 Reset Timing

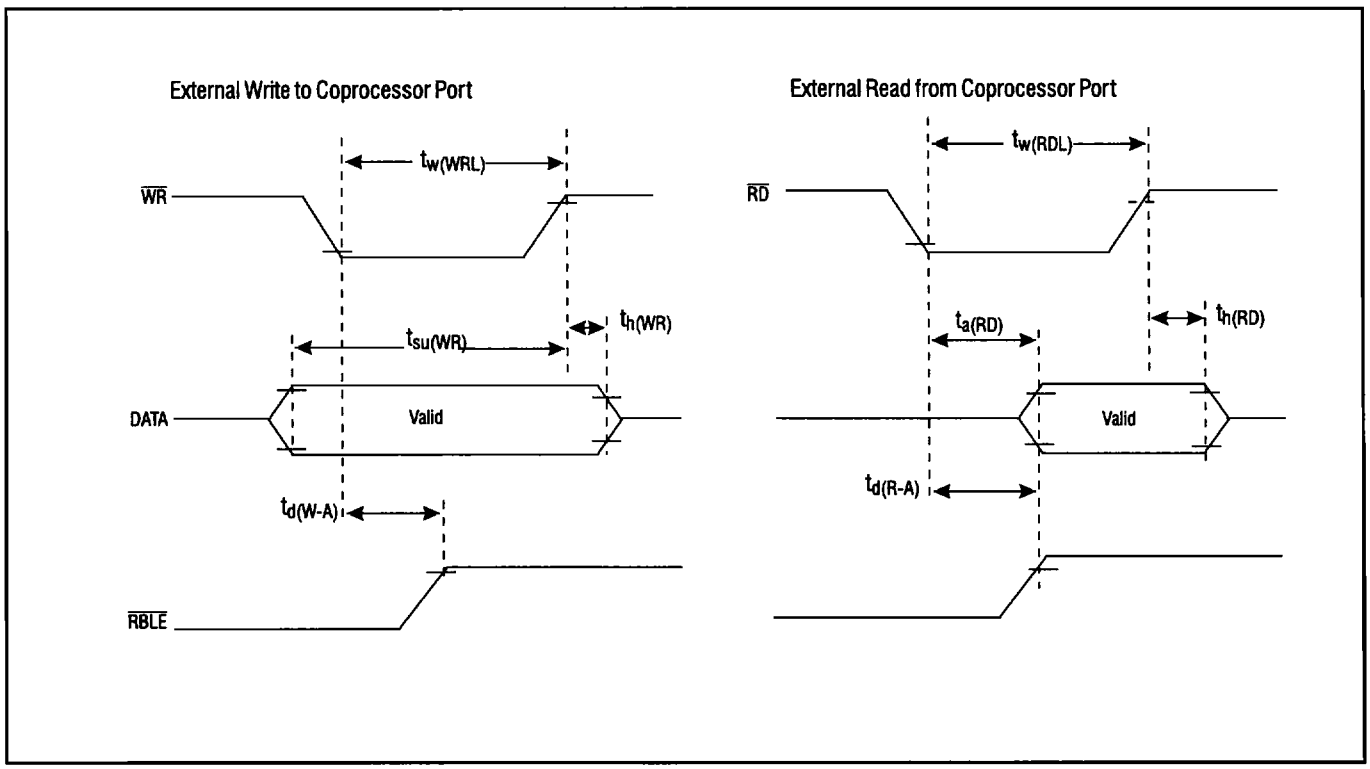


Figure 6 Coprocessor Timing

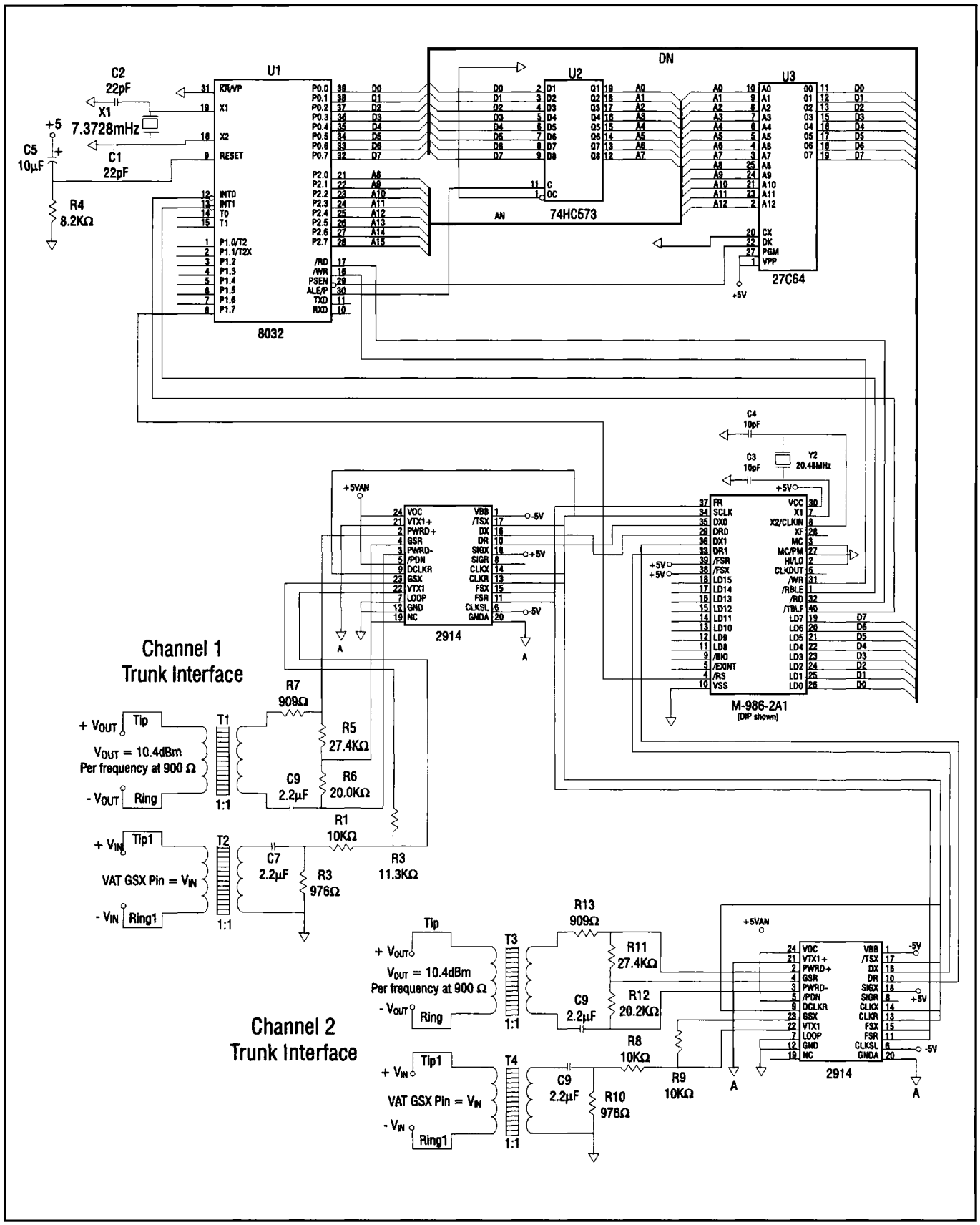
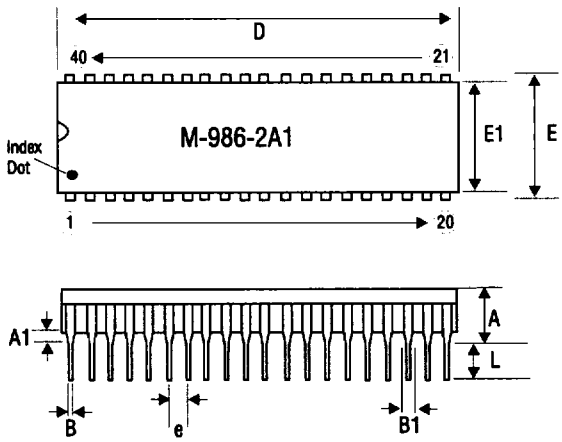


Figure 7 M-986 Dual Channel 4-wire Interface Application Circuit

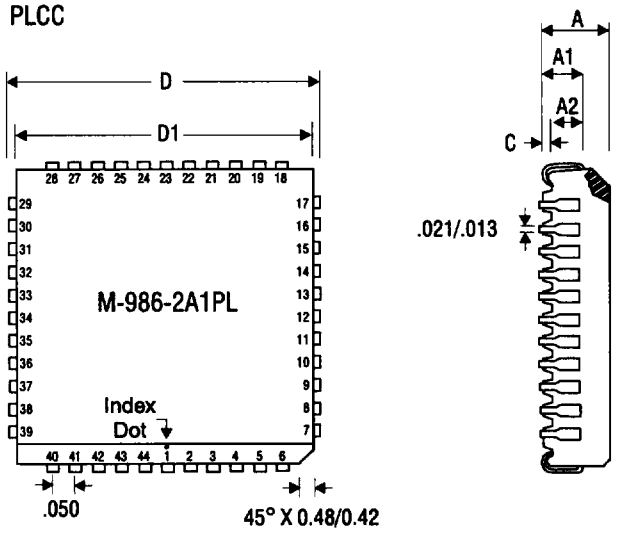
Drawing not to scale.
Drawing does not reflect actual part marking.

DIP



	Tolerances			
	(inches)		Metric (mm)	
	Min	Max	Min	Max
A		.250		6.35
A1	.015		.39	
B	.014	.022	.36	.56
B1	.030	.070	.77	1.78
C	.008	.015	.20	.38
D	1.98	2.095	50.30	53.20
E	.600	.625	15.24	15.87
E1	.485	.580	12.32	14.73
e	.100 BSC		2.54 BSC	
L	.115	.200	2.93	5.08

PLCC



	Tolerances			
	Inches		Metric (mm)	
	Min	Max	Min	Max
A	.165	.180	4.19	4.57
A1	.090	.20	2.29	5.08
A2	.062	.083	1.58	2.11
C	.020 min		.51 min	
D	.685	.695	17.40	17.65
D1	.650	.653	16.51	16.66

Figure 8 Package Dimensions