KS54HCTLS / KS74HCTLS 299

8-Bit Universal Shift/Storage Registers with 3-State Outputs

T-46-09-05

FEATURES

- Multiplexed I/O ports provides improved bit density
- Four modes of operation: hold (store), shift, shift left, and load data
- Operates with outputs enabled or at high impedance
- Can be cascaded for N-bit word lengths
- Direct overriding clear
- Application:
  Stacked or push-down registers, buffer storage, and accumulator registers
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with drive current
  (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

DESCRIPTION

These eight-bit universal registers feature multiplexed I/O ports to achieve full eight-bit data handling. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines S0 and S1 high. This places the three-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs asynchronously when $\overline{CLR}$ is low. Pulling either of the output controls, $\overline{G}1$ or $\overline{G}2$, high disables the outputs but this has no effect on clearing, shifting, or storage of data.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

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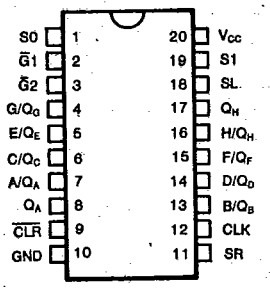
PIN CONFIGURATION



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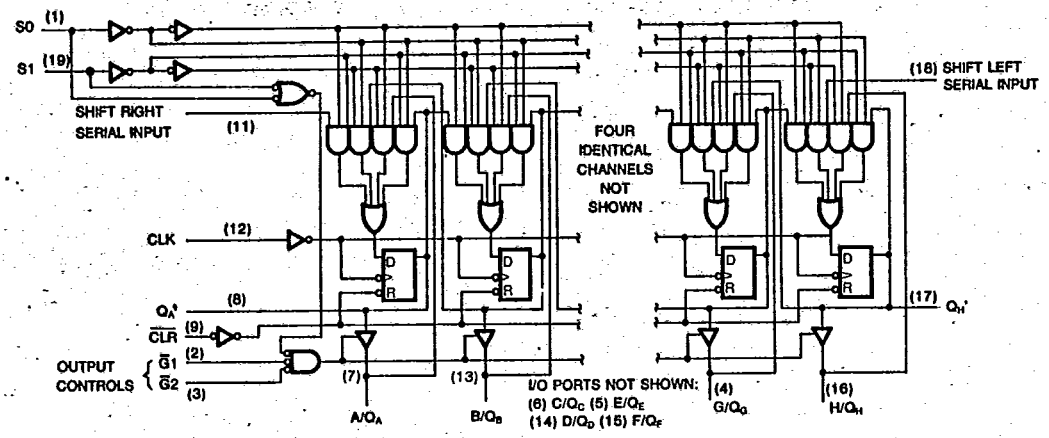
LOGIC DIAGRAM



FUNCTION TABLE

Mode	Inputs							I/O Ports								Outputs	
	$\overline{CLR}$	S1	S0	Output Control $\overline{G1}$	Output Control $\overline{G2}$	CLK	SL	SR	A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	Q_A'	Q_H'
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

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Absolute Maximum Ratings*

Supply Voltage Range V_{CC} . . . . . −0.5V to +7V
DC Input Diode Current, I_{IK}
(V_I < −0.5V or V_I > V_{CC} +0.5V) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
(V_O < −0.5V or V_O > V_{CC} +0.5V) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
(−0.5V < V_O < V_{CC} +0.5V) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a=25°C	KS74HCTLS T_a=−40°C to +85°C	KS54HCTLS T_a=−55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL} I_O=−20μA Q'A and Q'H outputs: I_O= −4mA QA thru QH outputs: I_O= −6mA	V_{CC} 4.2 4.2	V_{CC} −0.1 3.98 3.84	V_{CC} −0.1 3.84 3.7	V_{CC} −0.1 3.7	V
Mixmum Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL} I_O=20μA Q'A and Q'H outputs: I_O=4mA I_O=8mA QA thru QH outputs: I_O=12mA I_O=24mA	0	0.1 0.26 0.39 0.26 0.39	0.1 0.33 0.5 0.33 0.5	0.1 0.4 0.4	V
Maximum Input Current	I_{IN}	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable = V_{IN} V_{OUT}=V_{CC} or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin V_I=2.4V other inputs: at V_{CC} or GND I_{OUT}=0μA		2.7	2.9	3.0	mA

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8-Bit Universal Shift/Storage Registers with 3-State Outputs

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AC ELECTRICAL CHARACTERISTICS (Input t_r, t_f≤6 ns), HCTLS299

Characteristic		Symbol	Conditions†		T_a=25°C, V_{CC}=5.0V Typ	T_a=25°C, V_{CC}=5.0V	KS74HCTLS T_a=−40°C to +85°C, V_{CC}=5.0V±10%	KS54HCTLS T_a=−55°C to +125°C, V_{CC}=5.0V± 10%	Unit
					Typ	Guaranteed Limits			
Maximum Clock Frequency		f_{max}			35	25	20	18	MHz
Maximum Propagation Delay, CLK to Q'_A or Q'_H		t_{PLH}	C_L=50pF		26	35	4	53	ns
		t_{PHL}			26	35	44	53	
Maximum Propagation Delay, $\overline{CLR}$ to Q'_A or Q'_H		t_{PHL}			30	40	50	60	ns
Maximum Propagation Delay, CLK to Q_A thru Q_H		t_{PLH}	C_L=50pF		24	32	40	48	ns
			C_L=150pF		27	35	45	54	
		t_{PHL}	C_L=50pF		24	32	40	48	
			C_L=150pF		27	35	45	54	
Maximum Propagation Delay, $\overline{CLR}$ to Q_a thru Q_H		t_{PHL}	C_L=50pF		30	40	50	60	ns
			C_L=150pF		33	43	55	66	
Maximum Output Enable Time, $\overline{G1}$, $\overline{G2}$, to Q_A thru Q_H		t_{PZH}	R_L=1kΩ	C_L=50pF	20	26	33	39	ns
				C_L=150pF	23	29	38	45	
		t_{PZL}		C_L=50pF	20	26	33	39	
				C_L=150pF	23	29	38	45	
Maximum Output Disable Time, $\overline{G1}$, $\overline{G2}$ to Q_A thru Q_H		t_{PHZ}	R_L=1kΩ		13	17	21	26	ns
		t_{PLZ}	C_L=50pF		13	17	21	26	
Minimum Pulse Width	CLK High or Low	t_w			10	13	17	20	ns
	$\overline{CLR}$ Low				10	13	17	20	
Minimum Setup time before CLK↑	S0 and S1	t_{su}			13	17	21	25	ns
	High-Level Inputs				10	13	17	20	
	High-Level Inputs				10	13	17	20	
	$\overline{CLR}$ Inactive				10	13	17	20	
Minimum Hold Time after CLK↑	S0 and S1	t_h			5	7	8	10	ns
	All Inputs				−3	0	0	0	
Maximum Input Capacitance		C_{IN}				5			pF
Maximum Output Capacitance		C_{OUT}	Output Disabled			10			pF
Power Dissipation Capacitance*		C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

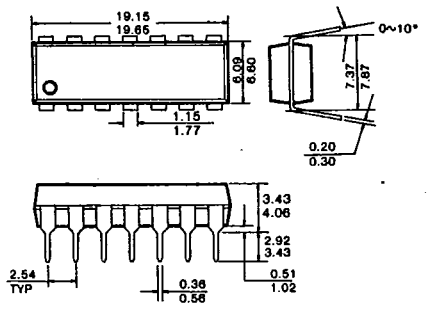
† For AC switching test circuits and timing waveforms see section 2.

PACKAGE DIMENSIONS

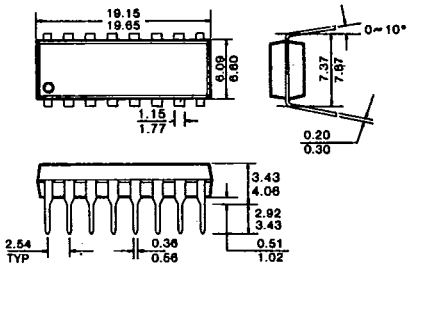
T-90-20

1. PLASTIC PACKAGES

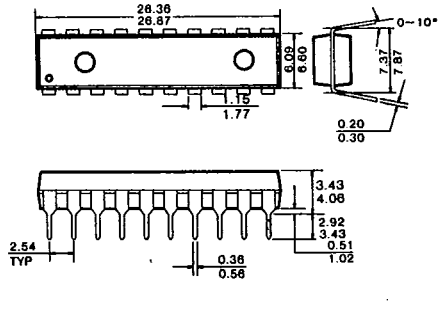
14-Pin Plastic DIP **Units: mm**



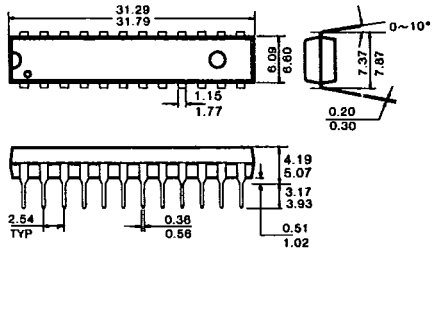
16-Pin Plastic DIP **Units: mm**



20-Pin Plastic DIP **Units: mm**



24-Pin Plastic DIP **Units: mm**



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PACKAGE DIMENSIONS

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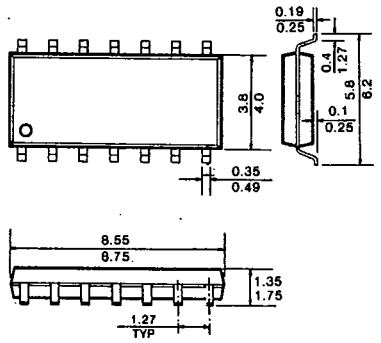
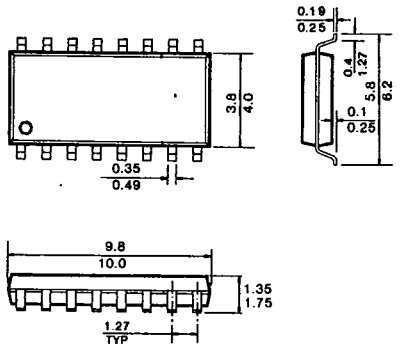
14-Pin SOP

Unit: mm



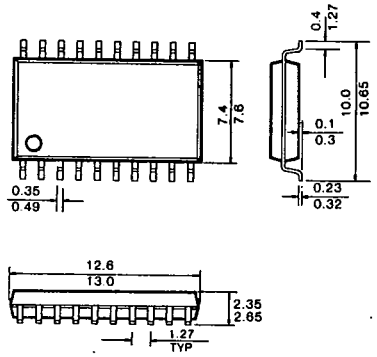
16-Pin SOP

Unit: mm



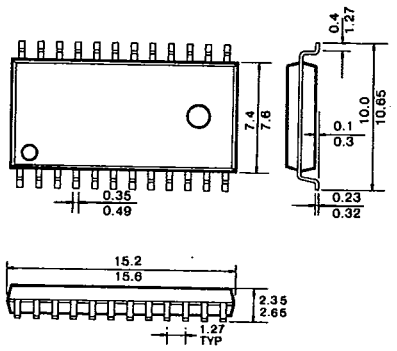
20-Pin SOP

Unit: mm



24-Pin SOP

Unit: mm

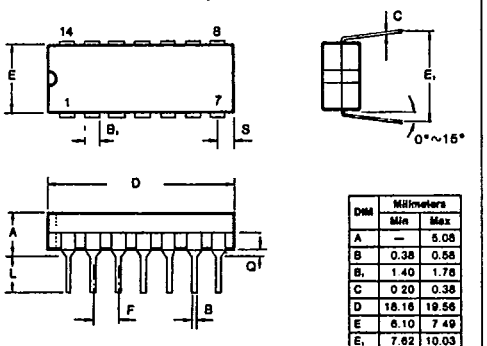


PACKAGE DIMENSIONS

T-90-20

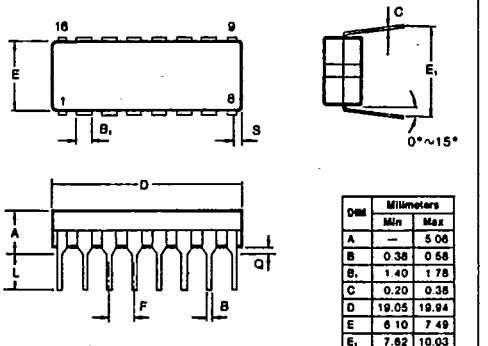
2. CERAMIC PACKAGES

14-Pin Ceramic DIP Units: mm



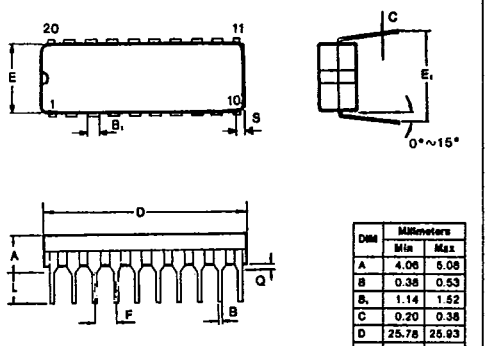
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B1	1.40	1.78
C	0.20	0.38
D	18.16	19.56
E	6.10	7.49
E1	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	1.91	2.29

16-Pin Ceramic DIP Units: mm



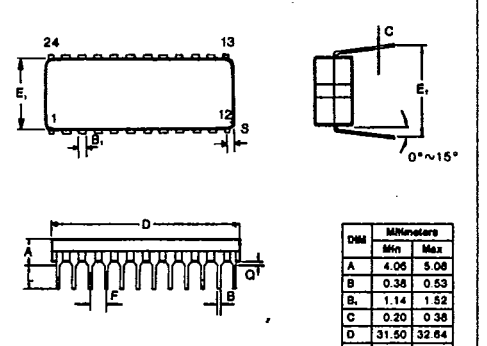
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B1	1.40	1.78
C	0.20	0.38
D	19.05	19.94
E	6.10	7.49
E1	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	0.51	1.14

20-Pin Ceramic DIP Units: mm



DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B1	1.14	1.52
C	0.20	0.38
D	25.78	25.93
E	6.10	6.60
E1	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.38	0.89
S	0.51	1.14

24-Pin Ceramic DIP Units: mm



DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B1	1.14	1.52
C	0.20	0.38
D	31.50	32.64
E	7.24	7.75
E1	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.508	1.778
S	1.65	1.93

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