HN624116L Series — Preliminary

16M (1M x16-bit) and (2M x 8-bit) Mask ROM

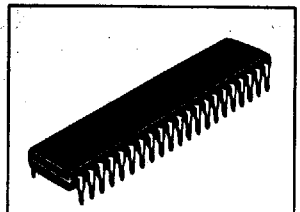
T-46-13-15

■ DESCRIPTION

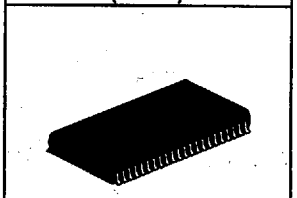
The Hitachi HN624116L is a 16-Megabit CMOS Mask Programmable Read Only Memory organized as 1,048,576 x 16-bit and 2,097,152 x 8-bit.

The HN624116L is capable of operating down to 3.0V, which makes it ideal for battery powered, portable systems. In addition, the high density provides enough capacity to be used as a character generator in laser printers.

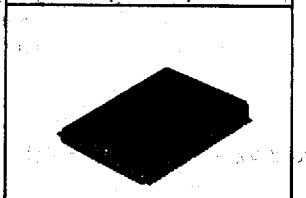
Hitachi's HN624116L is offered with JEDEC-Standard pinouts in 42-pin Plastic DIP and 44-lead Plastic SOP packages. The HN624116L is also packaged in a 48-lead Plastic SOP.



(DP-42)



(FP-44D)



(FP-48DA)

■ FEATURES

- Single Power Supply:
  V_{CC} = 3.0V to 5.5V (HN624116-30L)
  V_{CC} = 3.5V to 5.5V (HN624116-25L)
- Fast Access Times:
  250 ns/300 ns (max)
- Low Power Consumption:
  Active Current: 275 mW (typ)
  Standby Current: 5 µW (typ)
- User Selectable Organization:
  1M x 16-bit (Word-Wide)
  2M x 8-bit (Byte-Wide)
  Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
  JEDEC Standard Word-Wide/Byte-Wide Pinout
- Packages:
  42-pin Plastic DIP
  44-lead Plastic SOP
  48-lead Plastic SOP

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN624116P-25L	250 ns	42-pin Plastic DIP
HN624116P-30L	300 ns	(DP-42)
HN624116FB-25L	250 ns	44-lead Plastic SOP
HN624116FB-30L	300 ns	(FP-44D)
HN624116F-25L	250 ns	48-lead Plastic SOP
HN624116F-30L	300 ns	(FP-48DA)

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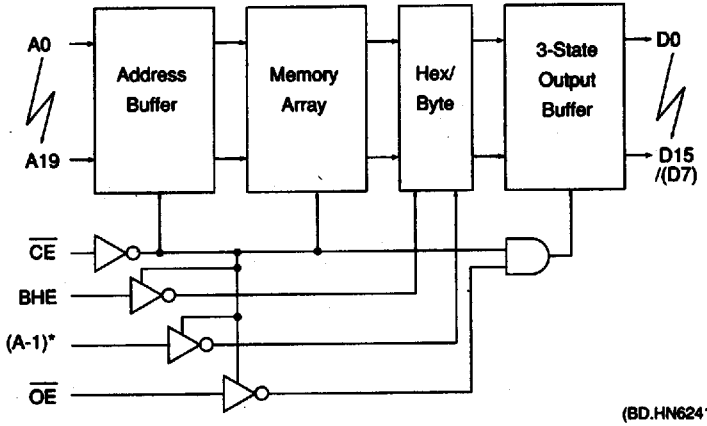
■ BLOCK DIAGRAM



(BD.HN624116L)

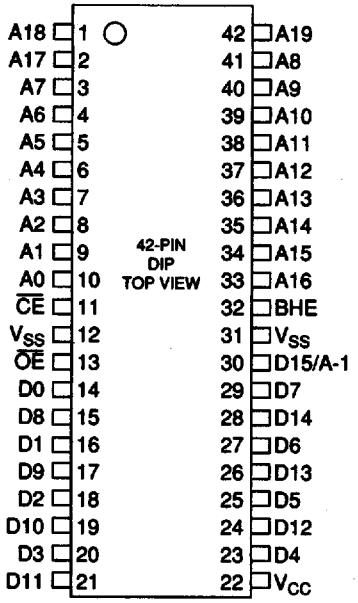
Notes: 1. * : A_{-1} is the Least Significant Address bit in Byte-Wide Mode.
2. BHE=V_{IH} : 16-bit (D_{15} - D_0)
BHE=V_{IL} : 8-bit (D_7 - D_0)
When BHE is low, D_{14} - D_8 are in high impedance states.

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{19}	Address
A_{-1}	Address (Word-Wide)
D_0 - D_{15}	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
BHE	Byte Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

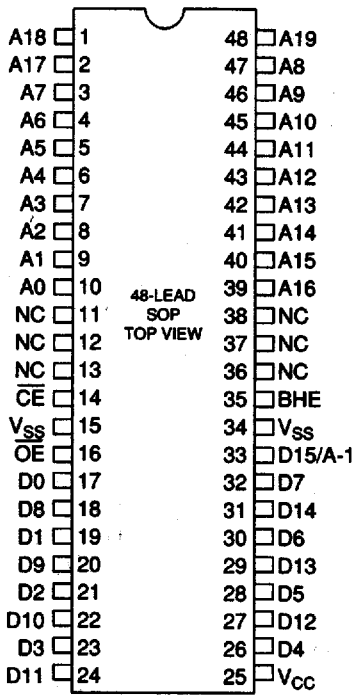
PIN ARRANGEMENT

HN624116P



(PinD42.HN624116L)

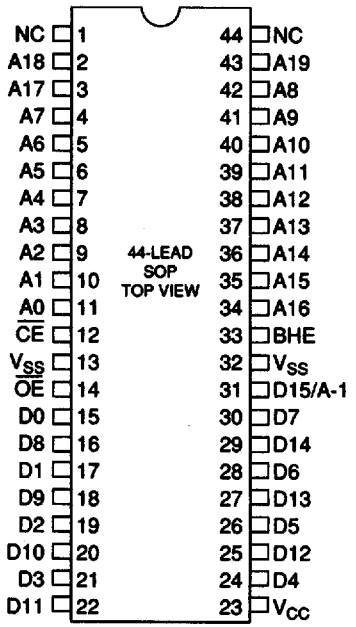
HN624116F



12-13 pin and 36-37 pin are connected to inner lead frame.

(PinT248.HN624116L)

HN624116FB



(PinT244.HN624116L)

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■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage [1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Note: 1. Relative to V_{SS}.

■ CAPACITANCE

(V_{CC} = 3.5/3.0 to 5.5V, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0V, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit
Input Capacitance [1]	C_{IN}	-	-	15	pF
Output Capacitance [1]	C_{OUT}	-	-	15	pF

Note: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 3.5/3.0 to 5.5V, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	-	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	-	65	mA	V_{CC} = 5.5 V, ID_{OUT} = 0 mA, t_{RC}=min.
				35	mA	V_{CC} = 3.5 V, ID_{OUT} = 0 mA, t_{RC}=Min.
Standby V_{CC} Current	I_{SB}	-	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ -0.2V
Input Voltage	V_{IH}	2.2	-	V_{CC}+0.3	V	
	V_{IL}	-0.3	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -205 µA
	V_{OL}	-	-	0.4	V	I_{OL} = 1.6 mA

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AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{SS} = 0V, T_a = 0 to +70°C)

Test Conditions

- Input pulse levels: 0.8 / 2.4V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

Item	Symbol	V_{CC} =3.5 to 5.5V HN624116-25L		V_{CC} =3.0 to 5.5V HN624116-30L		Test Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	250	-	300		ns
Address Access Time	t_{AA}	-	250	-	300	ns
Chip Enable Access Time	t_{ACE}	-	250	-	300	ns
Output Enable Access Time	t_{OE}	-	100	-	150	ns
BHE Access Time	t_{BHE}	-	250	-	300	ns
Output Hold Time from Address Change	t_{DHA}	0	-	0	-	ns
Output Hold Time from Chip Enable	t_{DHC}	0	-	0	-	ns
Output Hold Time from Output Enable	t_{DHO}	0	-	0	-	ns
Output Hold Time from BHE	t_{DHB}	0	-	0	-	ns
Chip Enable to Output in High-Z [1]	t_{CHZ}	-	100	-	100	ns
Output Enable to Output in High-Z [1]	t_{OHZ}	-	100	-	100	ns
BHE to Output in High-Z [1]	t_{BHZ}	-	100	-	100	ns
Chip Enable to Output in Low-Z	t_{CLZ}	10	-	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}	10	-	10	-	ns
BHE to Output in Low-Z	t_{BLZ}	10	-	10	-	ns

Note: 1. t_{CHZ}, t_{OHZ}, and t_{BHZ} are defined as the time at which the output becomes an open circuit and are not referenced to output voltage levels.

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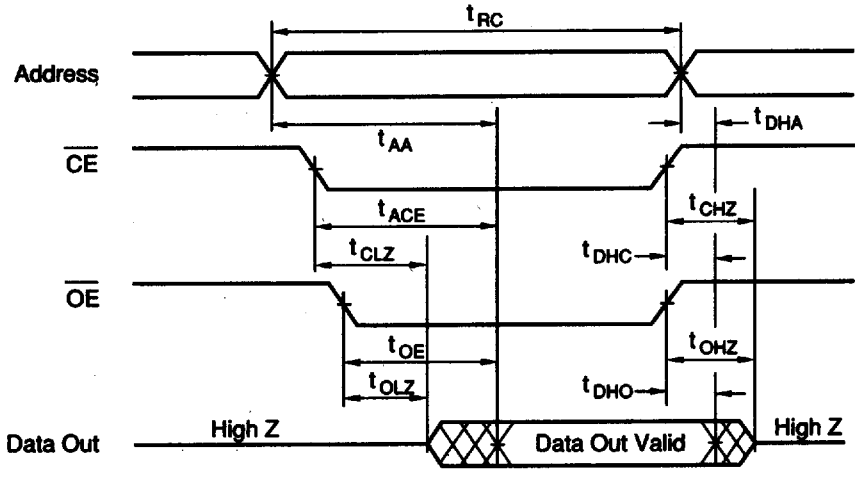
READ TIMING WAVEFORM

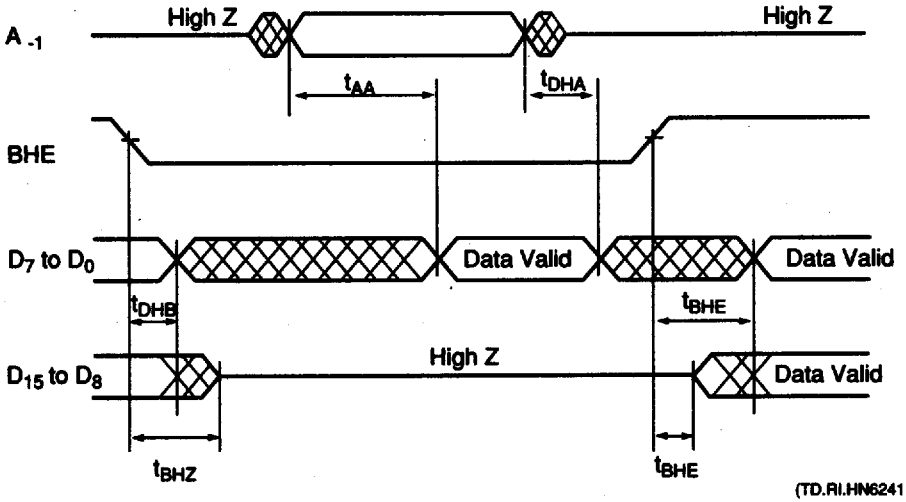
Word Mode (BHE = V_{IH}) or Byte Mode (BHE = V_{IL})



(TD.R.HN624116L)

Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

Word Mode/ Byte Mode Switch



(TD.RI.HN624116L)

Note: 1. If $\overline{CE}$ and $\overline{OE}$ are enabled, A_{19} to A_0 are valid.
2. D_{15}/A_{-1} pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enabled. Therefore, the input signals of opposite phase to the output must not be applied to them.