Contents

The S-4630A is a CMOS thermal print head driver containing a 64-bit shift register and a latch. It can be easily used for general purpose because “H” or “L” can be selected for the driver enable and the latch is fixed to “L”. It is ideal for the thermal print head of 200 dpi or 8 dots/mm because of its driver output pad pitch of 110 μm.

■ Features

- Low current consumption : 0.4 mA typ.
  (f_{CLK}=5 MHz, SI : fixed)
- High speed operation : 7 MHz (chip)
  5 MHz (cascade connection)
- Driver output voltage : 36 V max.
- Driver output current : 9 mA max.
- 64-bit shift register and latch are built in
- Driver enable
- Driver-off function when supply voltage falls

■ Block Diagram

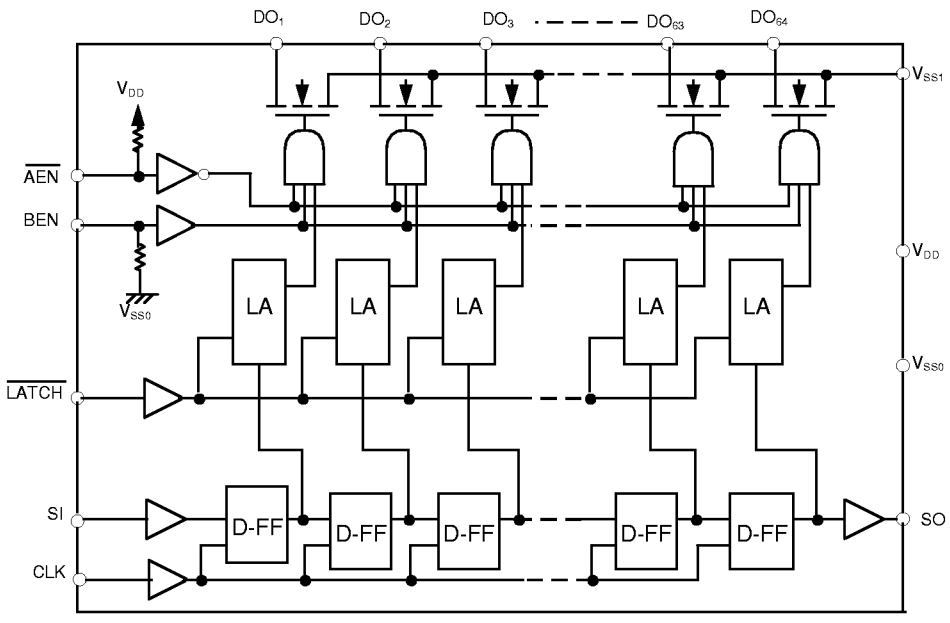

Figure 1

■ Operation

The 64-bit shift register reads the data input to SI on the rising edge of the CLOCK input.

The latch circuit reads the data of the shift register when it is "L" level, and it holds the preceding data when it is "H" level.

The latch data are output to the respective drivers when $\overline{AEN}$ is low and BEN is high. The driver output transistor turns on when the latch data are high and turns off when low. Turning $\overline{AEN}$ high or BEN low makes all driver output transistors go off.

All driver output transistors go off when power supply voltage becomes lower than V_{DET} regardless of all input signals.

■ Terminal Functions (Refer to the dimensions for the pad arrangement)

Table 1

No.	Name	Functions
1 to 64	DO_1 to DO_{64} (DO_n)	Driver output terminals (Nch open-drain)
65, 66, 71, 72, 79, 80	V_{SS1}	GND for driver (0 V)
68, 75	V_{DD}	Positive power supply for logic (+5 V)
70, 73	V_{SS0}	GND for logic (0 V)
76	CLK	Clock input terminal for 64-bit shift register
78	SI	Serial data input terminal for 64-bit shift register
67	SO	Serial data output terminal for 64-bit shift register
77	$\overline{LATCH}$	Data latch signal input terminal $\overline{LATCH}$="L": reads the data of the shift register $\overline{LATCH}$= "H": holds the preceding data
74	$\overline{AEN}$	Driver enable terminal : outputs the latch data to the driver when low(pull-up resistor is built in)
69	BEN	Driver enable terminal : outputs the latch data to the driver when high(pull-down resistor is built in)

■ Absolute Maximum Ratings

Table 2

Parameter	Symbol	Ratings	Unit
Supply voltage	$V_{SS0,1}$ - V_{DD}	-0.4 to +7.0	V
Driver output voltage	V_{DOH}	36	V
Driver output current	I_{DOL}	15	mA
Input voltage	V_{IN}	V_{SS0}-0.5 to V_{DD}+0.5	V
Output voltage	V_{OUT}	V_{SS0}-0.5 to V_{DD}+0.5	V
Max. junction temperature	T_{jMAX}	125	°C
Operating temperature	T_{opr}	-10 to +80	°C
Storage temperature	T_{stg}	-40 to +125	°C

■ DC Electrical Characteristics

Table 3
(Unless otherwise specified : V_{DD}=5.0 V±10%, Ta=-10°C to 80°C)

Parameter	Sybl	Conditions		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}			4.5	5.0	5.5	V
High level input voltage	V_{IH}			0.7×V_{DD}	—	V_{DD}	V
Low level input voltage	V_{IL}			V_{SS}	—	0.3×V_{DD}	V
High level input current	I_{IH}	V_{DD}=5.0 V V_{IH}=5.0 V Ta=25°C	BEN	—	—	35	µA
				—	—	0.5	µA
Low level input current	I_{IL}	V_{DD}=5.0 V V_{IL}=0 V Ta=25°C	$\overline{AEN}$	-35	—	—	µA
				-0.5	—	—	µA
High level output voltage	V_{OH}	SO terminal, no load		4.45	—	—	V
Low level output voltage	V_{OL}	SO terminal, no load		—	—	0.05	V
High level output current	I_{OH}	SO terminal, V_{OH}=V_{DD}-0.4 V		—	—	-0.5	mA
Low level output current	I_{OL}	SO terminal, V_{OL}=0.4 V		0.5	—	—	mA
High level driver output voltage	V_{DOH}			—	24	26	V
Low level driver output voltage	V_{DOL}	I_{DOL}=9 mA, V_{DD}=5.0 V		—	0.7	1.5	V
Driver leakage current	I_{LEAK}	V_{DOH}=26 V Per 1-bit of driver output		—	—	1.0	µA
Current consumption	I_{DD}	Ta= 25 C	f_{CLK} =2 MHz,SI : fixed	—	0.2	0.6	mA
			f_{CLK} =5 MHz,SI : fixed	—	0.4	1.2	mA
			f_{CLK} =5 MHz, SI=1/2f_{CLK}	—	1.6	5.0	mA
Lower V_{DD} detection voltage	V_{DET}			2.0	—	4.0	V

■ AC Electrical Characteristics

Table 4
(V_{DD}= 5.0 V±10%, Ta=-10°C to 80°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CLK pulse width	t_{WCLK}		70	—	—	ns
Data setup time	t_{SUD}	V_{IH}=V_{DD}, V_{IL}=V_{SS0}	40	—	—	ns
Data hold time	t_{HD}	V_{IH}=V_{DD}, V_{IL}=V_{SS0}	40	—	—	ns
Latch pulse width	t_{WLA}		100	—	—	ns
Latch setup time	t_{SULA}		100	—	—	ns
CLK-SO propagation delay time	t_{dSO}	C_L=3 pF	—	—	120	ns
EN-DOn propagation delay time	t_{dDO}	R_L=3.0 kΩ, V_{DOH}=24 V	—	—	3.0	µs
DOn rise time	t_{rDO}	R_L=3.0 kΩ, V_{DOH}=24 V	—	1.0	3.0	µs
DOn fall time	t_{fDO}	R_L=3.0 kΩ, V_{DOH}=24 V	—	1.0	3.0	µs
Clock frequency	f_{CLK}	When cascade connection	—	—	5.0	MHz

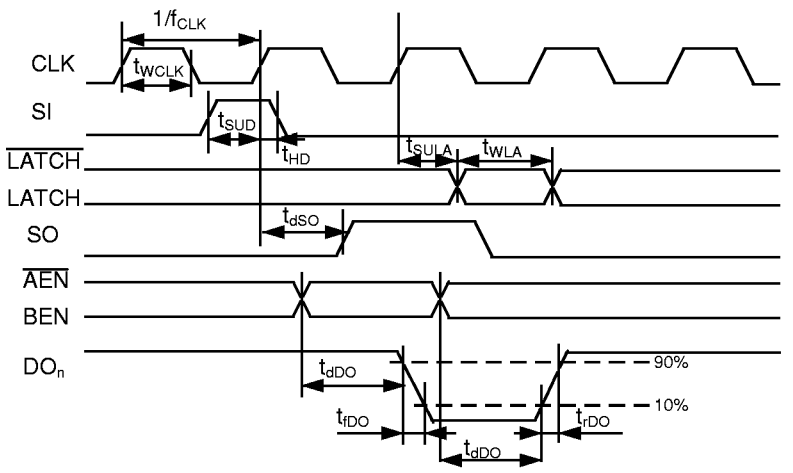

Figure 2