54F/74F418

32-Bit Memory Error Detection And Correction Circuit

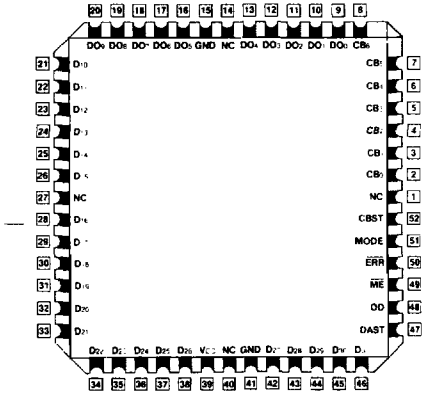
Description

The 'F418 Memory Error Detection And Correction (EDAC) circuit contains the logic to generate seven check bits on a 32-bit data field, according to a modified Hamming code. The check bits are then stored in memory with the data word. On a subsequent read from memory, the device will detect and correct any single-bit data error, and detect any double-bit error.

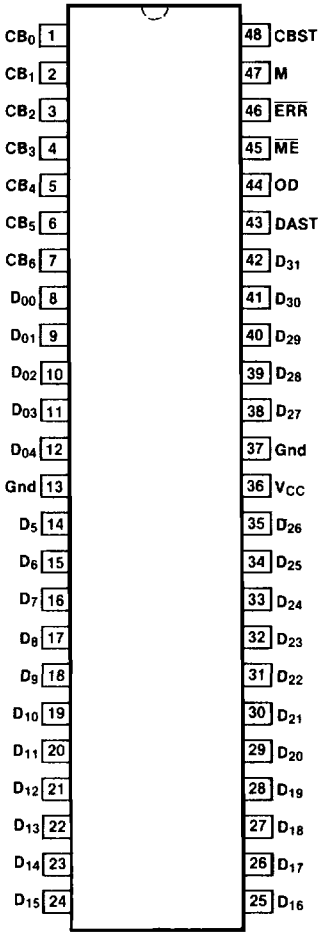
The 'F418 is fully compatible with all TTL families. Data and check bit signals are bidirectional 3-state lines.

- **Increases Memory System Reliability**
- **Corrects Single-Bit Errors in 60 ns**
- **Detects Double-Bit Errors in 85 ns**

Connection Diagrams



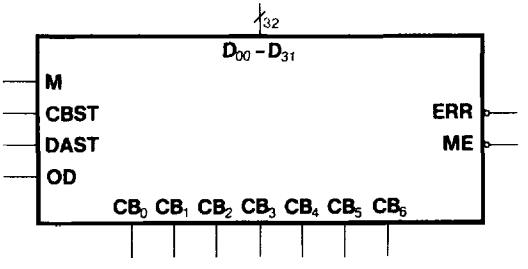
Pin Assignment for LCC and PCC



Pin Assignment for DIP

Ordering Code: See Section 5

Logic Symbol



Input Loading/Fan-Out: See Section 3 for U.L. definitions

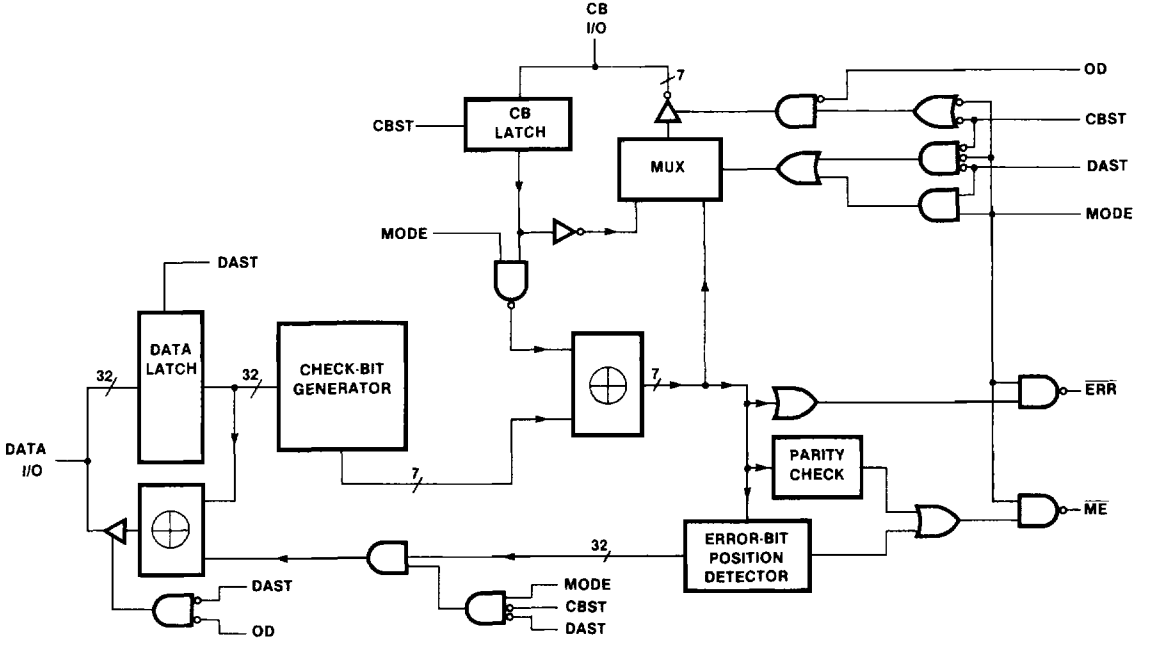
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_{31}	Data Input/ Output Lines	0.5/0.375 75/15 (12.5)
CB_0-CB_6	Check Bit Input/ Output Lines	0.5/0.375 75/15 (12.5)
DAST	Data Strobe	0.5/0.375
OD	Output Disable	0.5/0.375
$\overline{ME}$	Multiple Error	25/12.5
$\overline{ERR}$	Error	25/12.5
MODE	Mode	0.5/0.375
CBST	Check Bit Strobe	0.5/0.375

Functional Description

During generate mode, MODE is LOW, CB_2 through CB_5 are calculated so that the indicated bits are an even number of ones (i.e. even parity) while CB_0, CB_1, and CB_6 are calculated for an odd number of ones. This modification of the Hamming code makes the device respond to a memory read of all ones or all zeroes (all 39 bits) with an $\overline{ME}$ indication.

During correction mode, with DAST LOW and CBST LOW, the fail pattern will be placed on the CB I/O lines. Each zero in the fail pattern indicates a discrepancy between that particular bit in the input (latched) checkbit (based on D_0 through D_{31}). A fail pattern of all ones indicates no error. A single zero indicates that the corresponding bit is in error and no correction of the data is required. This situation is still flagged with a LOW $\overline{ERR}$.

Block Diagram



Function Table

Control Inputs			Outputs			Function
DAST	MODE	CBST	DATA I/O*	CB I/O*	$\overline{ERR}$, $\overline{ME}$	
0	0	0	O/P Latched Data	O/P Latched CB's	1	Read Latches
0	0	1	O/P	O/P New CB's	1	Latched, Generate CB's
0	1	0	O/P Corrected Data	O/P Syndromes	Active	Correct
0	1	1	O/P Uncorrected Data	O/P Latched CB's	Active	Monitor w/Latched Data
1	0	X	I/P	O/P New CB's	1	Unlatched Data, Generate CB's
1	1	0	I/P	O/P Latched CB's	Active	Monitor w/Latched CB's
1	1	1	I/P	I/P	Active	Monitor Inputs

*OD must be LOW to enable the output drivers

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DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current			400	mA	V_{CC} = Max, OD = 4.5 V

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F	54F	74F	Units
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$	T_A, V_{CC} = Mil $C_L = 50\ pF$	T_A, V_{CC} = Com $C_L = 50\ pF$	
		Min Typ Max	Min Max	Min Max	
t_{PLH} t_{PHL}	Propagation Delay Data to CB	63.0 63.0			ns
t_{PLH} t_{PHL}	Propagation Delay Data or Check Bit to $\overline{ERR}$	55.0 55.0			ns
t_{PLH} t_{PHL}	Propagation Delay Data or Check Bit to $\overline{ME}$	75.0 75.0			ns
t_{PLH} t_{PHL}	Propagation Delay MODE to $\overline{ERR}$	23.0 23.0			ns
t_{PLH} t_{PHL}	Propagation Delay MODE to $\overline{ME}$	24.0 24.0			ns
t_{PLH} t_{PHL}	Propagation Delay MODE to Corrected Data	52.0 52.0			ns
t_{PLH} t_{PHL}	Propagation Delay MODE to Syndromes	35.0 35.0			ns
t_{PLH} t_{PHL}	Propagation Delay DAST+ to $\overline{ERR}$	68.0 68.0			ns
t_{PLH} t_{PHL}	Propagation Delay DAST+ to $\overline{ME}$	86.0 86.0			ns
t_{PLH} t_{PHL}	Propagation Delay CBST+ to $\overline{ERR}$	43.0 43.0			ns
t_{PLH} t_{PHL}	Propagation Delay CBST+ to $\overline{ME}$	50.0 50.0			ns
t_{PLH} t_{PHL}	Propagation Delay DAST+ to Corrected Data	84.0 84.0			ns
t_{PLH} t_{PHL}	Propagation Delay CBST+ to Syndromes	70.0 70.0			ns
t_{PHZ} t_{PLZ}	Enable Times	22.0 22.0			ns
t_{PZH} t_{PZL}	Disable Times	24.0 24.0			ns

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com	
		Min Typ Max	Min Max	Min Max	
$t_s(H)$	Setup Time, HIGH Data to DAST-	11.0			ns
$t_h(H)$	Hold Time, HIGH DAST- to Data	9.0			
$t_s(L)$	Setup Time, LOW Check Bits to CBST+	7.0			ns
$t_h(L)$	Hold Time, LOW CBST- to Check Bits	7.0			
$t_w(H)$	DAST Pulse Width	26.0			ns
$t_w(H)$	CBST Pulse Width	15.0			ns

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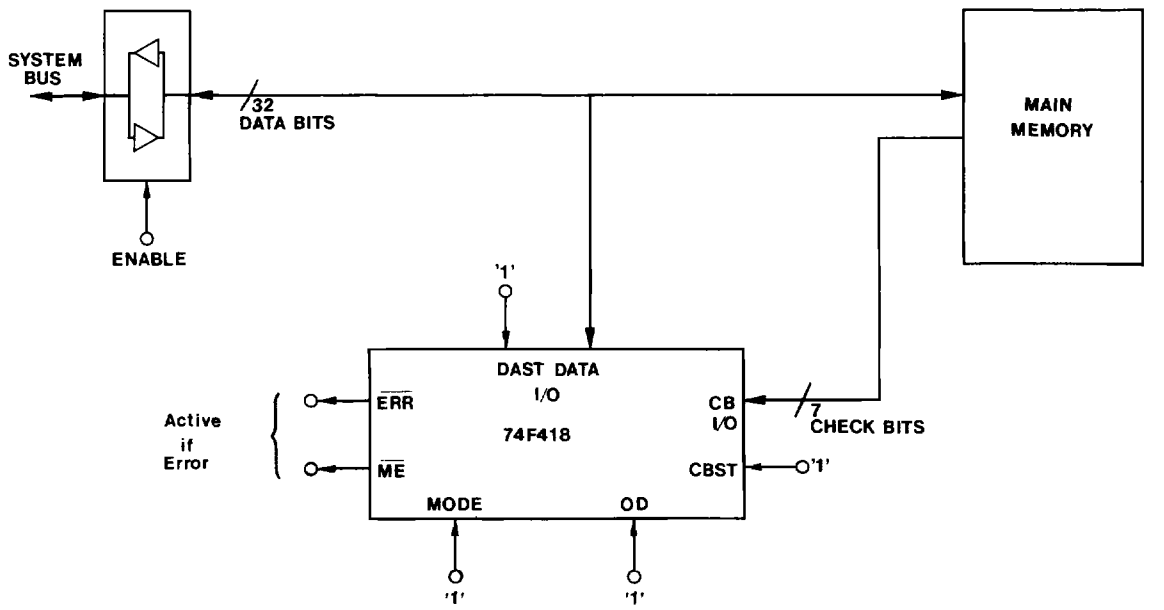
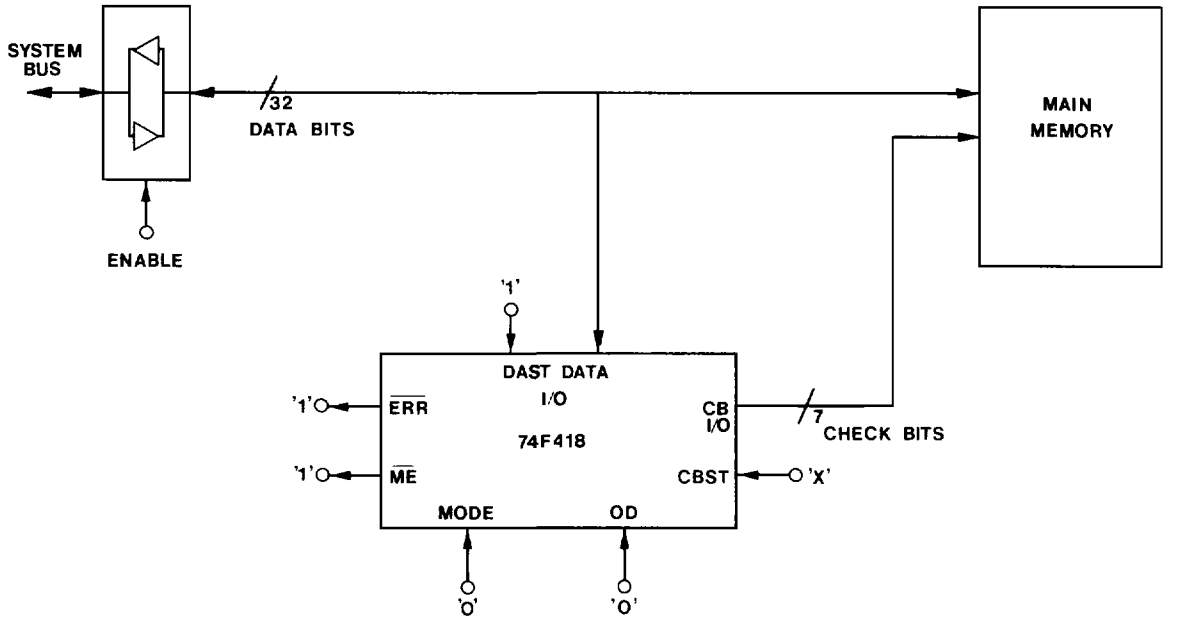
Memory Read Operation
Check for Error



Memory Write Operation



Single-Bit Error Correction