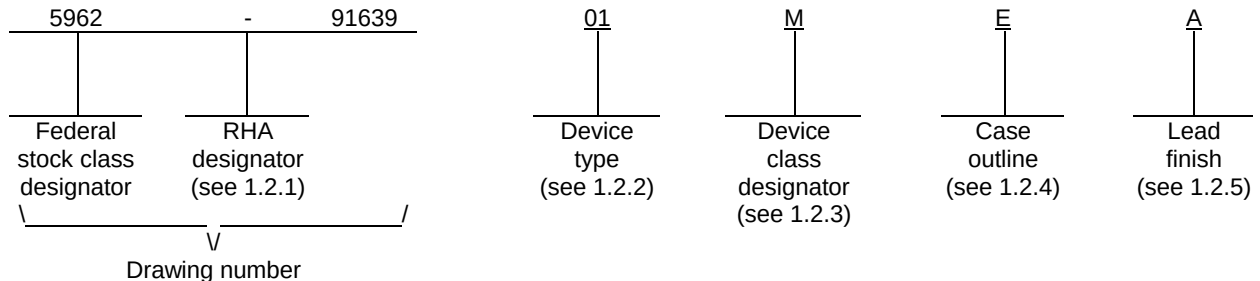


REVISIONS																			
LTR	DESCRIPTION										DATE (YR-MO-DA)				APPROVED				
A	Add vendor CAGE 01295. Make change to VIN and PD as specified under paragraph 1.3. Make change to VOH, ICC, IOZ, ISC, skew, tPHZ, and tPLZ tests as specified in table I. Changes in accordance with N.O.R. 5962-R109-95.										95-04-14				M. A. Frye				
B	Add case X which is a 16 lead flat pack. Make changes to 1.2.4, 1.3, 1.4, 3.2.1, and figure 1. Redrawn. ro										98-02-20				Raymond Monnin				
C	Update drawing to current requirements. Editorial changes throughout. - drw										05-01-24				Raymond Monnin				
THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.																			
REV																			
SHEET																			
REV																			
SHEET																			
REV STATUS					REV		C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS					SHEET		1	2	3	4	5	6	7	8	9	10	11	12	14
PMIC N/A					PREPARED BY					DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990 http://www.dscc.dla.mil									
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A					CHECKED BY														
					APPROVED BY														
					DRAWING APPROVAL DATE														
					91-09-16														
					REVISION LEVEL					SIZE	CAGE CODE	5962-91639							
					C					A	67268								
										SHEET 1 OF 14									

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identifies the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	26C31	CMOS quad differential line driver

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDIP2-F16 or CDIP3-F16	16	Flat pack
X	See figure 1	16	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

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1.3 Absolute maximum ratings. ^{1/}

Supply voltage range (V_{CC})	-0.5 V dc to 7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to $V_{CC} + 0.5$ V dc
DC output voltage range (V_{OUT})	-0.5 V dc to 7.0 V dc
DC output current, per pin (I_{OUT})	± 150 mA
Input, output clamp diode current (I_{IK}, I_{OK})	± 20 mA
DC V_{CC} or GND current, per pin (I_{CC})	± 150 mA
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 4 seconds)	260°C
Junction temperature (T_J)	150°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases E, F, 2	See MIL-STD-1835
Case X	11°C/W
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case E	+100°C/W
Case F	+150°C/W
Case X	+116°C/W
Case 2	+85°C/W
Power dissipation (P_D): ($T_A = +25^\circ\text{C}$)	
Case E	1375 mW
Case F	1000 mW
Case X	1293 mW
Case 2	1375 mW

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
DC input or output voltage range (V_{IN}, V_{OUT})	0 V dc to V_{CC}
Ambient operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

^{1/} Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 77 (see MIL-PRF-38535, appendix A).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C -4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Logical 1 input voltage	V _{IH}		1,2,3	01	2.0		V
Logical 0 input voltage	V _{IL}		1,2,3	01		0.8	V
Logical 1 output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL} , I _{CC} = 4.5 V, I _{OUT} = -20 mA	1	01	2.4		V
			2,3		2.2		
Logical 0 output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL} , V _{CC} = 4.5 V, I _{OUT} = 20 mA	1,2,3	01		0.5	V
Differential output voltage	V _T	V _{CC} = 4.5 V, R _L = 100 Ω <u>1/</u>	1,2,3	01	2.0		V
Difference in differential output	$\frac{ V_T - \bar{V}_T }{ V_T }$	V _{CC} = 4.5 V, R _L = 100 Ω <u>1/</u>	1,2,3	01		0.4	V
Common mode output voltage	V _{OS}	V _{CC} = 5.5 V, R _L = 100 Ω <u>1/</u>	1,2,3	01		3.0	V
Difference in common mode output	$\frac{ V_{OS} - \bar{V}_{OS} }{V_{OS}}$	V _{CC} = 5.5 V, R _L = 100 Ω <u>1/</u>	1,2,3	01		0.4	V
Input current	I _{IN}	V _{IN} = V _{CC} , GND, V _{IH} , or V _{IL} , V _{CC} = 5.5 V	1,2,3	01	-1.0	+1.0	μA
Quiescent power supply current	I _{CC}	I _{OUT} = 0 μA, V _{CC} = 4.5 V, V _{IN} = 5 V or GND <u>2/</u>	1,2,3	01		500	μA
		I _{OUT} = 0 μA, V _{CC} = 5.5 V, V _{IN} = 2.4 V or 0.5 V <u>2/</u>	1			3.0	mA
			2,3			3.2	
TRI-STATE output leakage current	I _{OZ}	V _{OUT} = 2.5 V or 0.5 V, ENABLE = V _{IL} , V _{CC} = 5.5 V, ENABLE = V _{IH}	1,2,3	01	-20	+20	μA
Output short circuit current	I _{SC}	V _{IN} = V _{CC} or GND, V _{CC} = 5.5 V <u>1/</u> , <u>3/</u>	1	01	-150	-30	mA
			2,3		-170	-30	
Output leakage current "power off"	I _{OFF}	V _{CC} = 0 V, V _{OUT} = 6 V	1,2,3	01		100	μA
		V _{CC} = 0 V, V _{OUT} = 0 V			-100		
Functional tests to output		See 4.4.1b	7,8	01			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C -4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay input to output	t _{PLH}	S1 open <u>4/</u>	9,10,11	01		14	ns
	t _{PHL}					14	
Skew		S1 open <u>4/</u> <u>5/</u>	9,10,11	01		4	ns
Output rise time	t _{TLH}	S1 open <u>4/</u>	9,10,11	01		14	ns
Output fall time	t _{THL}	S1 open <u>4/</u>	9,10,11	01		14	ns
Output enable time	t _{PZH}	S1 closed <u>4/</u>	9,10,11	01		22	ns
	t _{PZL}					28	
Output disable time	t _{PHZ}	S1 closed <u>4/</u> <u>6/</u>	9,10,11	01		16	ns
	t _{PLZ}					16	

1/ See EIA specification RS-422 for exact test conditions.

2/ Measure per input. All other inputs at 5 V or GND.

3/ This is a current forced when a high output is shorted to GND. Only one output shall be shorted at a time.

4/ See figures 5 and 6. Rise time (t_r) ≤ 6 ns and fall time (t_f) ≤ 6 ns. V_{CC} = 5.0 V.

5/ Skew is defined as the difference in propagation delay between complementary output at 50 % point.

6/ Output disable time is the delay from ENABLE or $\overline{\text{ENABLE}}$ being switched to the output transistor turning off.

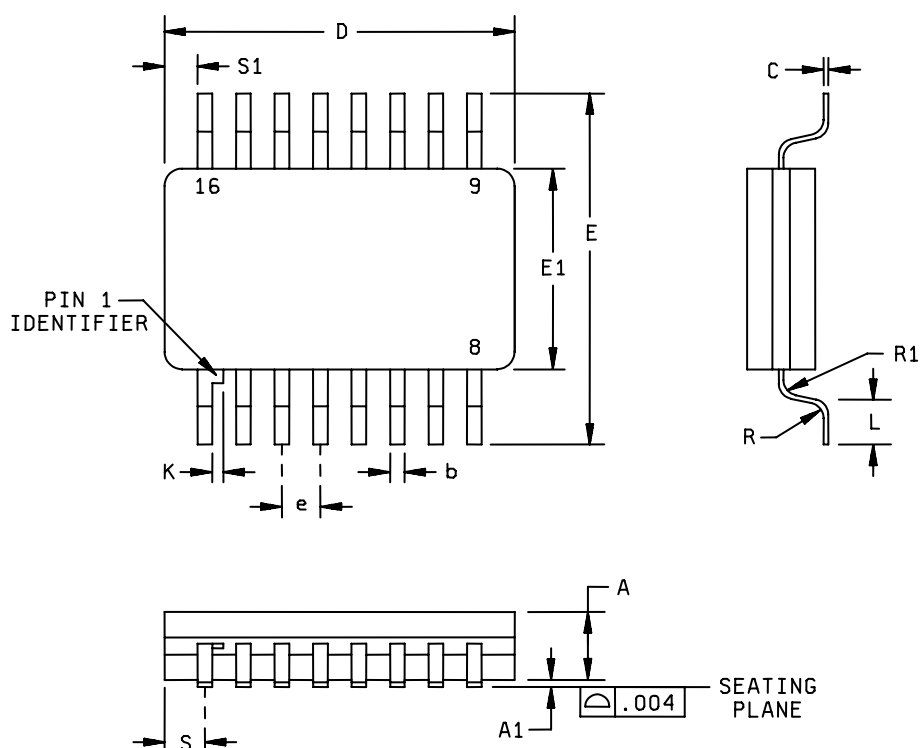
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Ltr	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.050	.080	1.27	2.03	
A1	.004	.012	0.10	0.30	
b	.015	.019	0.38	0.48	2
C	.004	.008	0.10	0.20	2
D	---	.390	---	9.91	
E	.400	.420	10.16	10.67	
E1	.245	.270	6.22	6.86	
e	.050 BSC		1.27 BSC		
K	.008	.012	0.20	0.30	
L	.037	.043	0.94	1.09	
R	.013	.017	0.33	0.43	
R1	.013	.017	0.33	0.43	
S	---	.018	---	0.46	
S1	.005	---	0.13	---	

NOTES:

1. The U.S. government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
2. Maximum limits may be increased by .003 inches after lead finish is applied.

FIGURE 1. Case outline X.

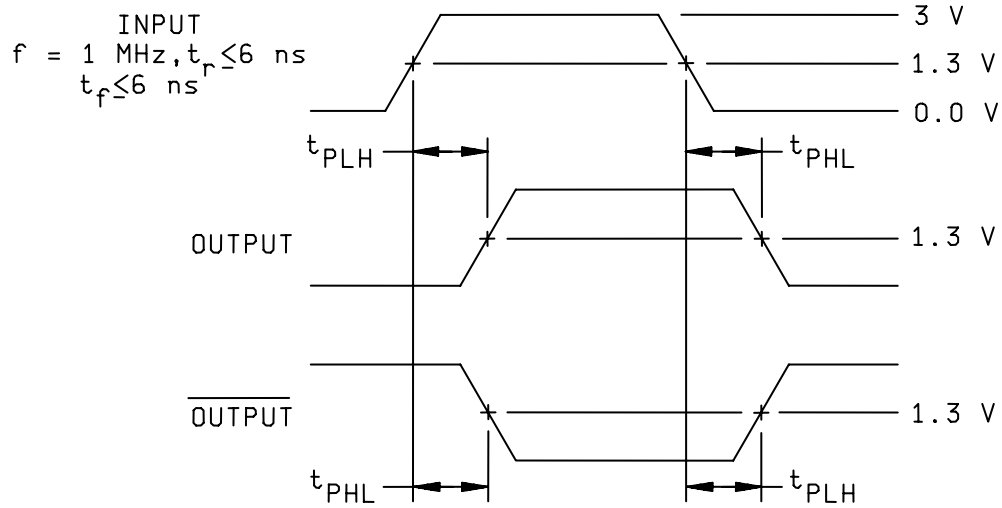
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Device type	01	
Case outlines	E, F, and X	2
Terminal number	Terminal symbol	
1	INPUT A	NC
2	CHANNEL A2 OUTPUT	INPUT A
3	CHANNEL A1 OUTPUT	CHANNEL A2 OUTPUT
4	ENABLE	CHANNEL A1 OUTPUT
5	CHANNEL B1 OUTPUT	ENABLE
6	CHANNEL B2 OUTPUT	NC
7	INPUT B	CHANNEL B1 OUTPUT
8	GND	CHANNEL B2 OUTPUT
9	INPUT C	INPUT B
10	CHANNEL C2 OUTPUT	GND
11	CHANNEL C1 OUTPUT	NC
12	$\overline{\text{ENABLE}}$	INPUT C
13	CHANNEL D1 OUTPUT	CHANNEL C2 OUTPUT
14	CHANNEL D2 OUTPUT	CHANNEL C1 OUTPUT
15	INPUT D	$\overline{\text{ENABLE}}$
16	V _{CC}	NC
17	---	CHANNEL D1 OUTPUT
18	---	CHANNEL D2 OUTPUT
19	---	INPUT D
20	---	V _{CC}

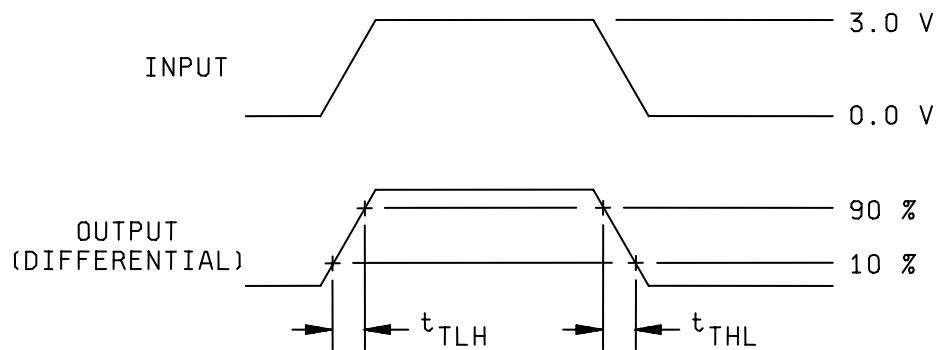
NC = No connection

FIGURE 2. Terminal connections.

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PROPAGATION DELAYS



INPUT PULSE: $f = 1 \text{ MHz}$, DUTY CYCLE $\leq 50\%$; $t_r = t_f \leq 6 \text{ ns}$

DIFFERENTIAL RISE AND FALL TIMES

FIGURE 5. Timing waveforms.

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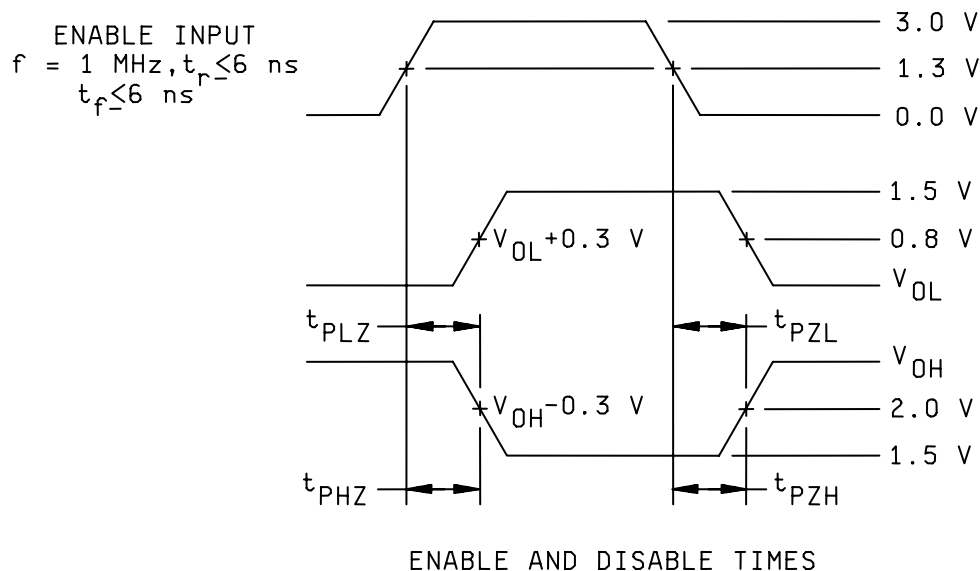
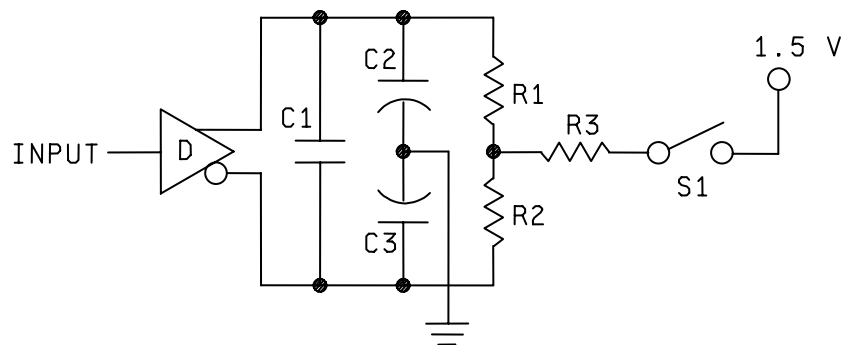


FIGURE 5. Timing waveforms - continued.



NOTE: $C1 = C2 = C3 = 40 \text{ pF}$, $R1 = R2 = 50\Omega$, $R3 = 500\Omega$

FIGURE 6. AC test circuit.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) $T_A = +125^{\circ}\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

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TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	---	1
Final electrical parameters (see 4.2)	1, 2, 3, 9 <u>1/</u>	1, 2, 3, 9 <u>1/</u>	1, 2, 3, 9 <u>1/</u>
Group A test requirements (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b. $T_A = +125^{\circ}\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table II herein.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-91639
		REVISION LEVEL C	SHEET 14

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 05-01-24

Approved sources of supply for SMD 5962-91639 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at <http://www.dscclia.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-9163901MEA	27014	DS26C31MJ/883
5962-9163901MFA	27014	DS26C31MW/883
5962-9163901MXA	27014	DS26C31MWG/883
5962-9163901M2A	27014	DS26C31ME/883
5962-9163901QEA	01295	AM26C31MJB
5962-9163901QFA	01295	AM26C31MWB
5962-9163901Q2A	01295	AM26C31MFK

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

Vendor name
and address

27014

National Semiconductor
2900 Semiconductor Dr
PO Box 58090
Santa Clara, CA 95052-8090

01295

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Ln.
PO Box 660199
Dallas, TX 75243

Point of contact:

U.S. Highway 75 South
P.O. Box 84, M/S 853
Sherman, TX 75090-9493

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.