



November 2000
Revised December 2000

FI1532

5V LVDS Quad High Speed Differential Receiver (Preliminary)

General Description

This quad receiver is designed for high speed interconnects utilizing Low Voltage Differential Signaling (LVDS) technology. The receiver translates LVDS levels, with a typical differential input threshold of 100 mV, to LVTTTL signal levels. LVDS provides low EMI at ultra low power dissipation even at high frequencies. This device is ideal for high speed transfer of clock and data.

The FI1532 can be paired with its companion driver, the FI1531, or any other Fairchild LVDS driver.

Features

- Greater than 400Mbps data rate
- 5V power supply operation
- 0.4ns maximum differential pulse skew
- 3ns maximum propagation delay
- Low power dissipation
- Power OFF protection
- Fail safe protection for open-circuit, shorted and terminated conditions
- Meets or exceeds the TIA/EIA-644 LVDS standard
- Pin compatible with equivalent RS-422 and PECL devices
- 16-Lead SOIC and TSSOP packages save space

Ordering Code:

Order Number	Package Number	Package Description
FI1532M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
FI1532MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

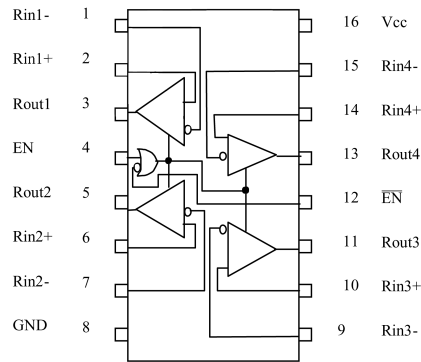
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Pin Descriptions

Pin Name	Description
Rout1, Rout2, Rout3, Rout4	LVTTTL Data Outputs
Rin1+, Rin2+, Rin3+, Rin4+	Non-inverting LVDS Inputs
Rin1-, Rin2-, Rin3-, Rin4-	Inverting LVDS Inputs
EN	Driver Enable Pin
$\overline{\text{EN}}$	Inverting Driver Enable Pin
V _{CC}	Power Supply
GND	Ground

Fail Safe = Open, Shorted, Terminated

Connection Diagram



Function Table

Input				Outputs
EN	$\overline{\text{EN}}$	Rin+	Rin-	Rout
H	X	H	L	H
H	X	L	H	L
H	X	Fail Safe Condition		H
X	L	H	L	H
X	L	L	H	L
X	L	Fail Safe Condition		H
L	H	X		Z

H = HIGH Logic Level
X = Don't Care

L = LOW Logic Level
Z = High Impedance

FI1532 5V LVDS Quad High Speed Differential Receiver (Preliminary)

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	-0.5V to +7V
DC Input Voltage (V_{IN})	-0.5V to +7V
DC Output Voltage (V_{OUT})	-0.5V to +7V
DC Output Current (I_O)	16 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C
Max Junction Temperature (T_J)	150°C
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C
ESD (Human Body Model)	≥ 8000V
ESD (Machine Model)	≥ 600V

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_{IN})	0 to V_{CC}
Magnitude of Differential Voltage ($ V_{ID} $)	100 mV to V_{CC}
Common-mode Input Voltage (V_{IC})	0.05V to 2.35V
Operating Temperature (T_A)	-40°C to +85°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. Fairchild does not recommend operation of circuits outside databook specification.

DC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ (Note 2)	Max	Units
V_{TH}	Differential Input Threshold HIGH	See Figure 1 and Table 1			100	mV
V_{TL}	Differential Input Threshold LOW	See Figure 1 and Table 1	-100			mV
I_{IN}	Input Current	$V_{IN} = 0V$ or V_{CC}			±20	µA
$I_{I(OFF)}$	Power-OFF Input Current	$V_{CC} = 0V$, $V_{IN} = 0V$ or 5.5V			±20	µA
V_{OH}	Output HIGH Voltage	$I_{OH} = -100 \mu A$ $I_{OH} = -8 mA$	$V_{CC} - 0.2$ 2.4			V
V_{OL}	Output LOW Voltage	$I_{OH} = 100 \mu A$ $I_{OL} = 8 mA$			0.2 0.5	V
I_{OZ}	Disabled Output Leakage Current	$EN = 0.8$ and $\overline{EN} = 2V$, $V_{OUT} = 7V$ or $0V$			±20	µA
V_{IK}	Input Clamp Voltage	$I_{IK} = -18 mA$	-1.5			V
I_{CCZ}	Disabled Power Supply Current	Receiver Disabled			5	mA
I_{CC}	Power Supply Current	Receiver Enabled ($R_{I+} = 1V$ and $R_{I-} = 1.4V$) or ($R_{I+} = 1.4V$ and $R_{I-} = 1V$)			15	mA
C_{IN}	Input Capacitance			3		pF
C_{OUT}	Output Capacitance			5		pF

Note 2: All typical values are at $T_A = 25^\circ C$ and with $V_{CC} = 5.0V$.

AC Electrical Characteristics

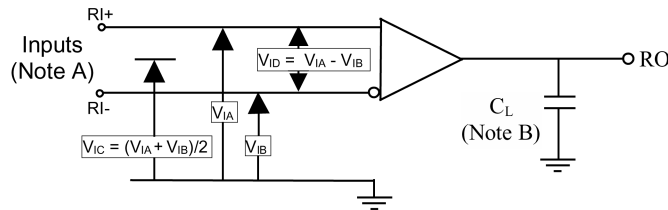
Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ (Note 3)	Max	Units
t_{PLH}	Propagation Delay LOW-to-HIGH	$ V_{ID} = 400 \text{ mV}$, $C_L = 10 \text{ pF}$ See Figure 1 and Figure 2	1.0		3.0	ns
t_{PHL}	Propagation Delay HIGH-to-LOW		1.0		3.0	ns
t_{TLH}	Output Rise Time (20% to 80%)			0.5		ns
t_{THL}	Output Fall Time (80% to 20%)			0.5		ns
$t_{SK(P)}$	Pulse Skew $ t_{PLH} - t_{PHL} $				0.4	ns
$t_{SK(LH)}$	Channel-to-Channel Skew (Note 4)	$R_L = 500\Omega$, $C_L = 10 \text{ pF}$ See Figure 3			0.3	ns
$t_{SK(HL)}$					0.3	ns
$t_{SK(PP)}$	Part-to-Part Skew (Note 5)				1.0	ns
t_{ZH}	LVTTTL Output Enable Time from Z to HIGH				5.0	ns
t_{ZL}	LVTTTL Output Enable Time from Z to LOW				5.0	ns
t_{HZ}	LVTTTL Output Disable Time from HIGH to Z			5.0	ns	
t_{LZ}	LVTTTL Output Disable Time from LOW to Z			5.0	ns	

Note 3: All typical values are at $T_A = 25^\circ\text{C}$ and with $V_{CC} = 5\text{V}$.

Note 4: $t_{SK(LH)}$, $t_{SK(HL)}$ is the skew between specified outputs of a single device when the outputs have identical loads and are switching in the same direction.

Note 5: $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction (either LOW-to-HIGH or HIGH-to-LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits.



Note A: All input pulses have frequency = 10 MHz, t_R or $t_F = 1 \text{ ns}$

Note B: C_L includes all probe and jig capacitances

FIGURE 1. Differential Receiver Voltage Definitions and Propagation Delay

TABLE 1. Receiver Minimum and Maximum Input Threshold Test Voltages

Applied Voltages (V)		Resulting Differential Input Voltage (mV)	Resulting Common Mode Input Voltage (V)
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25	1.15	100	1.2
1.15	1.25	-100	1.2
2.4	2.3	100	2.35
2.3	2.4	-100	2.35
0.1	0	100	0.05
0	0.1	-100	0.05
1.5	0.9	600	1.2
0.9	1.5	-600	1.2
2.4	1.8	600	2.1
1.8	2.4	-600	2.1
0.6	0	600	0.3
0	0.6	-600	0.3

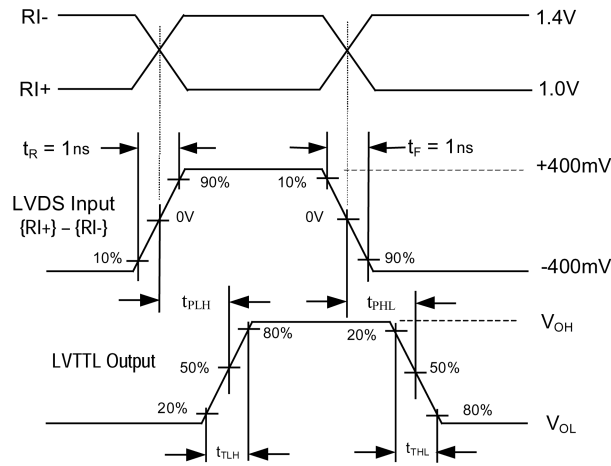
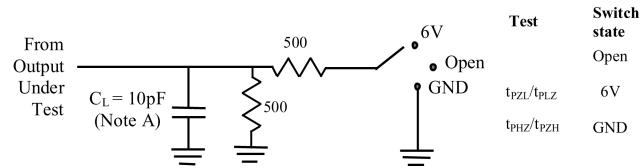
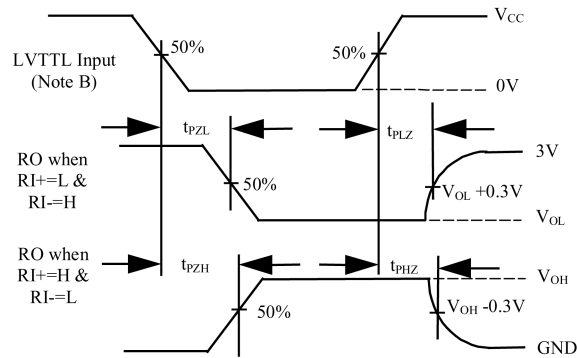


FIGURE 2. LVDS Input to LVTTTL Output AC Waveforms

Test Circuit for LVTTTL Outputs



Voltage Waveforms Enable and Disable Times

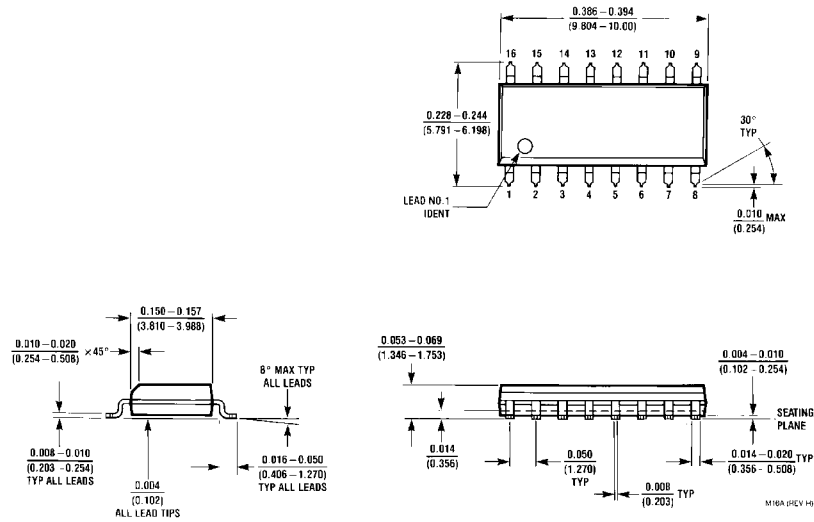


Note A: C_L includes probes and jig capacitance

Note B: All LVTTTL input pulses have the following characteristics: Frequency = 10 MHz, t_R or t_F = 2 ns

FIGURE 3. LVTTTL Outputs Test Circuit and AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow Package Number M16A

