Signetics

FAST 74F173
Quad D-Type Flip-Flop (3-State)

FAST Products

Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F173	125MHz	23mA

FEATURES

- **Edge-triggered D-type register**
- **Gated Clock Enable for hold "do nothing" mode**
- **3-state ouput buffers**
- **Gated Output Enable control**
- **Speed upgrade of N8T10 and current sink upgrade**
- **Controlled output edges to minimize ground bounces**
- **48mA sinking capability**

DESCRIPTION

The 74F173 is a high speed 4-bit parallel load register with clock enable control, 3-state buffered outputs, and Master Reset (MR). When the two clock Enable ($\overline{E}_0$ and $\overline{E}_1$) inputs are Low, the data on the D inputs is loaded into the register simultaneously with Low-to-High CLock (CP) transition. When one or both Enable inputs are High one setup time before the Low-to-High clock transition, the register retains the previous data. Data inputs and Clock Enable inputs are fully edge-triggered and must be stable only one setup time before the Low-to-High clock transition.The Master Reset(MR) is an active-High asynchronous input. When the MR is High, all four flip-flops are reset (cleared) independently of any other input condition.The 3-state output buffers are controlled by a 2-input NOR gate. When both Output Enable ($\overline{OE}_0$ and $\overline{OE}_1$) inputs are Low, the data in the register is presented at the Q output. When one or both $\overline{OE}$ inputs are High, the outputs are forced to a high impedance "off" state. The 3-state output buffers are completely independent of the register operation; the $\overline{OE}$ transition does not affect the clock and reset operations.

ORDERING INFORMATION

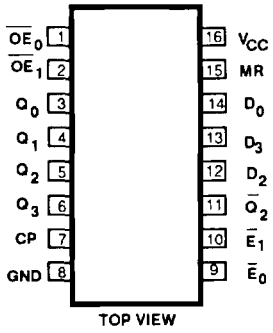
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F173N
16-Pin Plastic SO	N74F173D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input	1.0/1.0	20µA/0.6mA
$\overline{E}_0$, $\overline{E}_1$	Clock Enable inputs	1.0/1.0	20µA/0.6mA
MR	Master Reset input	1.0/1.0	20µA/0.6mA
$\overline{OE}_0$, $\overline{OE}_1$	Output Enable inputs	1.0/1.0	20µA/0.6mA
Q_0 - Q_4	Data outputs	750/80	15mA/48mA

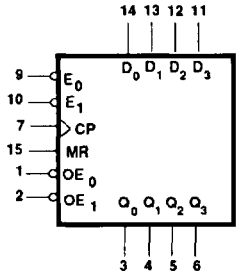
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



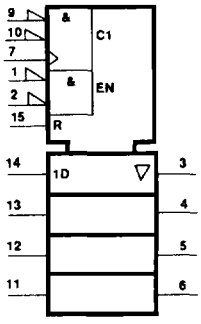
TOP VIEW

LOGIC SYMBOL

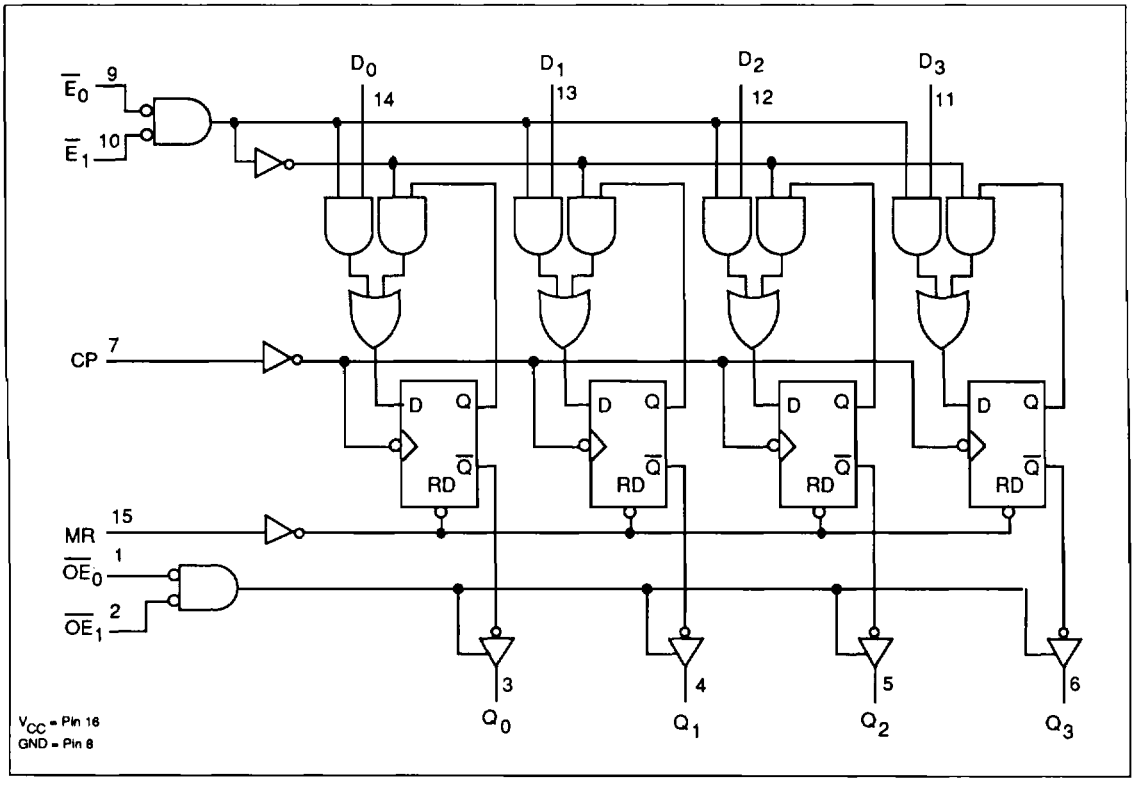


V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUT	OPERATING MODE
MR	CP	$\overline{E}_0$	$\overline{E}_1$	D_n	Q_n(Register)	
H	X	X	X	X	L	Reset (clear)
L	↑	l	l	l	L	Parallel load
L	↑	l	l	h	H	
L	X	h	X	X	q_n	Hold (do nothing)
L	X	X	h	X	q_n	

H = High voltage level
h = High voltage level one setup prior to Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup prior to Low-to-High clock transition
q_n = Lower case letters indicate the state of the referenced input (or output) on setup time priorn to the Low-to-High clock transition
X = Don't care
↑ =Low-to-High clock transition

FUNCTION TABLE

INPUTS			OUTPUT	OPERATING MODE
Q_n(Register)	$\overline{OE}_0$	$\overline{OE}_1$	Q_n	
L	L	L	L	Read
H	L	L	H	
X	H	X	Z	Disabled
X	X	H	Z	

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	96	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = -15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0	3.1		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX		±10%V_{CC}		0.38	0.55	V
					±5%V_{CC}		0.38	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				19	26	mA
		I_{CCL}					27	37	mA
		I_{CCZ}					23	32	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed lasty.

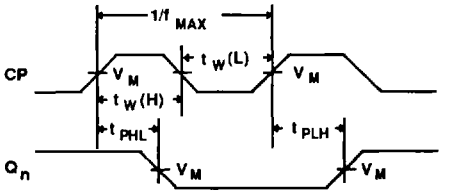
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	125		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	4.5 6.0	6.5 8.0	9.0 10.5	4.0 5.5	10.0 11.5	ns
t_{PHL}	Propagation delay MR to Q_n	Waveform 2	6.5	8.5	11.5	6.0	12.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 4 Waveform 5	3.5 5.5	5.0 7.0	8.0 10.0	2.5 4.5	8.5 11.0	ns
t_{PZH} t_{PZL}	Output Disable time to High or Low level	Waveform 4 Waveform 5	1.5 3.0	3.5 5.0	7.0 8.5	1.0 2.5	8.0 9.0	ns
t_{THL} t_{TLH}	Transition time 10% to 90%, 90% to 10%	Waveform 5 Waveform 4	2.0 4.0	5.0 7.5	8.0 10.0	2.0 4.0	8.5 11.0	ns

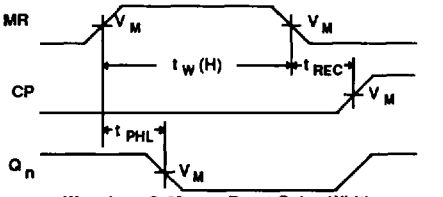
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 3	2.5 2.5			3.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{E}_n$ to CP	Waveform 3	4.5 7.5			5.0 8.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{E}_n$ to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	3.0 6.0			3.0 6.0		ns
$t_w(H)$	MR Pulse width, High	Waveform 2	3.5			3.5		ns
t_{REC}	Recovery time, MR to CP	Waveform 2	4.5			5.5		ns

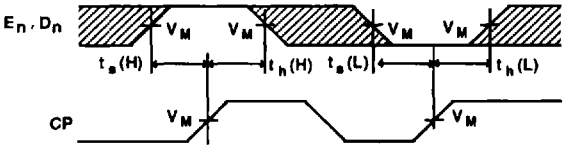
AC WAVEFORMS



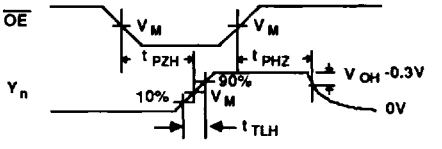
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



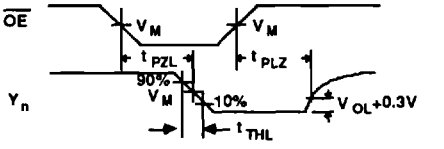
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Waveform 3. Data And Enable Setup And Hold Times



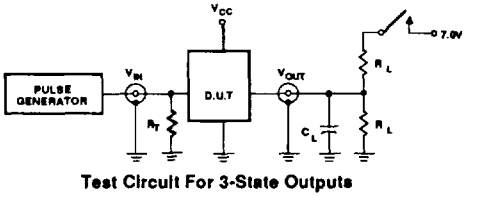
Waveform 4. 3-State Output Enable Time To High Level, Output Disable Time From High Level And Transition Time To High Level



Waveform 5. 3-State Output Enable Time To Low Level , Output Disable Time From Low Level And Transition Time To Low level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

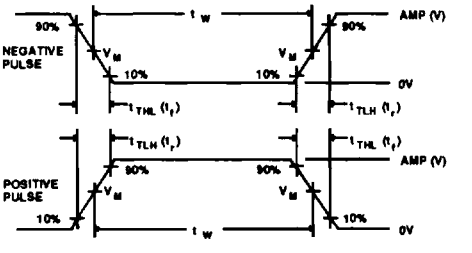
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns