

# MB81256-80

## MOS 262,144 BIT DYNAMIC RANDOM ACCESS MEMORY

### 262,144 Bit Dynamic Random Access Memory

The Fujitsu MB81256 is a fully decoded, dynamic NMOS random access memory organized as 262,144 one-bit words. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage, and environments where low power dissipation and a compact layout are required.

Multiplexed row and column address inputs permit the MB81256 to be housed in standard 16-pin DIP and ZIP packages or an 18-pin PLCC package. Pinouts conform to the JEDEC-approved pinouts. Additionally, the MB81256 offers new functional enhancements that make it more versatile than previous dynamic RAMs. CAS-before-RAS refresh provides an on-chip refresh capability that is upwardly compatible with the MB8266A. The MB81256 also features page mode which allows high speed random access of up to 512 bits of data within the same row.

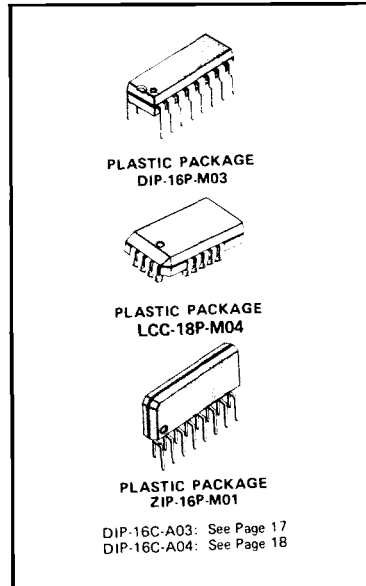
The MB81256 is fabricated using silicon gate NMOS and Fujitsu's advanced Triple-layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is used in the design, including the sense amplifiers. Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs are TTL compatible.

- 262,144 x 1 RAM organization
- Silicon-gate, Triple Poly NMOS, single transistor cell
- Row Access Time ( $t_{RAC}$ )  
80 ns max. (MB 81256-80)
- Random Cycle Time ( $t_{RC}$ )  
175 ns min. (MB 81256-80)
- Page Mode Cycle Time ( $t_{PCM}$ )  
100 ns max. (MB 81256-80)
- Single +5 V Supply,  $\pm 10\%$  tolerance
- Low Power  
385 mW max. (MB 81256-80)  
25 mW max. (standby)
- 256 refresh cycles every 4 ms
- CAS-before-RAS, RAS-only, Hidden refresh capability
- High speed Read-write-Write cycle
- $t_{AR}$ ,  $t_{WR}$ ,  $t_{BR}$ ,  $t_{WP}$  are eliminated
- Output unlatched cycle end allows two-dimensional chip select
- Common I/O capability using Early Write operation
- On-chip latches for Addresses and Data-in
- Standard 16-Pin Plastic Packages:  
DIP (MB81256-XXP)  
ZIP (MB81256-XXPSZ)
- Standard 18-Pin Plastic Package:  
PLCC (MB81256-XXPV)
- Standard 16-Pin Ceramic Package:  
DIP (MB81256-XXC)

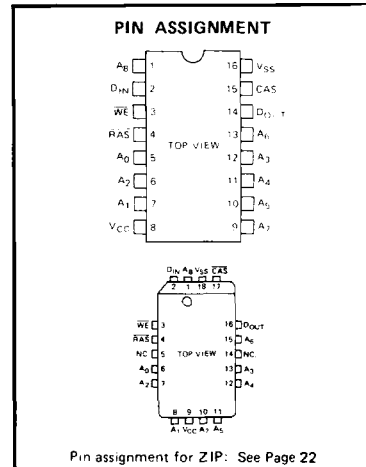
### Absolute Maximum Ratings (See Note)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-1 to +7	V
Voltage of $V_{CC}$ supply relative to $V_{SS}$	$V_{CC}$	-1 to +7	V
Storage Temperature	Ceramic	$T_{STG}$	-55 to +150
	Plastic		-55 to +125
Power Dissipation	$P_D$	1.0	W
Short Circuit Output Current	—	50	mA

**Note:** Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

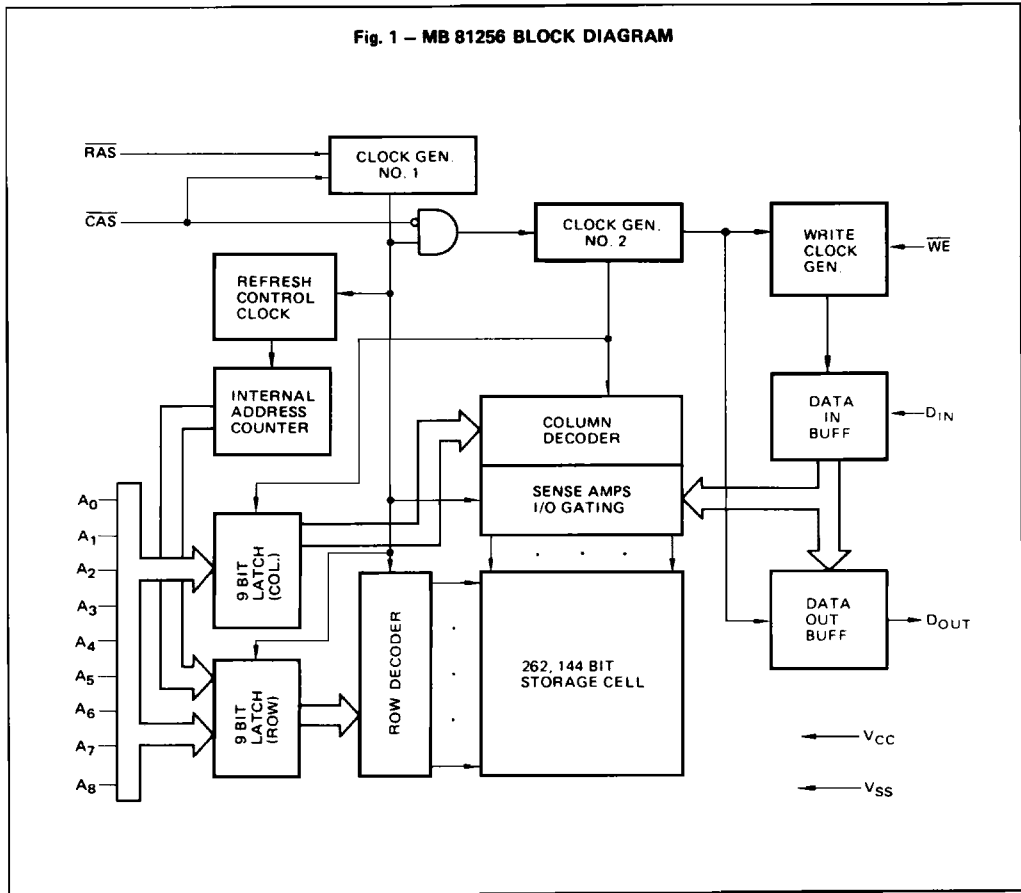


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This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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**CAPACITANCE** (T<sub>A</sub> = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance A <sub>0</sub> to A <sub>8</sub> , D <sub>IN</sub>	C <sub>IN1</sub>		7	pF
Input Capacitance RAS, CAS, WE	C <sub>IN2</sub>		10	pF
Output Capacitance D <sub>OUT</sub>	C <sub>OUT</sub>		7	pF

## RECOMMENDED OPERATING CONDITIONS

(Referenced to  $V_{SS}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V	0°C to +70°C
	$V_{SS}$	0	0	0	V	
Input High Voltage, all inputs	$V_{IH}$	2.4		6.5	V	
Input Low Voltage, all inputs	$V_{IL}$	-2.0		0.8	V	

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## DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Value			Unit	
		Min	Typ	Max		
OPERATING CURRENT* Average Power Supply Current ( $\overline{RAS}$ , $\overline{CAS}$ cycling; $t_{RC} = \text{Min.}$ )	MB 81256-80	$I_{CC1}$			70	mA
STANDBY CURRENT Standby Power Supply Current ( $\overline{RAS}$ , $\overline{CAS} = V_{IH}$ )		$I_{CC2}$			4.5	mA
REFRESH CURRENT 1* Average Power Supply Current ( $\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$ ; $t_{RC} = \text{Min.}$ )	MB 81256-80	$I_{CC3}$			60	mA
PAGE MODE CURRENT* Average Power Supply Current ( $\overline{RAS} = V_{IL}$ , $\overline{CAS}$ cycling; $t_{PC} = \text{Min.}$ )	MB81256-80	$I_{CC4}$			35	mA
REFRESH CURRENT 2* Average Power Supply Current ( $\overline{CAS}$ -before- $\overline{RAS}$ ; $t_{RC} = \text{Min.}$ )	MB 81256-80	$I_{CC5}$			65	mA
INPUT LEAKAGE CURRENT any input ( $V_{IN} = 0V$ to 5.5V, $V_{CC} = 4.5V$ to 5.5V, $V_{SS} = 0V$ , all other pins not under test = 0V)		$I_{I(L)}$	-10		10	$\mu A$
OUTPUT LEAKAGE CURRENT (Data is disabled, $V_{OUT} = 0V$ to 5.5V)		$I_{O(L)}$	-10		10	$\mu A$
OUTPUT LEVEL Output Low Voltage ( $I_{OL} = 4.2mA$ )		$V_{OL}$			0.4	V
OUTPUT LEVEL Output High Voltage ( $I_{OH} = -5.0mA$ )		$V_{OH}$	2.4			V

NOTE\* :  $I_{CC}$  is depended on output loading and cycle rates. Specified values are obtained with the output open.

## AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1, 2, 3

Parameter	NOTES	Symbol	Value		Unit
			Min	Max	
Time between Refresh		$t_{REF}$		4	ms
Random Read/Write Cycle Time		$t_{RC}$	175		ns
Read-Write Cycle Time		$t_{RWC}$	180		ns
Access Time from $\overline{RAS}$	4 6	$t_{RAC}$		80	ns
Access Time from $\overline{CAS}$	4 6	$t_{CAC}$		45	ns
Output Buffer Turn off Delay		$t_{OFF}$	0	25	ns
Transition Time		$t_T$	3	50	ns
$\overline{RAS}$ Precharge Time		$t_{RP}$	80		ns
$\overline{RAS}$ Pulse Width		$t_{RAS}$	85	100000	ns
$\overline{RAS}$ Hold Time		$t_{RSH}$	50		ns
$\overline{CAS}$ Pulse Width		$t_{CAS}$	50	100000	ns
$\overline{CAS}$ Hold Time		$t_{CSH}$	85		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	7 8	$t_{RCD}$	20	35	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		$t_{CRS}$	10		ns
Row Address Set Up Time		$t_{ASR}$	0		ns
Row Address Hold Time		$t_{RAH}$	10		ns
Column Address Set Up Time		$t_{ASC}$	0		ns
Column Address Hold Time		$t_{CAH}$	15		ns
Read Command Set Up Time		$t_{RCS}$	0		ns
Read Command Hold Time Referenced to $\overline{CAS}$	9	$t_{RCH}$	0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	9	$t_{RRH}$	20		ns
Write Command Set Up Time	10	$t_{WCS}$	0		ns
Write Command Pulse Width		$t_{WP}$	15		ns
Write Command Hold Time		$t_{WCH}$	15		ns
Write Command to $\overline{RAS}$ Lead Time		$t_{RWL}$	35		ns
Write Command to $\overline{CAS}$ Lead Time		$t_{CWL}$	35		ns
Data In Set Up Time		$t_{DS}$	0		ns
Data In Hold Time		$t_{OH}$	15		ns
$\overline{CAS}$ to WE Delay	10	$t_{CWD}$	15		ns
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ( $\overline{CAS}$ -before- $\overline{RAS}$ cycle)		$t_{FCS}$	20		ns
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ( $\overline{CAS}$ -before- $\overline{RAS}$ cycle)		$t_{FCH}$	20		ns

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## AC CHARACTERISTICS

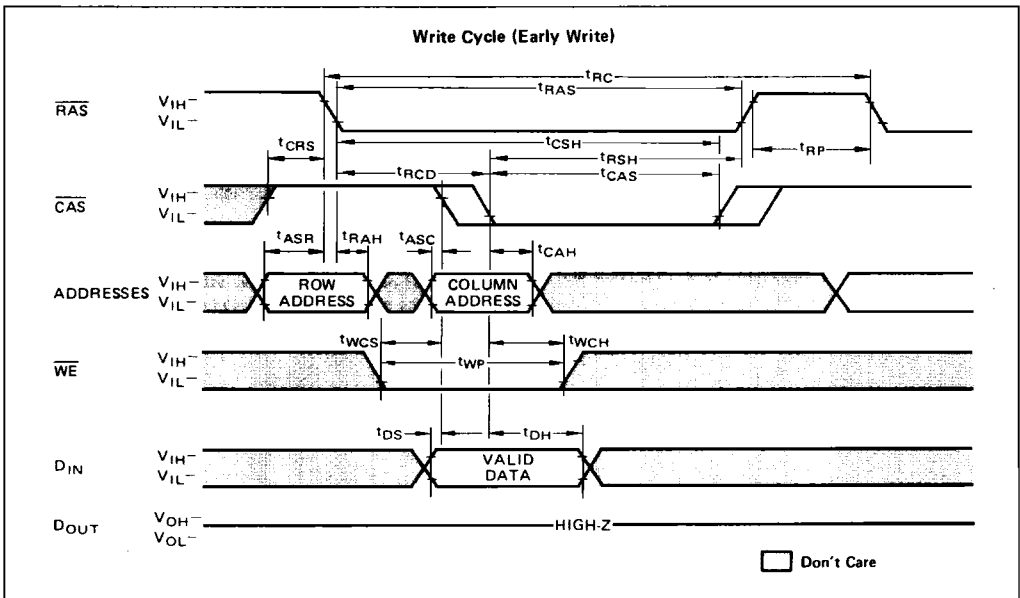
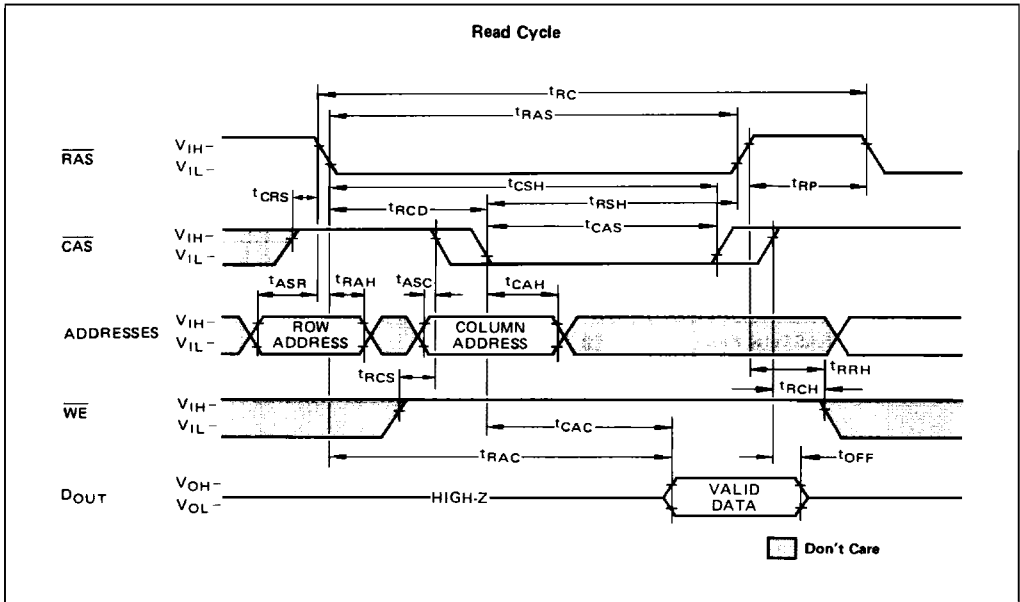
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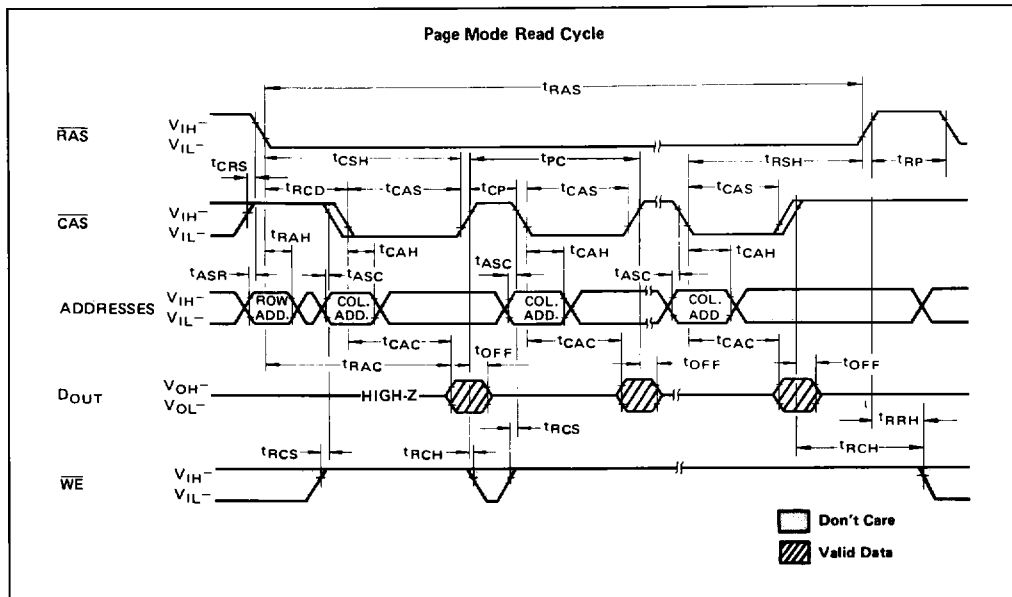
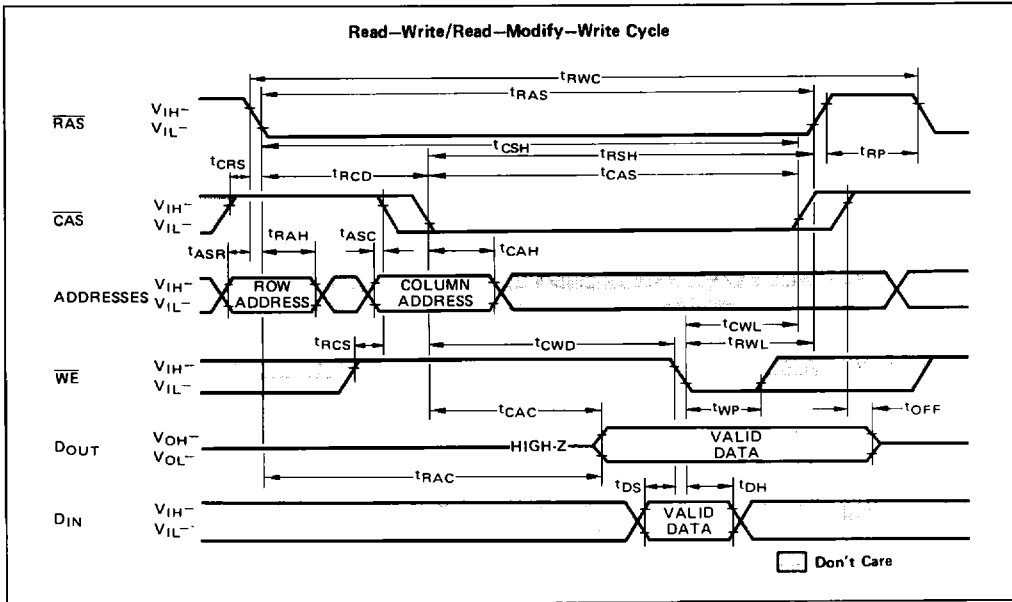
Parameter	NOTES	Symbol	Value		Unit
			Min	Max	
$\overline{\text{CAS}}$ Precharge Time ( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ cycle)		$t_{\text{CPR}}$	20		ns
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time (Refresh cycles)		$t_{\text{RPC}}$	20		ns
Page Mode Read/Write Cycle Time		$t_{\text{PC}}$	100		ns
Page Mode Read-Write Cycle Time		$t_{\text{PRWC}}$	100		ns
Page Mode $\overline{\text{CAS}}$ Precharge Time		$t_{\text{CP}}$	40		ns
Refresh Counter Test Cycle Time	10	$t_{\text{RTC}}$	330		ms
Refresh Counter Test $\overline{\text{RAS}}$ Pulse Width	11	$t_{\text{TRAS}}$	230	10000	ns
Refresh Counter Test $\overline{\text{CAS}}$ Precharge Time	11	$t_{\text{CPT}}$	50		ns

### Notes:

- 1 An initial pause of 200  $\mu\text{s}$  is required after power-up. And then several cycle (to which any 8 cycle to perform refresh are adequate) are required before proper device operation is achieved.  
If internal refresh counter is to be effective, a minimum of 8  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycles are required.
- 2 AC characteristics assume  $t_T = 5 \text{ ns}$ .
- 3  $V_{\text{IH}}$  (min) and  $V_{\text{IL}}$  (max) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{\text{IH}}$  (min) and  $V_{\text{IL}}$  (max.).
- 4 Assumes that  $t_{\text{RCD}} \leq t_{\text{RCD}} (\text{max.})$ . If  $t_{\text{RCD}}$  is greater than the maximum recommended value shown in this table,  $t_{\text{RAC}}$  will increase by the amount that  $t_{\text{RCD}}$  exceeds the value shown.
- 5 Assumes that  $t_{\text{RCD}} \geq t_{\text{RCD}} (\text{max.})$ .
- 6 Measured with a load equivalent to 2 TTL loads and 100 pF.
- 7 Operation within the  $t_{\text{RCD}} (\text{max.})$  limit insures that  $t_{\text{RAC}} (\text{max.})$  can be met.  $t_{\text{RCD}} (\text{max.})$  is specified as a reference point only; if  $t_{\text{RCD}}$  is greater than the specified  $t_{\text{RCD}} (\text{max.})$  limit, then access time is controlled exclusively by  $t_{\text{CAC}}$ .
- 8  $t_{\text{RCD}} (\text{min.}) = t_{\text{RAH}} (\text{min.}) + 2t_T$  ( $t_T = 5 \text{ ns}$ ) +  $t_{\text{ASC}} (\text{min.})$ .
- 9 Either  $t_{\text{RRH}}$  or  $t_{\text{RCH}}$  must be satisfied for a read cycle.
- 10  $t_{\text{WCS}}$  and  $t_{\text{CWD}}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{\text{WCS}} \geq t_{\text{WCS}} (\text{min.})$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle.  
If  $t_{\text{CWD}} \geq t_{\text{CWD}} (\text{min.})$  the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
- 11 Test mode cycle only.

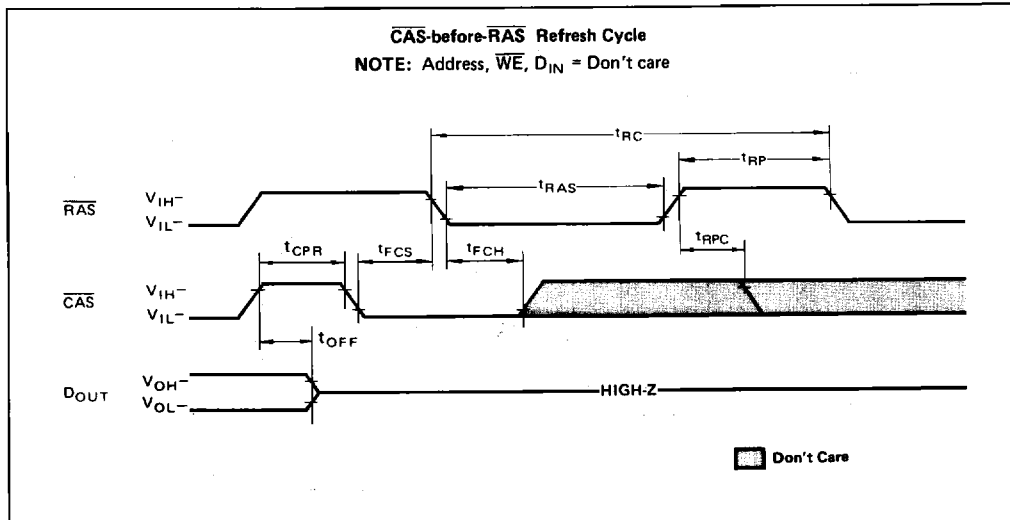
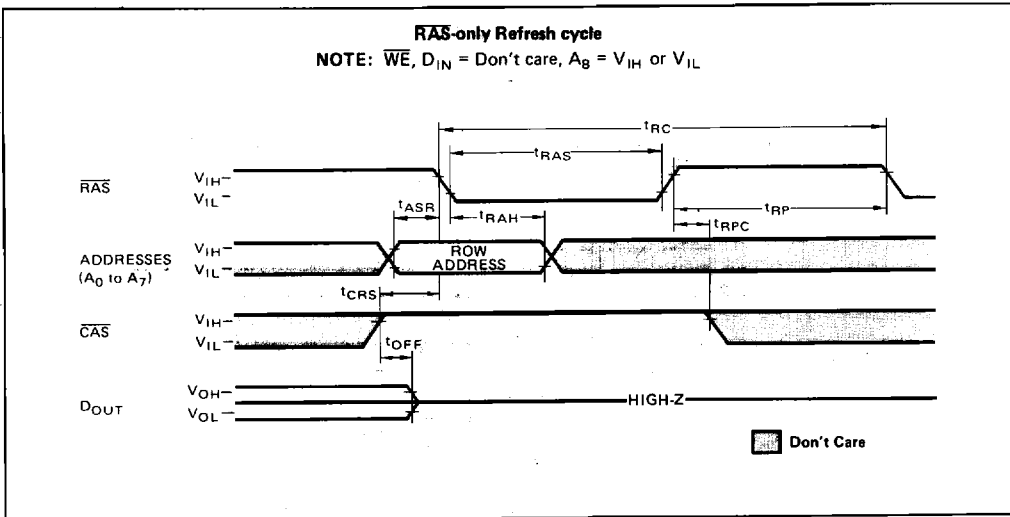
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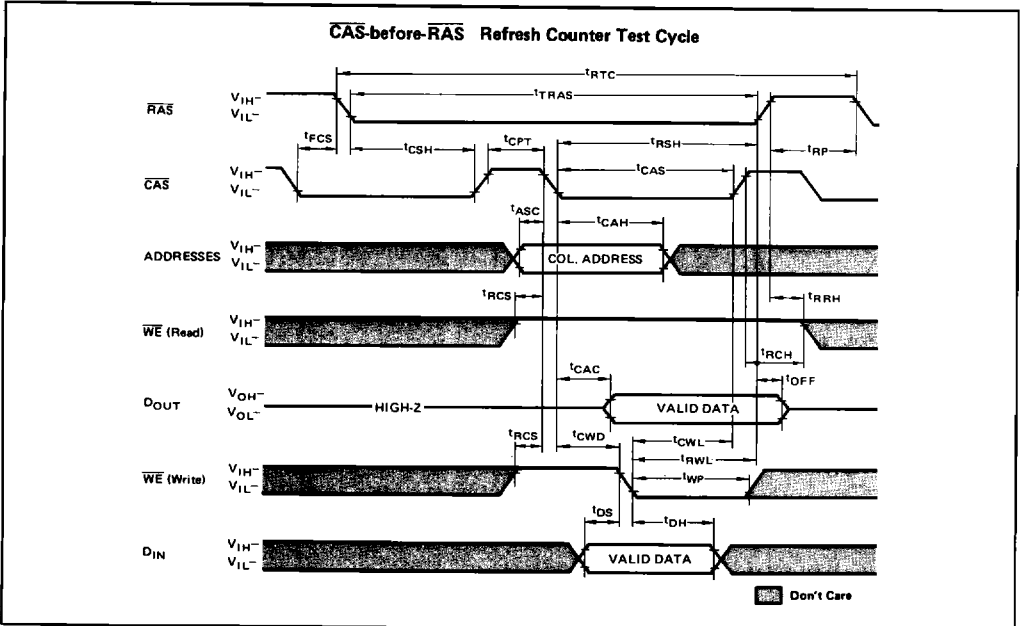
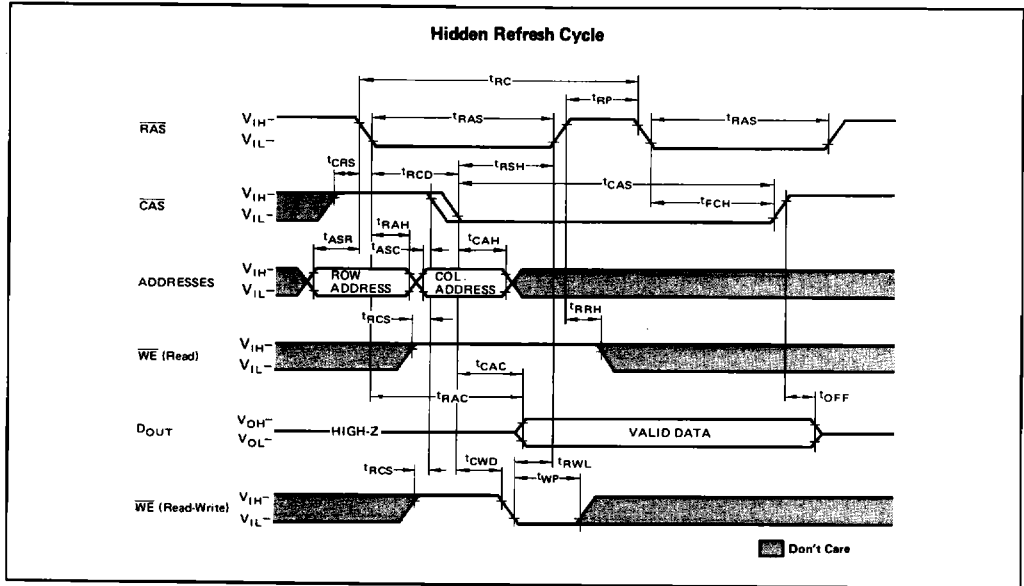




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## DESCRIPTION

### Simple Timing Requirement

The MB 81256 has improved circuitry that eases timing requirements for high speed access operations. The MB 81256 can operate under the condition of  $t_{\text{RCD}}(\text{max}) = t_{\text{CAC}}$  thus providing optimal timing for address multiplexing. In addition, the MB 81256 has the minimal hold time of Address ( $t_{\text{CAH}}$ ),  $\overline{\text{WE}}$  ( $t_{\text{WCH}}$ ) and  $\text{D}_{\text{IN}}$  ( $t_{\text{DH}}$ ). The MB 81256 provides higher throughput in inter-leaved memory system applications. Fujitsu has made timing requirements that are referenced to  $\overline{\text{RAS}}$  nonrestrictive and deleted them from the data sheet, these include  $t_{\text{AR}}$ ,  $t_{\text{WCR}}$ ,  $t_{\text{DHR}}$  and  $t_{\text{WD}}$ . As a result, the hold times of the Column Address,  $\text{D}_{\text{IN}}$  and  $\overline{\text{WE}}$  as well as  $t_{\text{CWD}}$  ( $\text{CAS}$  to  $\overline{\text{WE}}$  Delay) are not restricted by  $t_{\text{RCD}}$ .

### Address Inputs:

A total of eighteen binary input address bits are required to decode any 1 of 262,144 cell locations within the MB 81256. Nine row-address bits are established on the input pins ( $\text{A}_0$  to  $\text{A}_8$ ) and are latched with the Row Address Strobe ( $\overline{\text{RAS}}$ ). Nine column-address bits are established on the input pins and are latched with the Column Address Strobe ( $\text{CAS}$ ). All row addresses must be stable on or before the falling edge of  $\overline{\text{RAS}}$ .  $\text{CAS}$  is internally inhibited (or "gated") by  $\overline{\text{RAS}}$  to permit triggering of  $\text{CAS}$  as soon as the Row Address Hold Time ( $t_{\text{RAH}}$ ) specification has been satisfied and the address inputs have been changed from row-addresses to column-address.

### Write Enable:

The read mode or write mode is selected with the  $\overline{\text{WE}}$  input. A high on  $\overline{\text{WE}}$  selects read mode; low selects write mode. The data input is disable when read mode is selected.

### Data input:

Data is written into the MB 81256 during a write or read-write cycle. The later falling edge of  $\overline{\text{WE}}$  or  $\text{CAS}$  is a strobe for the Data In ( $\text{D}_{\text{IN}}$ ) register. In a write cycle, if  $\overline{\text{WE}}$  is brought low before

$\text{CAS}$ ,  $\text{D}_{\text{IN}}$  is strobed by  $\text{CAS}$ , and the set-up and hold times are referenced to  $\text{CAS}$ . In a read-write cycle,  $\overline{\text{WE}}$  can be delayed after  $\text{CAS}$  has been low and  $\text{CAS}$  to  $\overline{\text{WE}}$  Delay Time ( $t_{\text{CWD}}$ ) has been satisfied. Thus  $\text{D}_{\text{IN}}$  is strobed by  $\overline{\text{WE}}$ , and set-up and hold times are referenced to  $\overline{\text{WE}}$ .

### Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data-in. The output is in a high impedance state until  $\text{CAS}$  is brought low. In a read cycle, or read-write cycle, the output is valid after  $t_{\text{RAC}}$  from transition of  $\overline{\text{RAS}}$  when  $t_{\text{RCD}}(\text{max})$  is satisfied, or after  $t_{\text{CAC}}$  from transition of  $\text{CAS}$  when the transition occurs after  $t_{\text{RCD}}(\text{max})$ . Data remain valid until  $\text{CAS}$  is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

### Fast Read-While-Write cycle

The MB 81256 has a fast read while write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings described in the previous section. The output buffer is controlled by the state of  $\overline{\text{WE}}$  when  $\text{CAS}$  goes low. When  $\overline{\text{WE}}$  is low during  $\text{CAS}$  transition to low, the MB 81256 goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. Whereas, when  $\overline{\text{WE}}$  goes low after  $t_{\text{CWD}}$  following  $\text{CAS}$  transition to low, the MB 81256 goes into the delayed write mode. The output then contains the data from the cell selected and the data from  $\text{D}_{\text{IN}}$  is written into the cell selected. Therefore, a very fast read write cycle is possible with the MB 81256.

### Page Mode:

Page-mode operation permits strobing the row-address into the MB 81256 while maintaining  $\overline{\text{RAS}}$  at a low throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the

falling edge of  $\overline{\text{RAS}}$  is saved. Access and cycle times are decreased because the time normally required to strobe a new row address is eliminated.

### Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses ( $\text{A}_0$  to  $\text{A}_7$ ) at least every 4ms. The MB 81256 offers the following 3 types of refresh.

#### $\overline{\text{RAS}}$ -only Refresh;

$\overline{\text{RAS}}$ -only refresh avoids any output during refresh because the output buffer is in the high impedance state unless  $\text{CAS}$  is brought low.

Strobing each of 256 row-addresses ( $\text{A}_0$  to  $\text{A}_7$ ) with  $\overline{\text{RAS}}$  will cause all bits in each row to be refreshed. Further  $\overline{\text{RAS}}$ -only refresh results in a substantial reduction in power dissipation. During  $\overline{\text{RAS}}$ -only refresh cycle, either  $V_{\text{IH}}$  or  $V_{\text{IL}}$  is permitted to  $\text{A}_8$ .

#### $\text{CAS}$ -before- $\overline{\text{RAS}}$ Refresh;

$\text{CAS}$ -before- $\overline{\text{RAS}}$  refreshing available on the MB 81256 offers an alternate refresh method. If  $\text{CAS}$  is held "low" for the specified period ( $t_{\text{FCS}}$ ) before  $\overline{\text{RAS}}$  goes to "low", on-chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next  $\text{CAS}$ -before- $\overline{\text{RAS}}$  refresh operation.

#### Hidden Refresh;

A hidden refresh cycle may take place while maintaining the latest valid data at the output by extending  $\text{CAS}$  active time.

For the MB 81256 a hidden refresh is a  $\text{CAS}$ -before- $\overline{\text{RAS}}$  refresh cycle. The internal refresh address counters provide the refresh addresses, as in a normal  $\text{CAS}$ -before- $\overline{\text{RAS}}$  refresh cycle.

#### $\text{CAS}$ -before- $\overline{\text{RAS}}$ Refresh Counter Test Cycle:

A special timing sequence using  $\text{CAS}$ .

before- $\overline{RAS}$  counter test cycle provides a convenient method of verifying the functionality of the  $\overline{CAS}$ -before- $\overline{RAS}$  refresh activated circuitry.

After the  $\overline{CAS}$ -before- $\overline{RAS}$  refresh operation, if  $\overline{CAS}$  goes to high and then goes to low again while  $\overline{RAS}$  is held low, the read and write operations are enabled.

This is shown in the  $\overline{CAS}$ -before- $\overline{RAS}$  counter test cycle timing diagram. A memory cell address (consisting of a row address (9 bits) and column address (9 bits) to be accessed can be defined as follows:

\*A ROW ADDRESS – Bits  $A_0$  to  $A_7$

are defined by the refresh counter.

The bit  $A_8$  is set high internally.

\*A COLUMN ADDRESS – All the bits  $A_0$  to  $A_8$  are defined by latching levels on  $A_0$  to  $A_8$  at the second falling edge of  $\overline{CAS}$ .

**Suggested  $\overline{CAS}$ -before- $\overline{RAS}$  Counter Test Procedure**

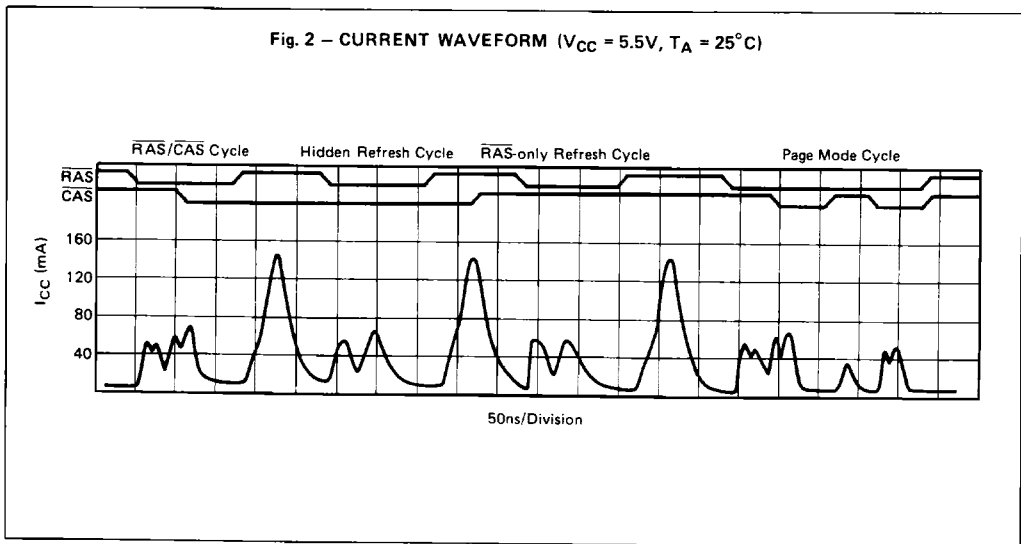
The timing as shown in the  $\overline{CAS}$ -before- $\overline{RAS}$  Counter Test cycles is used for the following operations:

- (1) Initialize the internal refresh address counter by using eight  $\overline{CAS}$ -before- $\overline{RAS}$  refresh cycles.
- (2) Throughout the test, use the same

column address, and keep  $RA8$  high.

- (3) Write "low" to all 256 row address on the same column address by using normal early write cycles.
- (4) Read "low" written in step 3) and check, and simultaneously write "high" to the same address by using internal refresh counter test read-write cycles. This step is repeated 256 times, with the addresses being generated by internal refresh address counter.
- (5) Read "high" written in step 4) and check by using normal read cycle for all 256 locations.
- (6) Complement the test pattern and repeat step 3), 4) and 5).

Fig. 2 – CURRENT WAVEFORM ( $V_{CC} = 5.5V, T_A = 25^\circ C$ )



## TYPICAL CHARACTERISTICS CURVES

Fig. 3 – NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE

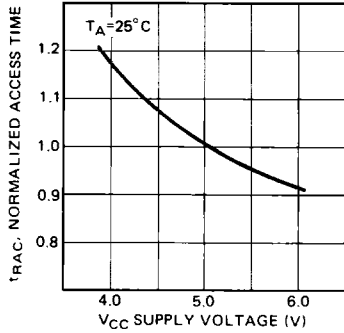


Fig. 4 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE

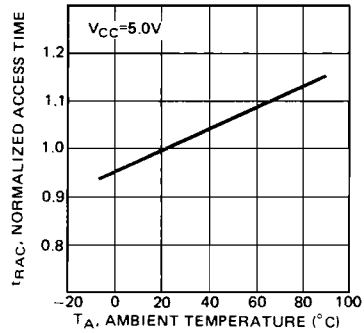


Fig. 5 – OPERATING CURRENT vs CYCLE RATE

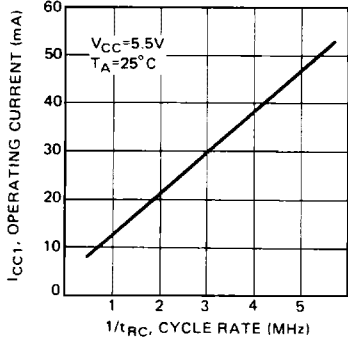


Fig. 6 – OPERATING CURRENT vs SUPPLY VOLTAGE

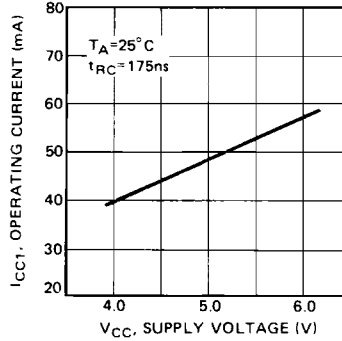


Fig. 7 – OPERATING CURRENT vs AMBIENT TEMPERATURE

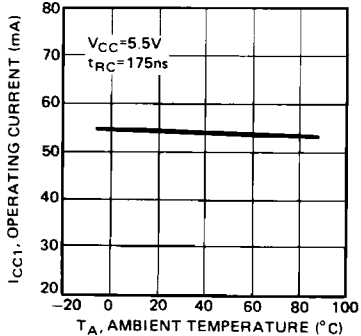
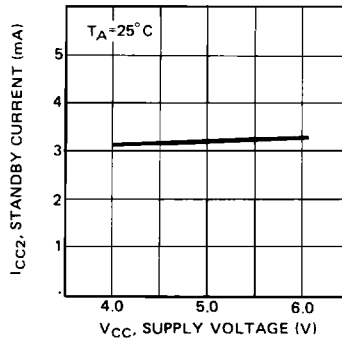


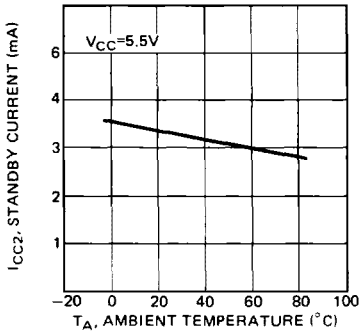
Fig. 8 – STANDBY CURRENT vs SUPPLY VOLTAGE



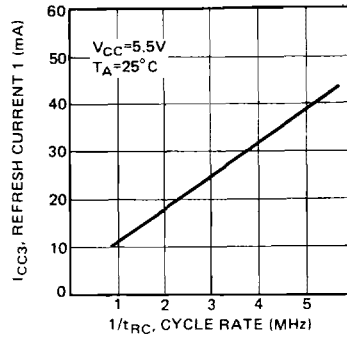
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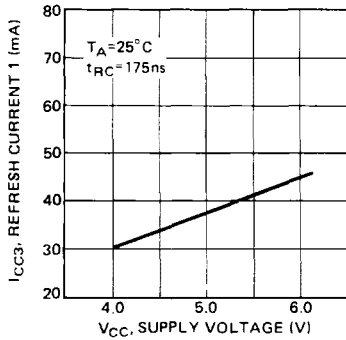
**Fig. 9 – STANDBY CURRENT vs AMBIENT TEMPERATURE**



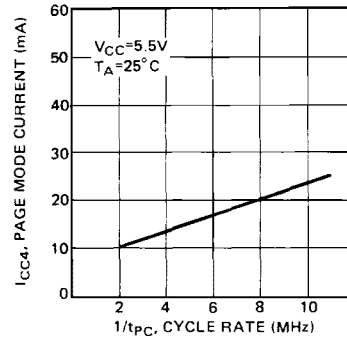
**Fig. 10 – REFRESH CURRENT 1 vs CYCLE RATE**



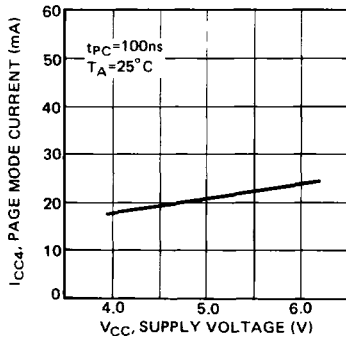
**Fig. 11 – REFRESH CURRENT 1 vs SUPPLY VOLTAGE**



**Fig. 12 – PAGE MODE CURRENT vs CYCLE RATE**



**Fig. 13 – PAGE MODE CURRENT vs SUPPLY VOLTAGE**



**Fig. 14 – REFRESH CURRENT 2 vs CYCLE RATE**

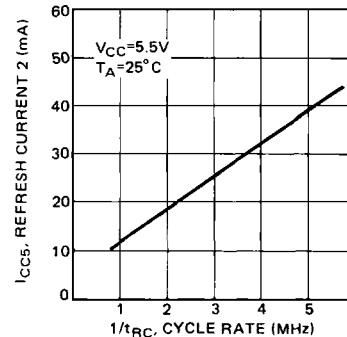


Fig. 15 – REFRESH CURRENT 2 vs SUPPLY VOLTAGE

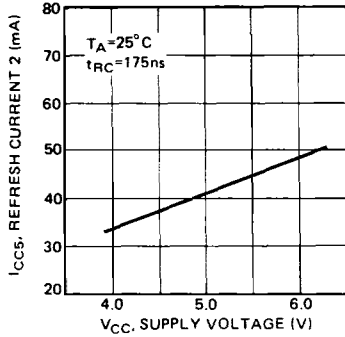


Fig. 16 – ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE

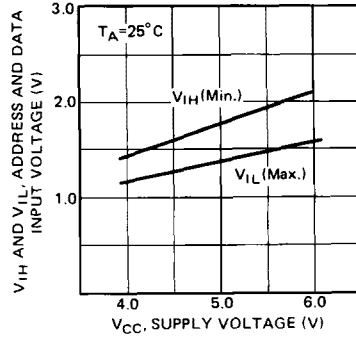


Fig. 17 – ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE

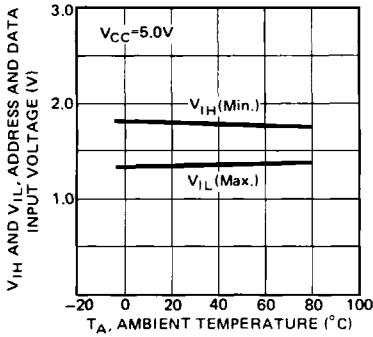


Fig. 18 – RAS, CAS AND WE INPUT VOLTAGE vs SUPPLY VOLTAGE

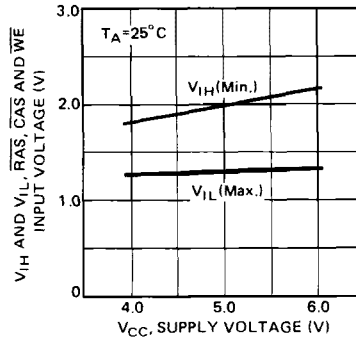


Fig. 19 – RAS, CAS AND WE INPUT VOLTAGE vs AMBIENT TEMPERATURE

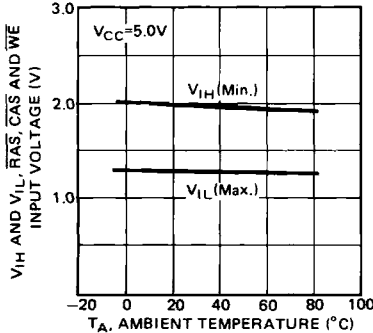
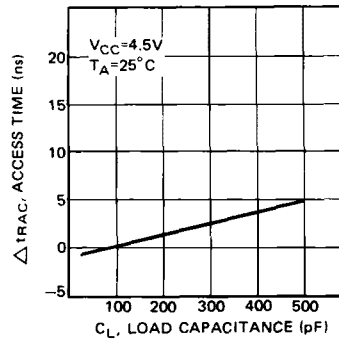


Fig. 20 – ACCESS TIME vs LOAD CAPACITANCE



1

Fig. 21 – OUTPUT CURRENT vs OUTPUT VOLTAGE

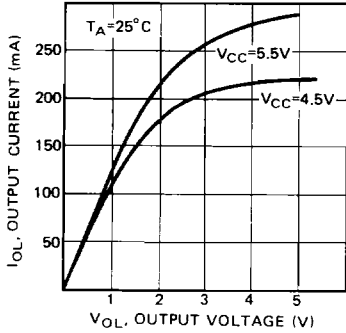


Fig. 22 – OUTPUT CURRENT vs OUTPUT VOLTAGE

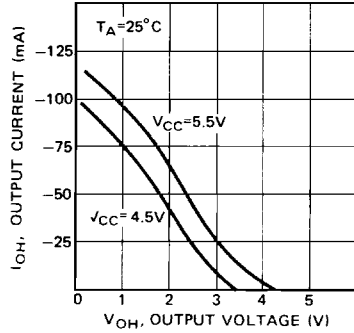


Fig. 23 – CURRENT WAVEFORM DURING POWER UP

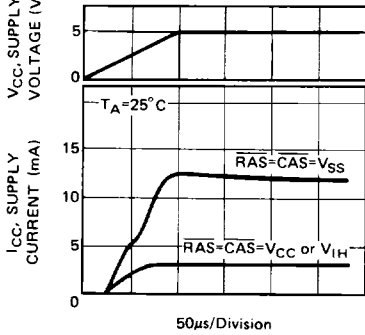
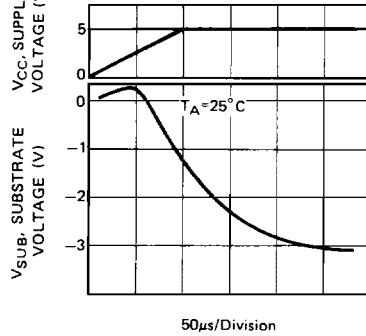
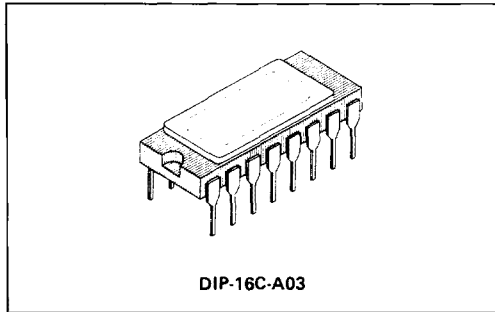


Fig. 24 – SUBSTRATE VOLTAGE DURING POWER UP

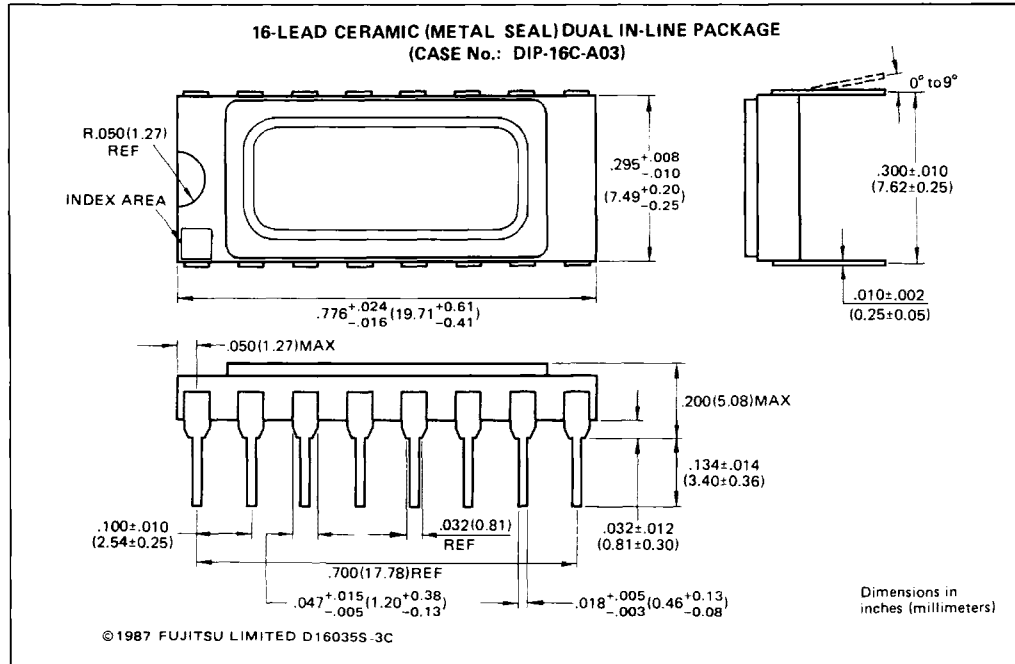


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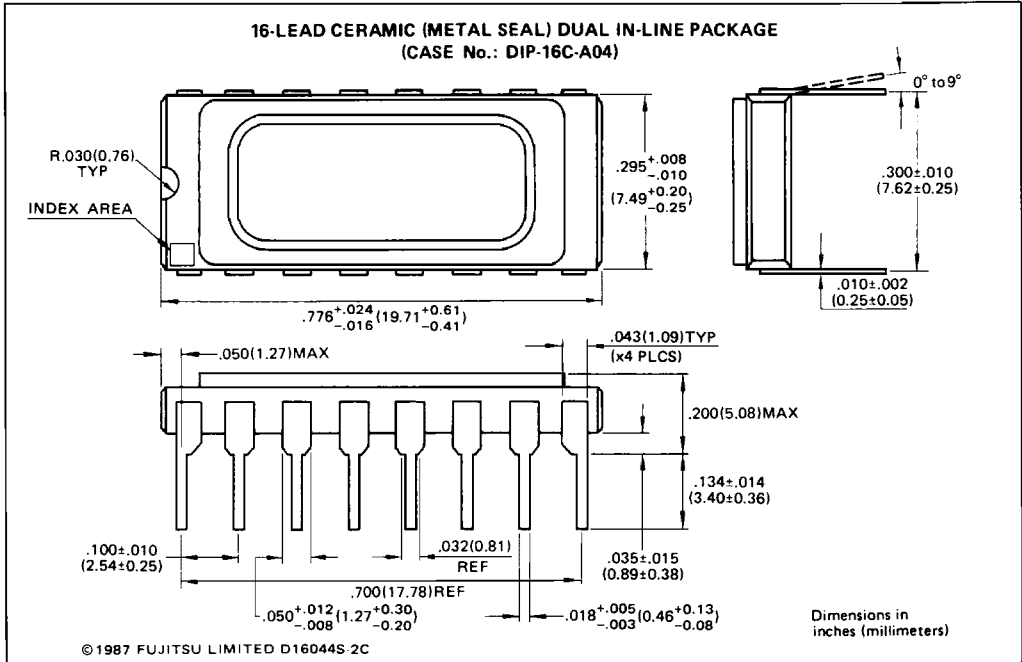
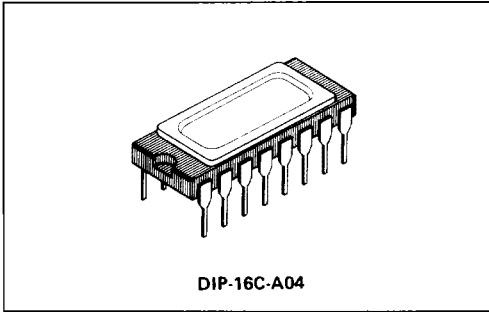
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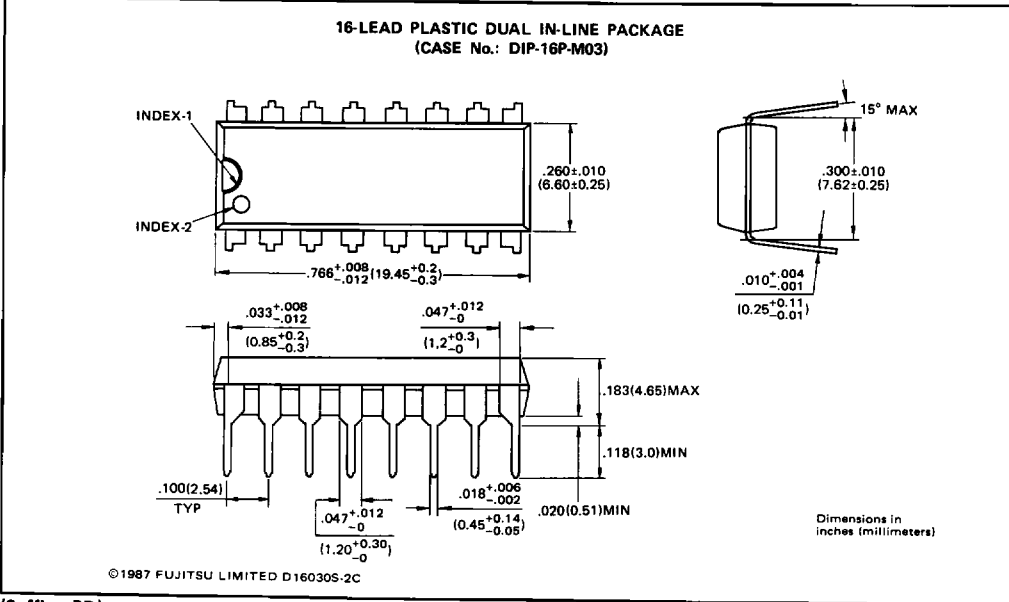
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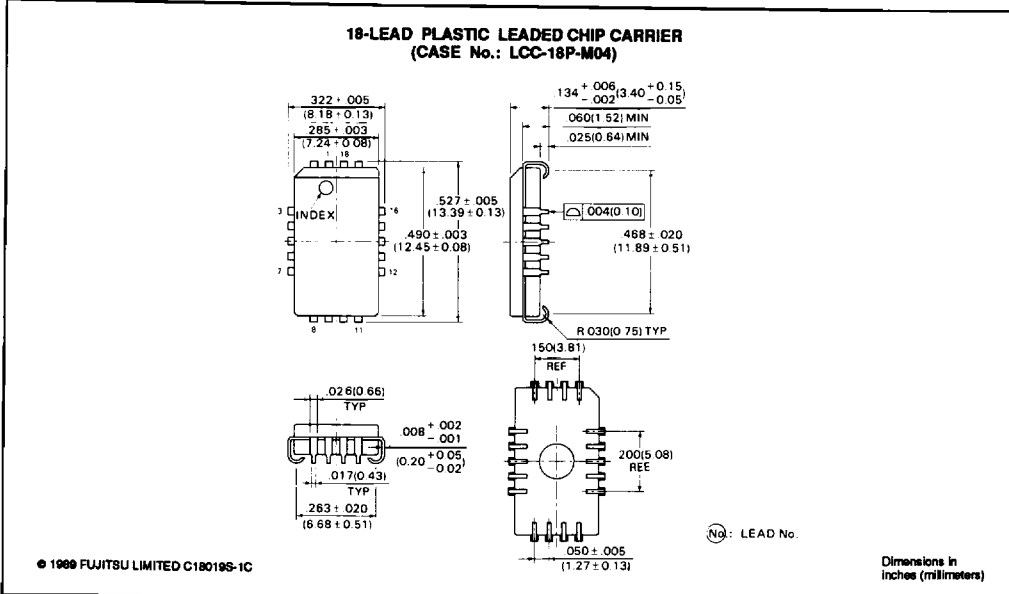


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(Suffix: -PD)



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# PACKAGE DIMENSIONS

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