CELESTICA™

16M x 32 EDO SIMM

FEATURES

- 72-pin industry standard four-byte single-in-line memory module
- JEDEC compliant: 21-C, Fig. 4-6, 4-18 (Release 6)
  No. 95 MO-116
- Supports 90°, 40° and 22.5° connectors
- High performance, CMOS
- Single 5.0V ± 10% power supply
- TTL-compatible inputs and outputs
- Extended Data Out access cycle
- Refresh modes: $\overline{\text{RAS}}$-ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$, HIDDEN
- Refresh: 4096 refresh cycles every 64 ms
- Dimensions: 4.25" (length) x 1.00" (height) x 0.208" (max thickness)

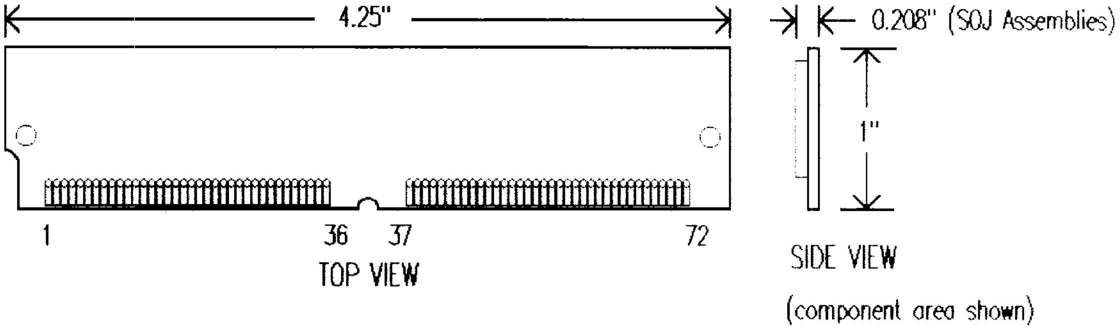
PERFORMANCE RANGE

SYMBOL	PARAMETER	Rating	
		60 ns	70 ns
t_{RAC}	$\overline{\text{RAS}}$ Access Time	60 ns (max)	70 ns (max)
t_{CAC}	$\overline{\text{CAS}}$ Access Time	15 ns (max)	20 ns (max)
t_{AA}	Access Time from Column Address	30 ns (max)	35 ns (max)
t_{RC}	Random Read or Write Cycle Time	104 ns (min)	124 ns (min)
t_{HPC}	EDO Mode Cycle Time	25 ns (min)	30 ns (min)

ORDERING INFORMATION

DESCRIPTION	PART NUMBER	ENGINEERING DESCRIPTOR
16M x 32, 60 ns, Gold Tabs, SOJ	20648C	CL001E16325B00J-60
16M x 32, 70 ns, Gold Tabs, SOJ	20649C	CL001E16325B00J-70
16M x 32, 60 ns, Tin/Lead Tabs, SOJ	20362C	CL001D16325B00J-60
16M x 32, 70 ns, Tin/Lead Tabs, SOJ	20650C	CL001D16325B00J-70

CARD OUTLINE



GENERAL DESCRIPTION

The 16M x 32 SIMM uses dynamic RAM devices and is designed for use as a general-purpose four-byte wide memory assembly with eight data bits per byte. The SIMM is populated with eight 16M x 4 DRAMs.

Presence Detect (PD) bits provide information about SIMM density, addressing, performance and features.

During Read or Write Cycles, each byte may be uniquely addressed via 24 address bits, with the first 12 bits (A0~A11) latched on $\overline{\text{RAS}}$ and the latter 12 bits (A0~A11) latched on $\overline{\text{CAS}}$. READ or WRITE cycles are selected with the $\overline{\text{WE}}$ input, with a logic low indicating a WRITE cycle and a logic HIGH indicating a READ cycle. During a WRITE cycle, data-in is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last.

EXTENDED DATA OUT (EDO) operation allows for faster READs or WRITEs within a row-address-defined page boundary. EDO MODE is an enhanced FAST PAGE MODE method of operation. An EDO MODE cycle is initiated with $\overline{\text{RAS}}$ followed by $\overline{\text{CAS}}$, then strobing $\overline{\text{CAS}}$ to latch different column addresses while holding RAS LOW.

Returning $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high terminates a memory cycle and returns the DRAMs to a reduced-current STANDBY state.

Memory cell data is retained in its correct state by maintaining power and executing any RAS cycle (READ, WRITE) or $\overline{\text{RAS}}$ refresh cycle ($\overline{\text{RAS}}$-ONLY,CBR, or HIDDEN) so that all 4096 combinations of RAS addresses (A0~A11) are executed at least every 64 ms. The CBR refresh and HIDDEN refresh cycles will invoke the on-chip refresh address counters for automatic $\overline{\text{RAS}}$ addressing.

PIN DESCRIPTION

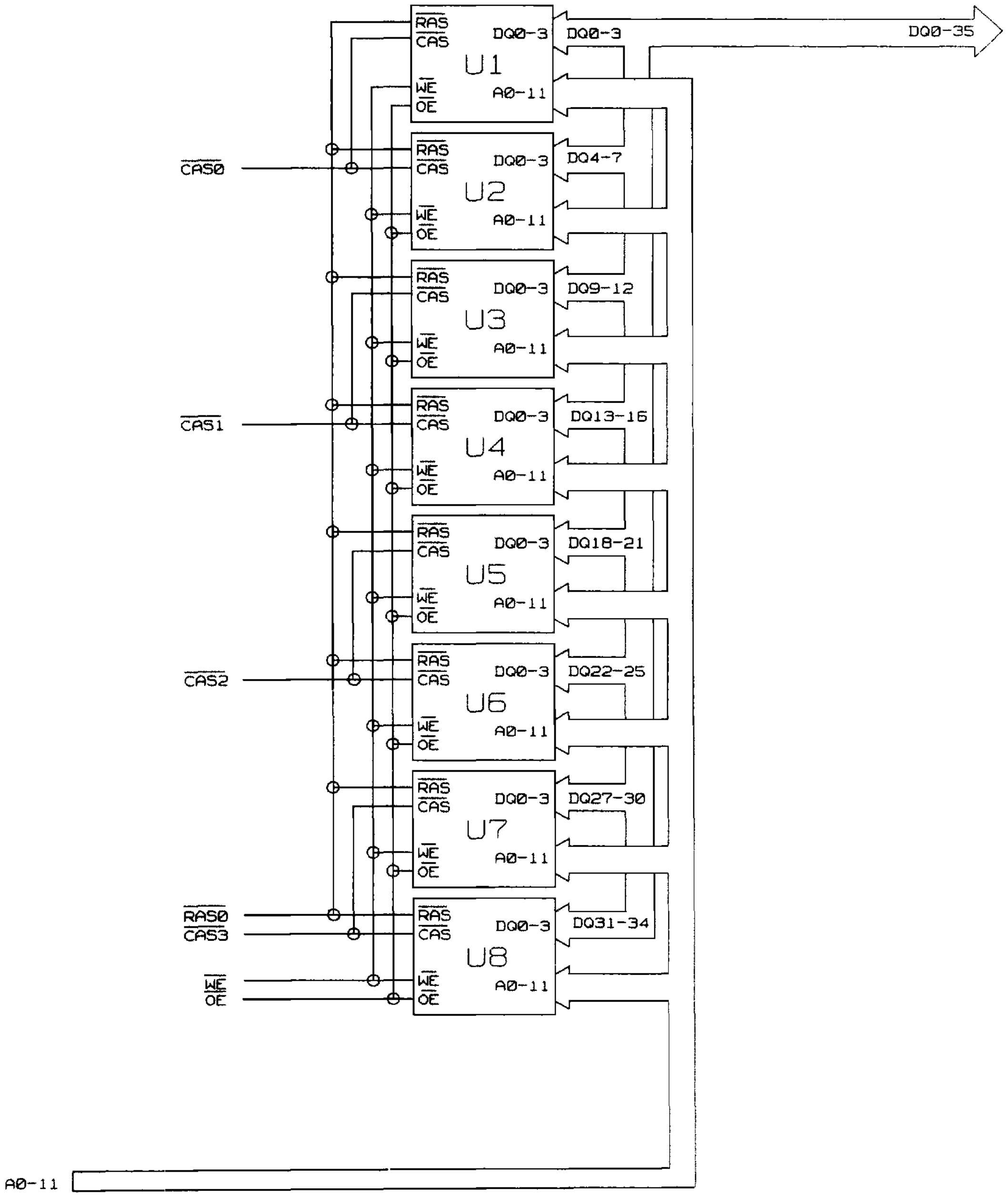
$\overline{\text{RAS0}}$,$\overline{\text{RAS2}}$	Row Address Strobe
$\overline{\text{CAS0}}$~$\overline{\text{CAS3}}$	Column Address Strobe
$\overline{\text{WE}}$	Write Enable
A0~A11	Address Inputs
DQ0~7,DQ9~16, DQ18~25,DQ27~34	Data In/Out
DQ8,17,26,35	Parity In/Out
VCC	Power (+5.0V)
VSS	Ground
NC	No Connection
PD1~5,PDEDO	Presence Detects

PRESENCE DETECT

PIN SYMBOL	CONFIGURATION	
	60 ns	70 ns
PD1	VSS	VSS
PD2	NC	NC
PD3	NC	VSS
PD4	NC	NC
PD5	NC	NC
PDEDO	VSS	VSS

PIN CONFIGURATION

#	Name	#	Name	#	Name	#	Name	#	Name	#	Name
1	VSS	13	A1	25	DQ24	37	DQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	DQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	VSS	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{\text{CAS0}}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	A11	41	$\overline{\text{CAS2}}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	VCC	42	$\overline{\text{CAS3}}$	54	DQ29	66	$\overline{\text{EDO}}$
7	DQ20	19	A10	31	A8	43	$\overline{\text{CAS1}}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{\text{RAS0}}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	NC	45	$\overline{\text{RAS1}}$	57	DQ13	69	PD3
10	VCC	22	DQ5	34	NC	46	$\overline{\text{OE}}$	58	DQ31	70	PD4
11	PD5	23	DQ23	35	DQ26	47	$\overline{\text{WE}}$	59	VCC	71	NC
12	A0	24	DQ6	36	DQ8	48	PD(ECC)	60	DQ32	72	VSS



FUNCTIONAL BLOCK DIAGRAM

(DQ8, 17, 26, 35 ARE FOR PARITY AND ARE NOT USED)

TRUTH TABLE

FUNCTION		$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ROW ADDR	COL ADDR	DATA IN/OUT
Standby		H	H→X	X	X	X	Hi-Z
Read		L	L	H	ROW	COL	Valid D_{OUT}
Early-Write		L	L	L	ROW	COL	Valid D_{IN}
EDO Mode-Read	1st Cycle	L	H→L	H	ROW	COL	Valid D_{OUT}
	2nd Cycle	L	H→L	H	N/A	COL	Valid D_{OUT}
EDO Mode-Read ($\overline{\text{WE}}$ Control)	1st Cycle	L	H→L	H→L→H	ROW	COL	Valid D_{OUT}
	2nd Cycle	L	H→L	H→L→H	N/A	COL	Valid D_{OUT}
EDO Mode-Write	1st Cycle	L	H→L	L	ROW	COL	Valid D_{IN}
	2nd Cycle	L	H→L	L	N/A	COL	Valid D_{IN}
$\overline{\text{RAS}}$-Only Refresh		L	H	X	ROW	N/A	Hi-Z
Hidden Refresh	Read	L→H→L	L	H	ROW	COL	Valid D_{OUT}
	Write	L→H→L	L	L	ROW	COL	Valid D_{IN}
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh		H→L	L	H	X	X	Hi-Z

X:"H" or "L" D_{IN}:Data In D_{OUT}:Data Out Hi-Z:High Impedance N/A:Not Applicable

ABSOLUTE MAXIMUM RATINGS (Note 1,22)

SYMBOL	PARAMETER	RATING	UNITS	NOTES
V_{CC}	Power Supply Voltage	-1.0 to 7.0	V	2
V_{IN}	Voltage on any Pin Relative to V_{SS}	-1.0 to 7.0	V	2
V_{OUT}		-1.0 to 7.0	V	2
T_{opr}	Operating Temperature	0 to 70	°C	
T_{stg}	Storage Temperature	-55 to 150	°C	
P_D	Power Dissipation	8	W	17,31
I_{OS}	Short Circuit Output Current	50	mA	17

RECOMMENDED OPERATING CONDITIONS (T_A= 0 to 70 °C) (Note 2)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Ground	0	0	0	V	
V_{IH}	Input High Voltage	2.4	-	Vcc	V	22
V_{IL}	Input Low Voltage	-1	-	0.8	V	22

T_A: Ambient temperature

CAPACITANCE (f = 1 MHz; T_A = 25 °C) (Note 22)

SYMBOL	PARAMETER	MAX.	UNITS	NOTES
C_{I1}	Input Capacitance (A0-A11)	40	pF	
C_{I2}	Input Capacitance ($\overline{RAS0}$,$\overline{RAS2}$)	56	pF	
C_{I3}	Input Capacitance ($\overline{CAS0}$~$\overline{CAS3}$)	14	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	56	pF	
C_{I5}	Input Capacitance ($\overline{OE}$)	56	pF	
C_{O1}	Output Capacitance (Data In/Out)	7	pF	

T_A: Ambient temperature

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) (Note 18,22)

SYMBOL	PARAMETER	SPEED	MIN.	MAX.	NOTES
I_{CC1}	OPERATING CURRENT: Average Power Supply Operating Current ($\overline{RAS}$,$\overline{CAS}$, Address Cycling@$t_{RC} = t_{RC(min)}$,$V_{CC} = V_{CC\ (max)}$)(mA)	60 ns	-	720	3,4,5,6, 16
		70 ns	-	640	
I_{CC2}	STANDBY CURRENT (TTL): Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=Vcc, Data out is disabled (Hi-Z), all other inputs =Vcc, $V_{CC} = V_{CC\ (max)}$) (mA)	Don't Care	-	16	
I_{CC3}	$\overline{RAS}$-ONLY REFRESH CURRENT: Average Power Supply Current, $\overline{RAS}$-Only Mode ($\overline{RAS}$, Address Cycling, $\overline{CAS}$=V_{IH}@$t_{RC}=t_{RC(min)}$,$V_{CC}=V_{CC(max)}$) (mA)	60 ns	-	720	3,4,5,6,16, 31
		70 ns	-	640	
I_{CC4}	EXTENDED DATA OUT MODE CURRENT: Average Power Supply Current, EDO ($\overline{RAS}$=V_{IL},$\overline{CAS}$, Address Cycling@ $t_{PC}=t_{PC(min)}$,$V_{CC}=V_{CC(max)}$) (mA)	60 ns	-	480	3,4,5,7,16
		70 ns	-	440	
I_{CC5}	STANDBY CURRENT (CMOS): Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V, Data Out is disabled (Hi-Z),$V_{CC} = V_{CC(max)}$) (mA)	Don't Care	-	8	
I_{CC6}	$\overline{CAS}$-BEFORE-$\overline{RAS}$, REFRESH CURRENT: Average Power Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Mode ($\overline{RAS}$,$\overline{CAS}$ Cycling@$t_{RC}=t_{RC(min)}$, $V_{CC} = V_{CC(max)}$)(mA)	60 ns	-	1120	3,4,5,6,16, 31
		70 ns	-	1040	
I_{LI}	INPUT LEAKAGE CURRENT: Input Leakage Current, any input ($0 \le V_{IN} \le V_{CC}$, all other pins not under test=0V, $V_{CC} = V_{CC(max)}$) (μA)	**A0~A11**	-40	40	
		$\overline{RAS0}$,$\overline{RAS2}$	-40	40	
		$\overline{CAS0}$~$\overline{CAS3}$	-10	10	
		$\overline{WE}$	-40	40	
		$\overline{OE}$	-40	40	
I_{LO}	OUTPUT LEAKAGE CURRENT: (Data Out is disabled (Hi-Z), $0 \le V_{OUT} \le V_{CC}$)(μA)		-5	5	
V_{OH}	OUTPUT HIGH LEVEL: Output "H" Level Voltage (I_{OUT}=-5mA) (V)		2.4	-	2
V_{OL}	OUTPUT LOW LEVEL: Output "L" Level Voltage (I_{OUT}=+4.2mA) (V)		-	0.4	2

AC CHARACTERISTICS

READ, WRITE, AND REFRESH CYCLES (COMMON PARAMETERS)

(Recommended operating conditions unless otherwise noted.) (Note 8,18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Random READ or WRITE Cycle Time (ns)	104	-	124	-	
t_{RP}	$\overline{\text{RAS}}$ Precharge Time (ns)	40	-	50	-	
t_{CP}	$\overline{\text{CAS}}$ Precharge Time (ns)	10	-	10	-	
t_{RAS}	$\overline{\text{RAS}}$ Pulse Width (ns)	60	10000	70	10000	23
t_{CAS}	$\overline{\text{CAS}}$ Pulse Width (ns)	10	10000	15	10000	23
t_{ASR}	Row Address Setup Time (ns)	0	-	0	-	22
t_{RAH}	Row Address Hold Time (ns)	10	-	10	-	
t_{ASC}	Column Address Setup Time (ns)	0	-	0	-	22
t_{CAH}	Column Address Hold Time (ns)	10	-	15	-	22
t_{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time (ns)	20	45	20	50	10
t_{RAD}	$\overline{\text{RAS}}$ to Col. Address Delay Time (ns)	15	30	15	35	15,23
t_{RSH}	$\overline{\text{RAS}}$ Hold Time (ns)	15	-	20	-	22
t_{CSH}	$\overline{\text{CAS}}$ Hold Time (ns)	45	-	50	-	
t_{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time (ns)	5	-	5	-	22
t_{RPC}	$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ hold Time (ns)	5	-	5	-	22
t_{T}	Transition Time (Rise and Fall) (ns)	2	50	2	50	22
t_{AR}	Column Address Hold Time Referenced to $\overline{\text{RAS}}$ (ns)	-	-	-	-	

READ CYCLES (Note 8,18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t_{RAC}	Access Time from $\overline{RAS}$ (ns)	-	60	-	70	9,10,15,30
t_{CAC}	Access Time from $\overline{CAS}$ (ns)	-	15	-	20	9,10,30
t_{AA}	Access Time from Address (ns)	-	30	-	35	9,15,30
t_{RCS}	Read Command Setup Time (ns)	0	-	0	-	22
t_{RCH}	Read Command Hold Time to $\overline{CAS}$ (ns)	0	-	0	-	14,22
t_{RRH}	Read Command Hold Time to $\overline{RAS}$ (ns)	0	-	0	-	14,22
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time(ns)	30	-	35	-	22
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z (ns)	3	-	3	-	9,22
t_{DZC}	Data to $\overline{CAS}$ Low Delay Time (ns)	-	-	-	-	

WRITE CYCLES (Note 8,18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t_{WCS}	Write Command Set Up Time (ns)	0	-	0	-	13
t_{WCH}	Write Command Hold Time (ns)	10	-	15	-	
t_{WP}	Write Command Pulse Width (ns)	10	-	15	-	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time (ns)	15	-	20	-	22
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time (ns)	10	-	15	-	
t_{DS}	D_{IN} Setup Time (ns)	0	-	0	-	25
t_{DH}	D_{IN} Hold Time (ns)	10	-	15	-	22,25
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$ (ns)	-	-	-	-	
t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$ (ns)	-	-	-	-	

EXTENDED DATA OUT MODE CYCLES (Note 8,9,18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t_{HPC}	EDO Mode Cycle Time (ns)	25	-	30	-	22
t_{RASP}	EDO Mode $\overline{\text{RAS}}$ Pulse Width (ns)	60	200000	70	200000	
t_{HCAS}	EDO MODE $\overline{\text{CAS}}$ Pulse Width (ns)	10	10000	15	10000	22
t_{CPRH}	$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge (ns)	35	-	40	-	22
t_{CPA}	Access Time from $\overline{\text{CAS}}$ Precharge (ns)	-	35	-	40	21,22,30
t_{WPZ}	EDO Mode Write Command Pulse Width (ns)	10	-	15	-	22
t_{DOH}	D_{OUT} Hold Time (ns)	5	-	5	-	22
t_{WHZ}	Output Buffer Turn-Off Delay from $\overline{\text{WE}}$ (ns)	3	15	3	20	12,22
t_{CPW}	$\overline{\text{WE}}$ Delay Time From $\overline{\text{CAS}}$ Precharge (ns)	54	-	64	-	

REFRESH CYCLE (Note 8,18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t_{CHR}	$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh Cycle) (ns)	10	-	15	-	22
t_{CSR}	$\overline{\text{CAS}}$ Setup Time ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh Cycle) (ns)	10	-	10	-	22
t_{WRP}	$\overline{\text{WE}}$ Setup Time ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh Cycle) (ns)	10	-	10	-	22
t_{WRH}	$\overline{\text{WE}}$ Hold Time ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh Cycle) (ns)	10	-	10	-	22
t_{REF}	Refresh Period (4096 cycles) (ms)	-	64	-	64	

NOTES

1. Permanent damage to the device may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. All voltages referenced to V_{SS}.

3. I_{CC} is specified as an average current.

4. This parameter depends on output loading and/or cycle rates.

5. Specified values are obtained with the output open.

6. Address can be changed a maximum of once while $\overline{RAS}=V_{IL}$.

7. Address can be changed a maximum of once while $\overline{CAS}=V_{IH}$.

8. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition time (t_T) is measured between $V_{IH(min)}$ and $V_{IL(max)}$, and is assumed to be 2ns for all inputs. All input signals must transit between V_{IH} and V_{IL} (or V_{IL} and V_{IH}) without slope reversal.

9. Measured with a load equivalent to 2 TTL loads and 100pF.

10. Operation within the $t_{RCD(max)}$ limit ensures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.

11. Assumes that $t_{RAD} \le t_{RAD(max)}$.

12. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

13. This is a non-restrictive operating parameter. It is included in the data sheet as an electrical characteristic only. If $t_{WCS} \ge t_{WCS(min)}$ the cycle is an early write cycle and the data out pins will remain high impedance (open circuit) for the duration of the cycle. If $t_{CWD(min)} \ge t_{CWD(min)}$, $t_{RWD} > t_{RWD(min)}$, $t_{AWD} \ge t_{AWD(min)}$, and $t_{CPW} > t_{CPW(min)}$ (for Fast Page Mode cycle only), then the cycle is a Read-Modify-Write cycle and the data output pins will hold the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out (at access time) is indeterminate.

14. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

15. Operation within the $t_{RAD(max)}$ limit ensures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled exclusively by t_{AA}.

16. Specified values are obtained with minimum cycle time.

17. Specified values are obtained with T_A=25°C.

18. An initial pause of 200µs is required after power-up followed by a minimum of eight initialization cycles (any 8 $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ or $\overline{\text{RAS}}$-only Refresh cycles with $\overline{\text{WE}}$ high) before proper device operation is assured. Also, any 8 $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ or $\overline{\text{RAS}}$-only Refresh cycles with $\overline{\text{WE}}$ high are required after prolonged periods (greater than t_{REF}) of $\overline{\text{RAS}}$ inactivity before proper device operation is assured.

19. Measured with a load equivalent to 50pF and 500 ohms.

20. Write cycle is applicable instead of read cycle. Timing requirements for $\overline{\text{RAS}}$,$\overline{\text{CAS}}$ and Address are the same for Hidden Refresh Write Cycle as that shown for Hidden Refresh Read Cycle. $\overline{\text{WE}}$, D_{IN} and D_{OUT} for Hidden Refresh Write Cycle are the same as for Write Cycle.

21. t_{CPA} is access time from $\overline{\text{CAS}}$ precharge (that is caused by changing $\overline{\text{CAS}}$ from "L" to "H"). Therefore, if t_{CP} is long, then t_{CPA} is longer than $t_{CPA(max)}$.

22. Calculated based on data supplied by the DRAM manufacturer(s).

23. Maximum value is calculated based on data supplied by the DRAM manufacturer(s).

24. Minimum value is calculated based on data supplied by the DRAM manufacturer(s).

25. This parameter is referenced to the $\overline{\text{CAS}}$ leading edge in Early Write cycles and to the WE leading edge in Read-Modify-Write cycles.

26. $V_{IN} = 0$ Volt.

27. Either t_{CDD} or t_{ODD} must be satisfied.

28. Either t_{DZC} or t_{DZO} must be satisfied.

29. $t_{RASP(MIN)}$ is specified as two cycles of $\overline{\text{CAS}}$ input are performed.

30. The access time is limited by all four parameters t_{RAC}, t_{CAC}, t_{AA}, t_{CPA}.

31. This assumes all $\overline{\text{RAS}}$ (and all $\overline{\text{CAS}}$ for CBR refresh) are active.

For Timing Diagrams see **"EDO Timing Diagrams"** (Document No. **20431C**).

Available from fax-on-demand and Website: **http://www.celestica.com/memory/**

Celestica Inc. 1996
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