



# SILEGO

# SLG59M603V

## Ultra-small 22 mΩ 4 A Load Switch with Discharge and Reverse Current Blocking

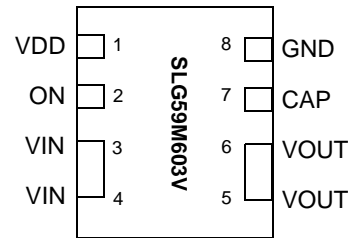
### General Description

The SLG59M603V is a 22 mΩ 4 A single-channel load switch that is able to switch 1 to 5 V power rails. The product is packaged in an ultra-small 1.5 x 2.0 mm package.

### Features

- 1.5 x 2.0 mm FC-TDFN 8L package (2 fused pins for drain and 2 fused pins for source)
- Logic level ON pin capable of supporting 0.85 V CMOS Logic
- User selectable ramp rate with external capacitor
- 22 mΩ RDS<sub>ON</sub> while supporting 4 A
- Discharges load when off
- Pb-Free / Halogen-Free / RoHS compliant
- Operating Temperature: -20 °C to 70°C
- Operating Voltage: 1.5 V to 5.5 V

### Pin Configuration

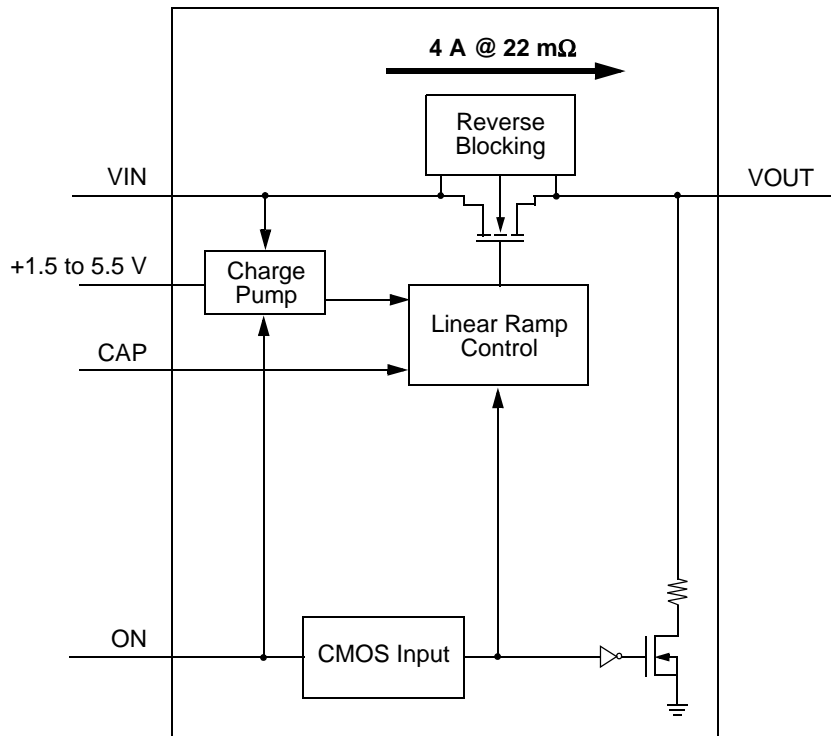


8-pin FC-TDFN (Top View)

### Applications

- Notebook Power Rail Switching
- Tablet Power Rail Switching
- Smartphone Power Rail Switching

### Block Diagram



Preliminary



### Pin Description

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	VDD power for load switch control (1.5 V to 5.5 V)
2	ON	Input	Turns MOSFET ON (4 M $\Omega$ pull down resistor) CMOS input with VIL < 0.3 V, VIH > 0.85 V
3	VIN	MOSFET	Drain of Power MOSFET (fused with pin 4)
4	VIN	MOSFET	Drain of Power MOSFET (fused with pin 3)
5	VOUT	MOSFET	Source of Power MOSFET (fused with pin 6)
6	VOUT	MOSFET	Source of Power MOSFET (fused with pin 5)
7	CAP	Input	Capacitor for controlling power rail ramp rate
8	GND	GND	Ground

### Ordering Information

Part Number	Type	Production Flow
SLG59M603V	FC-TDFN 8L	Commercial, -20 °C to 70 °C
SLG59M603VTR	FC-TDFN 8L (Tape and Reel)	Commercial, -20 °C to 70 °C



## Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$V_{DD}$	Power Supply		--	--	7	V
$T_S$	Storage Temperature		-65	--	150	°C
$ESD_{HBM}$	ESD Protection	Human Body Model	2000	--	--	V
$W_{DIS}$	Package Power Dissipation		--	--	1	W
MOSFET $IDS_{PK}$	Peak Current from Drain to Source	For no more than 1 ms with 1% duty cycle	--	--	6	A

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Electrical Characteristics

$T_A = -20$  to  $70$  °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$V_{DD}$	Power Supply Voltage	-20 to 70°C	1.5	--	5.5	V
$I_{DD}$	Power Supply Current (PIN 1)	when OFF	--	--	1	μA
		when ON, No load	--	70	100	μA
$RDS_{ON}$	Static Drain to Source ON Resistance	$T_A$ 25°C @ 100 mA	--	22	--	mΩ
		$T_A$ 70°C @ 100 mA	--	TBD	--	mΩ
$IDS$	Operating Current	$V_{IN} = 1.0$ V to 5.5 V	--	--	4	A
$V_{IN}$	Drain Voltage		1.0	--	$V_{DD}$	V
$T_{ON\_Delay}$	ON pin Delay Time	50% ON to Ramp Begin	0	300	500	μs
$T_{Total\_ON}$	Total Turn On Time	50% ON to 90% $V_{OUT}$	Configurable <sup>1</sup>			ms
		Example: CAP (PIN 7) = 4 nF, $V_{DD} = V_{IN} = 5$ V, Source_Cap = 10 μF, $IDS = 100$ mA	--	1.96	--	ms
$T_{SLEWRATE}$	Slew Rate	10% $V_S$ to 90% $V_S$	Configurable <sup>1</sup>			V/ms
		Example: CAP (PIN 7) = 4 nF, $V_{DD} = V_{IN} = 5$ V, Source_Cap = 10 μF, $IDS = 100$ mA	--	3.0	--	V/ms
$I_{REVERSE}$	Reverse Blocking Current	$V_{OUT} = 5.0$ , $V_{IN} = 0$ V	--	--	3	μA
$CAP_{SOURCE}$	Source Cap	Source to GND	--	--	500	μF
ON_ $V_{IH}$	High Input Voltage on ON pin		0.85	--	$V_{DD}$	V
ON_ $V_{IL}$	Low Input Voltage on ON pin		-0.3	0	0.3	V
$T_{OFF\_Delay}$	OFF Delay Time	50% ON to $V_{OUT}$ Fall, $V_{DD} = V_{IN} = 5$ V	--	--	15	μs
$T_{FALL}$	$V_{OUT}$ Fall Time	90% $V_{OUT}$ to 10% $V_{OUT}$ , $V_{DD} = V_{IN} = 5$ V	--	TBD	--	μs

Notes:

1. Refer to table for configuration details.



### **SLG59M603V Turn ON**

The normal power on sequence is first VDD, with VIN only being applied after VDD is  $> 1$  V, and then ON after VIN is at least 90% of final value. The normal power off sequence is the power on sequence in reverse.

If VDD and VIN are turned on at the same time then it is possible that a voltage glitch will appear on VOUT before VDD achieves 1V which is the  $V_T$  of the main MOSFET. The size of the glitch is dependent on source and drain capacitance loading and the ramp rate of VDD & VIN.

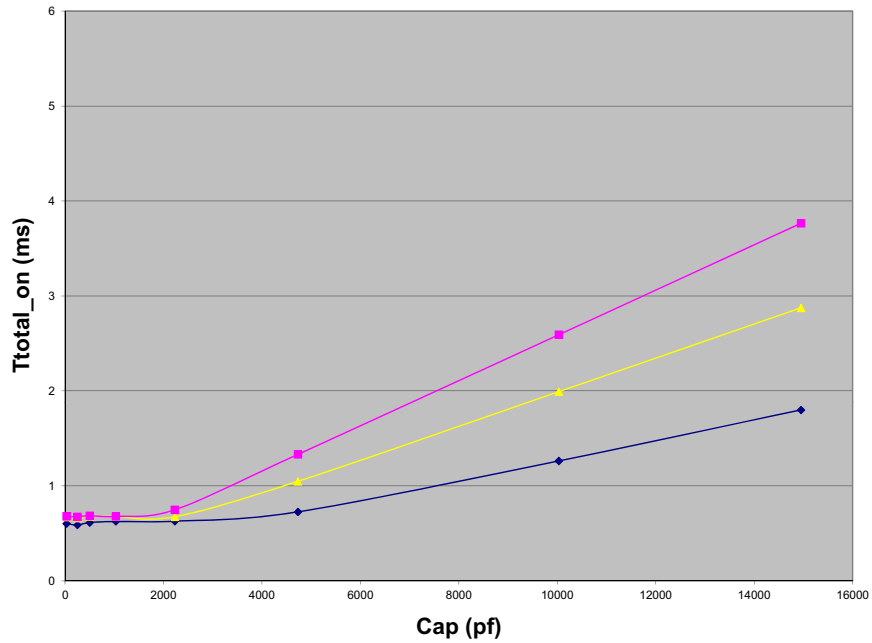
### **SLG59M603V Turn ON**

The VOUT ramp follows a linear path, not an RC limitation provided the ramp is slow enough to not be current limited by load capacitance.



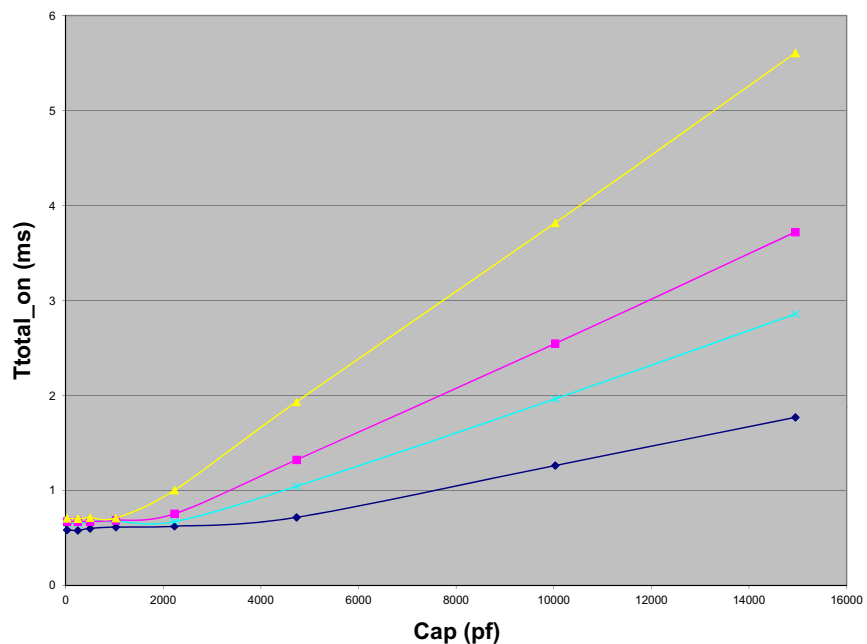
### T<sub>Total\_ON</sub> vs. CAP @ V<sub>DD</sub> = 3.3 V

SLG59M603V T<sub>Total\_ON</sub>: ON (50%) - V<sub>OUT</sub> (90%)  
V<sub>DD</sub> = 3.3 V, T<sub>A</sub> = 25 °C. C<sub>L</sub> = 10 μF, I<sub>DS</sub> = 100 mA



### T<sub>Total\_ON</sub> vs. CAP @ V<sub>DD</sub> = 5.0 V

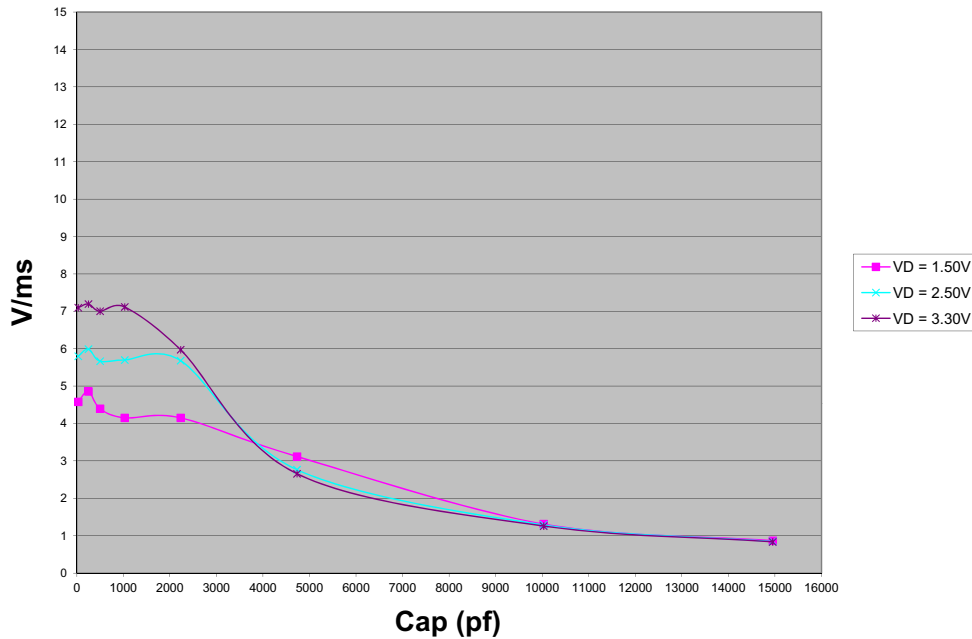
SLG59M603V T<sub>Total\_ON</sub>: ON (50%) - V<sub>OUT</sub> (90%)  
V<sub>DD</sub> = 5.0 V, T<sub>A</sub> = 25 °C. C<sub>L</sub> = 10 μF, I<sub>DS</sub> = 100 mA





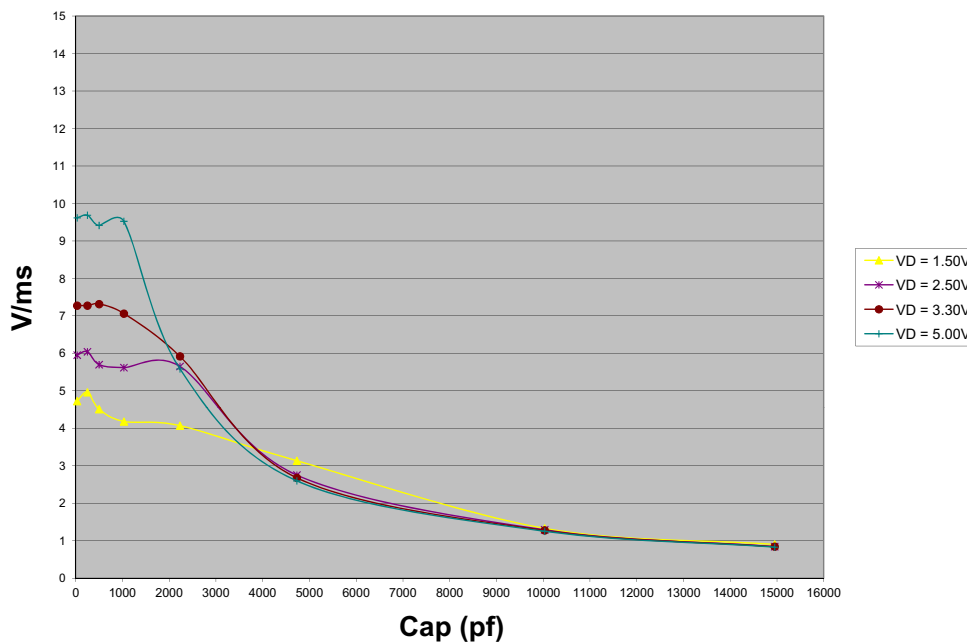
### $T_{SLEW}$ vs. CAP @ $V_{DD} = 3.3\text{ V}$

SLG59M603V  $T_{SLEW}$ :  $V_{OUT}$  (10%) -  $V_{OUT}$  (90%)  
 $V_{DD} = 3.3\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$ ,  $C_L = 10\text{ }\mu\text{F}$ ,  $I_{DS} = 100\text{ mA}$



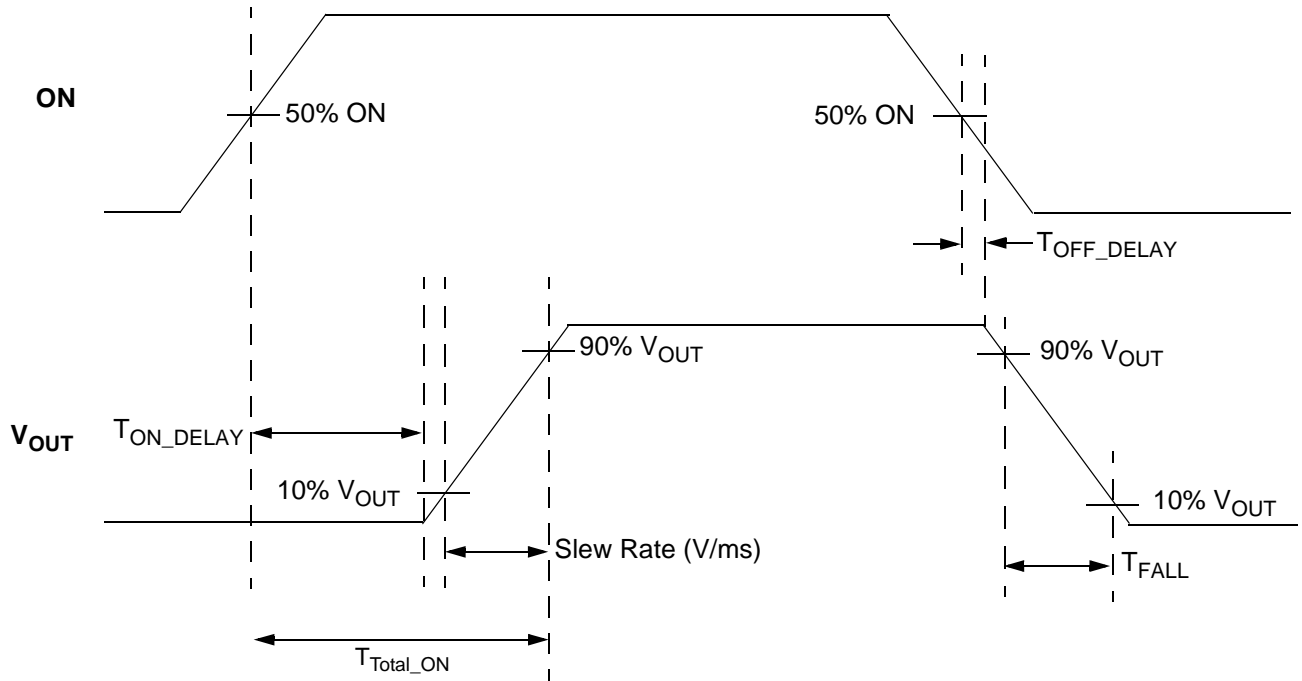
### $T_{SLEW}$ vs. CAP @ $V_{DD} = 5.0\text{ V}$

SLG59M603V  $T_{SLEW}$ :  $V_{OUT}$  (10%) -  $V_{OUT}$  (90%)  
 $V_{DD} = 5.0\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$ ,  $C_L = 10\text{ }\mu\text{F}$ ,  $I_{DS} = 100\text{ mA}$



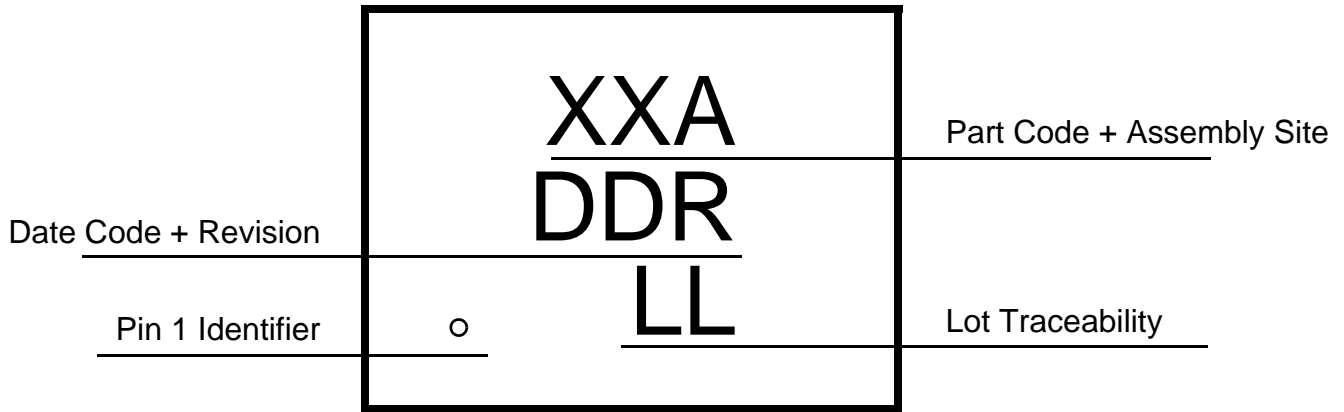


$T_{Total\_ON}$ ,  $T_{ON\_Delay}$  and Slew Rate Measurement





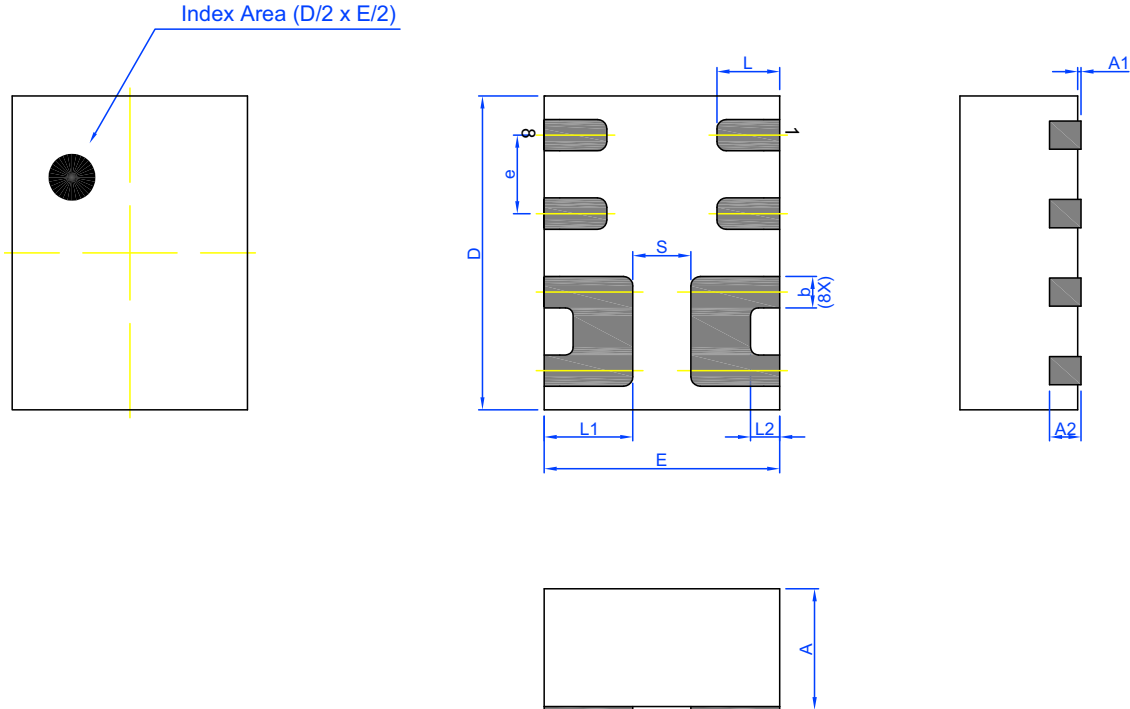
Package Top Marking System Definition





**Package Drawing and Dimensions**

8 Lead TDFN Package 1.5 x 2.0 mm (Fused Lead)  
JEDEC MO-252, Variation W2015D



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.70	0.75	0.80	L	0.35	0.40	0.45
A1	0.005	-	0.060	L1	0.515	0.565	0.615
A2	0.15	0.20	0.25	L2	0.135	0.185	0.235
b	0.15	0.20	0.25	e	0.50 BSC		
D	1.95	2.00	2.05	S	0.37 REF		
E	1.45	1.50	1.55				

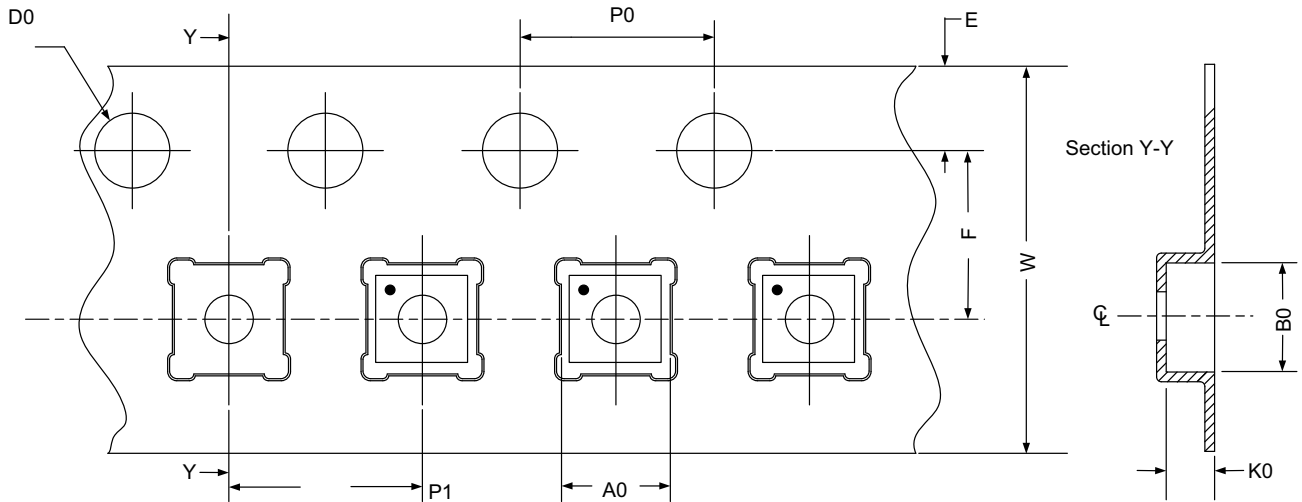


**Tape and Reel Specifications**

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
TDFN 8L FC Green	8	1.5 x 2.0 x 0.75	3000	3000	178 / 60	100	400	100	400	8	4

**Carrier Tape Drawing and Dimensions**

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
TDFN 8L FC Green	1.68	2.18	0.9	4	4	1.5	1.75	3.5	8



Refer to EIA-481 specification

**Recommended Reflow Soldering Profile**

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.25 mm<sup>3</sup> (nominal). More information can be found at [www.jedec.org](http://www.jedec.org).