

8-Bit Serial-Input Protected Latched Driver

General Description

The MIC58P42 serial-input latched driver is a high-voltage (80V), high-current (500mA) integrated circuit comprised of eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common STROBE, CLOCK, SERIAL DATA INPUT, and OUTPUT ENABLE functions. Similar to the MIC5842, additional protection circuitry supplied on this device includes thermal shutdown, under voltage lockout (UVLO), and over-current shutdown.

The bipolar/CMOS combination provides an extremely low-power latch with maximum interface flexibility. The MIC58P42 has open-collector outputs capable of sinking 500 mA and integral diodes for inductive load transient suppression with a minimum output breakdown voltage rating of 80V (50V sustaining). The drivers can be operated with a split supply, where the negative supply is down to -20V and may be paralleled for higher load current capability.

With a 5V logic supply, the MIC58P42 will typically operate at better than 5MHz. With a 12V logic supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL circuits may require pull-up resistors. By using the serial data output, drivers may be cascaded for interface applications requiring additional drive lines.

Each of these eight outputs has an independent over current shutdown of 500 mA. Upon over-current detection, the affected channel will turn OFF until V_{DD} is cycled or the ENABLE/RESET pin is pulsed high. Current pulses less than 2 μ s will not activate current shutdown. Temperatures above 165°C will shut down the device. The UVLO circuit prevents operation at low V_{DD} ; hysteresis of 0.5V is provided. See the MIC59P60 for a similar device that additionally provides an error flag output.

Features

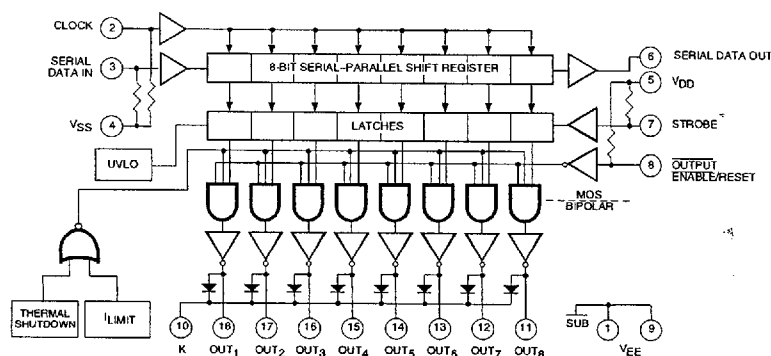
- 3.3 MHz Minimum Data-Input Rate
- CMOS, PMOS, NMOS, and TTL Compatible
- Internal Pull-Up/Pull-Down Resistors
- Low Power CMOS Logic and Latches
- High Voltage (80V) Current-Sink Outputs
- Output Transient-Protection Diodes
- Single or Split Supply Operation
- Thermal Shutdown
- Under-Voltage Lockout
- Per-Output Over-Current Shutdown (500mA typical)

Ordering Information

Part Number	Temperature Range	Package
MIC58P42AJ	-55°C to +125°C	18-Pin Ceramic DIP
MIC58P42AJB†	-55°C to +125°C	18-Pin Ceramic DIP
MIC58P42BN	-40°C to +85°C	18-Pin Plastic DIP
MIC58P42BV	-40°C to +85°C	20-Pin PLCC
MIC58P42BWM	-40°C to +85°C	18-Pin Wide SOIC

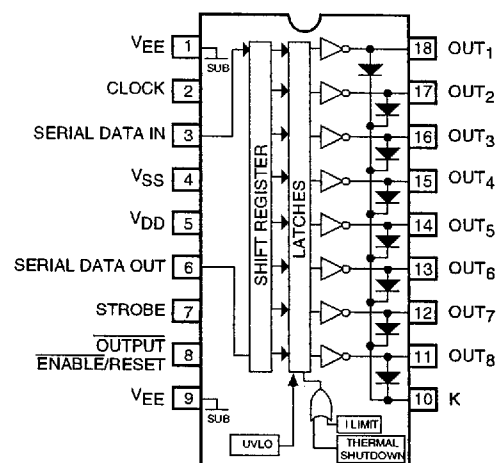
† AJB indicates units screened to MIL-STD 883, Method 5004, condition B, and burned-in for 1 week.

Functional Diagram



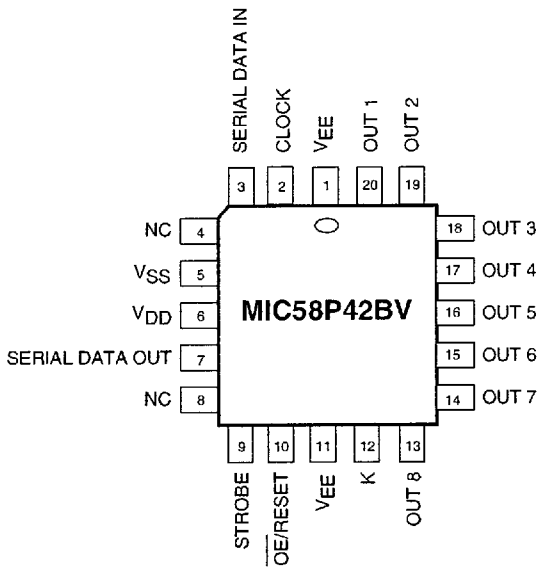
Pin Configuration

(Ceramic and Plastic DIP and SOIC)



6088819 0002106 646

PLCC Pin Configuration



Absolute Maximum Ratings (Note 1, 2)

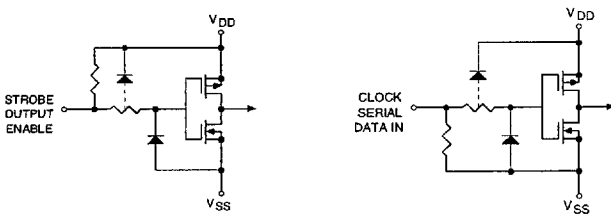
at 25°C Free-Air Temperature and $V_{SS} = 0V$

Output Voltage	80V
Output Voltage, $V_{CE(SUS)}$ (Note 1)	50V
Logic Supply Voltage Range, V_{DD}	4.5V to 15V
V_{DD} with Reference to V_{EE}	25V
Emitter Supply Voltage (Substrate), V_{EE}	-20V
Input Voltage Range, V_{IN}	-0.3V to $V_{DD} + 0.3V$
Package Power Dissipation, P_D	
MIC58P42BN	1.82W
Derate above $T_A = +25^\circ C$	18mW/
MIC58P42AJ/AJB	1.6W
Derate above $T_A = +25^\circ C$	16mW/
MIC58P42BV	1.4
Derate above $T_A = +25^\circ C$	14mW/
MIC58P42BWM	1.2W
Derate above $T_A = +25^\circ C$	12mW/
Operating Temperature Range, T_A	-55°C to +125°C
Storage Temperature Range, T_S	-65°C to +150°C

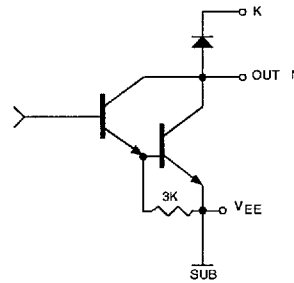
Note 1: For inductive load applications.

Note 2: CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Typical Input Circuits



Typical Output Driver



Pin Description

Pin	Name	Description
(DIP & S.O.)		
1,9	V_{EE}	Substrate. Most Negative voltage in the system connects here.
2	CLOCK	Serial Data Clock. A CLEAR input must also be clocked into the latches.
3	SERIAL DATA IN	Serial Data Input pin.
4	V_{SS}	Logic reference (Ground) pin.
5	V_{DD}	Logic Positive Supply voltage.
6	SERIAL DATA OUT	Serial Data Output pin. (Flow-through).
7	STROBE	Output Strobe pin. Loads output latches when high. Strobe is needed to clear latch.
8	$\overline{\text{OUTPUT ENABLE/RESET}}$	When Low, Outputs are active. When High, device is reset from a fault condition.
10	K	Transient suppression diode's cathode common pin.
11—18	OUTPUT N	Open Collector outputs 8 through 1.

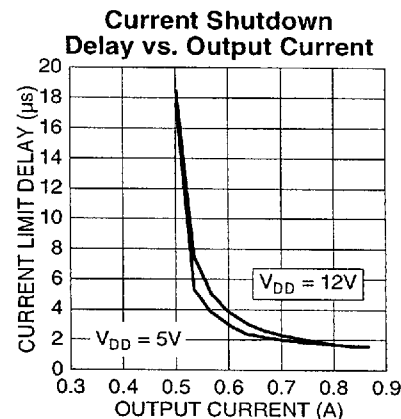
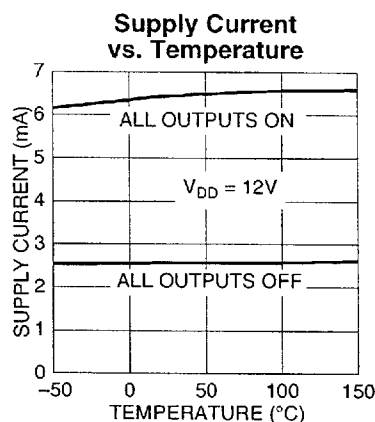
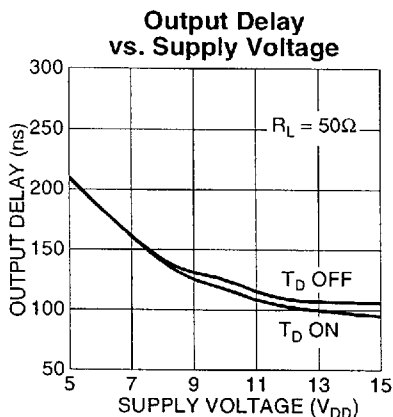
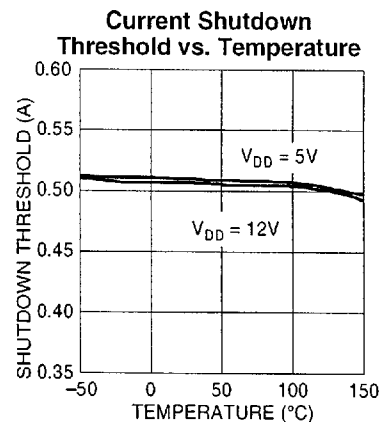
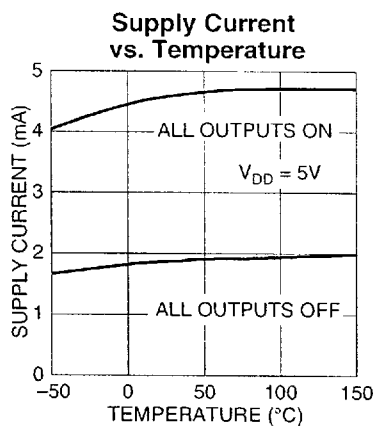
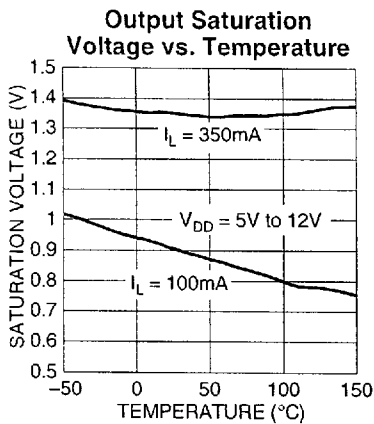
Electrical Characteristics at $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{V}$, $V_{SS} = V_{EE} = 0\text{V}$ (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	$V_{OUT} = 80\text{V}$			50	μA
		$V_{OUT} = 80\text{V}$, $T_A = +70^\circ\text{C}$			100	
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 100\text{mA}$		0.9	1.1	V
		$I_{OUT} = 200\text{mA}$		1.1	1.3	
		$I_{OUT} = 350\text{mA}$		1.3	1.6	
Collector-Emitter Sustaining Voltage	$V_{CE(SUS)}$	$I_{OUT} = 350\text{mA}$, $L = 2\text{mH}$	50			V
Input Voltage	$V_{IN(0)}$				1.0	V
	$V_{IN(1)}$	$V_{DD} = 12\text{V}$		10.5		
		$V_{DD} = 10\text{V}$		8.5		
		$V_{DD} = 5.0\text{V}$, Note 1		3.5		
Input Resistance	R_{IN}	$V_{DD} = 12\text{V}$	50	200		$\text{k}\Omega$
		$V_{DD} = 10\text{V}$	50	300		
		$V_{DD} = 5.0\text{V}$	50	600		
Supply Current	$I_{DD(ON)}$	All Drivers ON, $V_{DD} = 12\text{V}$		6.4	10.0	mA
		All Drivers ON, $V_{DD} = 10\text{V}$		6.0	9.0	
		All Drivers ON, $V_{DD} = 5.0\text{V}$		4.6	7.5	
	$I_{DD(1\text{ ON})}$	One Driver ON, All others OFF, $V_{DD} = 12\text{V}$		3.1	4.5	
		One Driver ON, All others OFF, $V_{DD} = 10\text{V}$		2.9	4.5	
		One Driver ON, All others OFF, $V_{DD} = 5\text{V}$		2.3	3.6	
	$I_{DD(OFF)}$	All Drivers OFF, $V_{DD} = 12\text{V}$		2.6	4.2	
		All Drivers OFF, $V_{DD} = 10\text{V}$		2.4	3.6	
		All Drivers OFF, $V_{DD} = 5.0\text{V}$		1.9	3.0	
Clamp Diode Leakage Current	I_R	$V_R = 80\text{V}$			50	μA
Clamp Diode Forward Voltage	V_F	$I_F = 350\text{mA}$		1.7	2.0	V
Output Current Shutdown Threshold	I_{LIM}			500		mA
Start Up Voltage	V_{SU}	Note 2	3.5	4.0	4.5	V
Minimum Supply (V_{DD})	$V_{DD\text{ MIN}}$		3.0	3.5	4.0	V
Thermal Shutdown				165		$^\circ\text{C}$
Thermal Shutdown Hysteresis				10		$^\circ\text{C}$

Note 1: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".

Note 2: Undervoltage Lockout is guaranteed to release device at no more than 4.5V, and disable the device at no less than 3.0V.

Typical Characteristic Curves



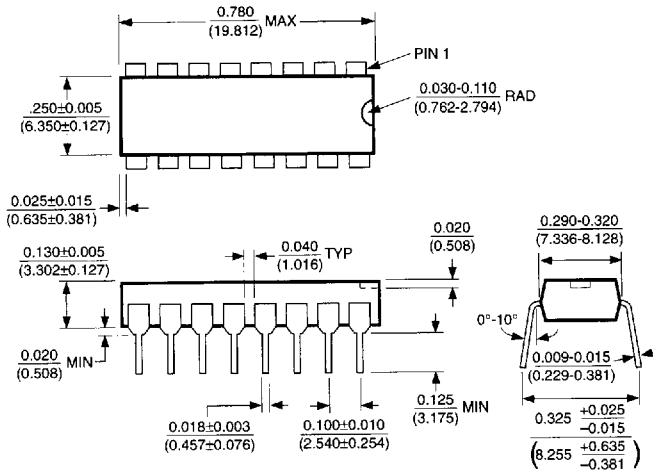
Maximum Allowable Duty Cycle, Plastic DIP

V_{DD} = 5.0V

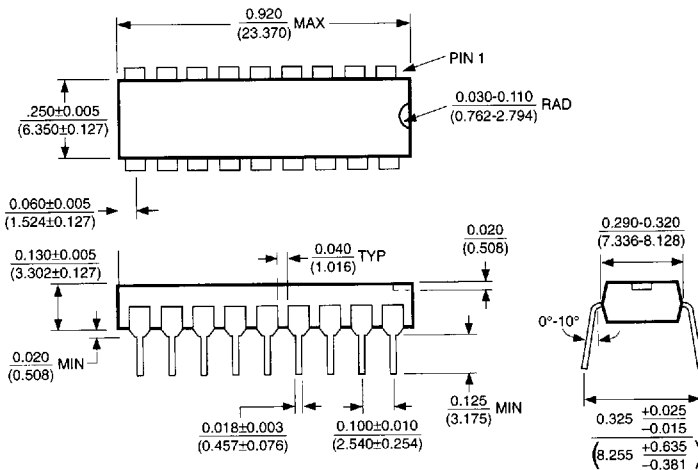
Number of Outputs ON (I _{OUT} = 200mA V _{DD} = 5.0V)	Max. Allowable Duty Cycle at Ambient Temperature of:				
	25°C	40°C	50°C	60°C	70°C
8	85%	72%	64%	55%	46%
7	97%	82%	73%	63%	53%
6	100%	96%	85%	73%	62%
5	100%	100%	100%	88%	75%
4	100%	100%	100%	100%	93%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

V_{DD} = 12V

Number of Outputs ON (I _{OUT} = 200mA V _{DD} = 12V)	Max. Allowable Duty Cycle at Ambient Temperature of:				
	25°C	40°C	50°C	60°C	70°C
8	80%	68%	60%	52%	44%
7	91%	77%	68%	59%	50%
6	100%	90%	79%	69%	58%
5	100%	100%	95%	82%	69%
4	100%	100%	100%	100%	86%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

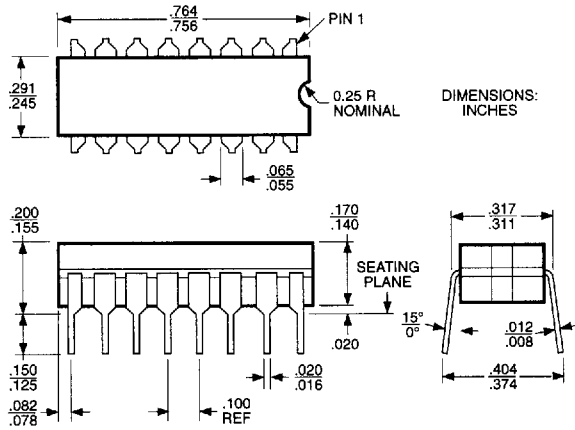


16-Pin Plastic DIP (N)

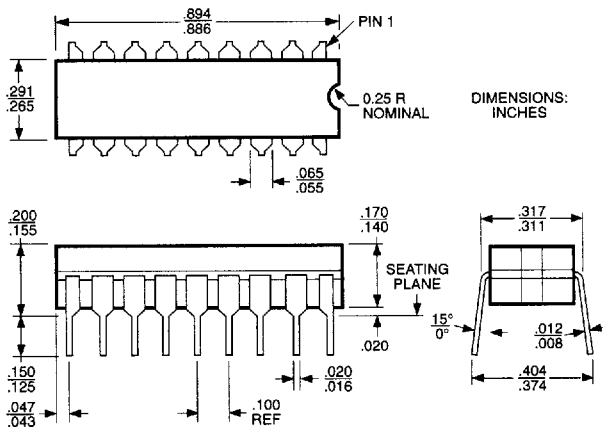


18-Pin Plastic DIP (N)

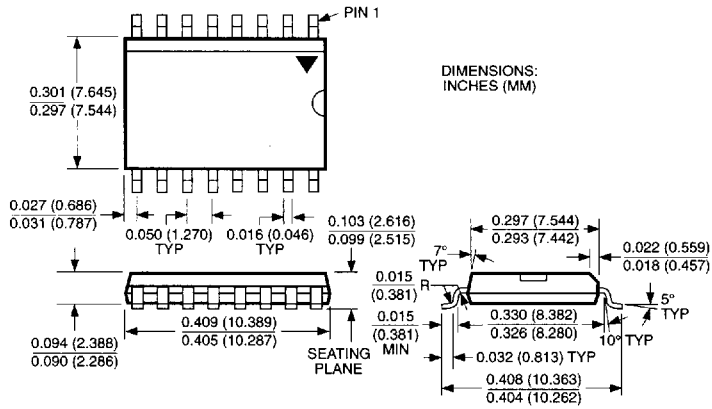
Note: Pin 1 is denoted by one or more of the following: a notch, a printed triangle, or a mold mark.



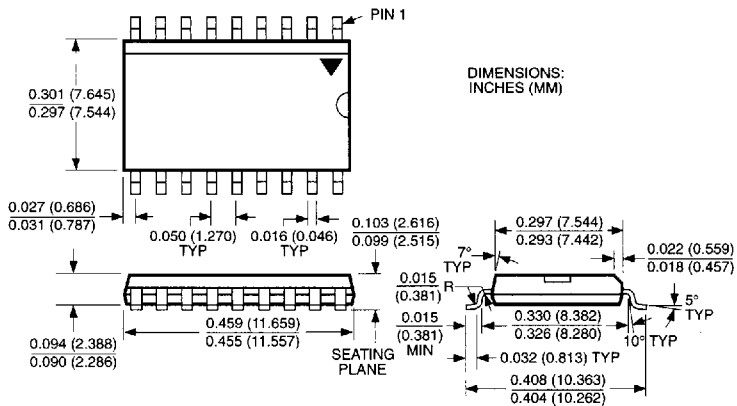
16-Pin Ceramic DIP (J)



18-Pin Ceramic DIP (J)

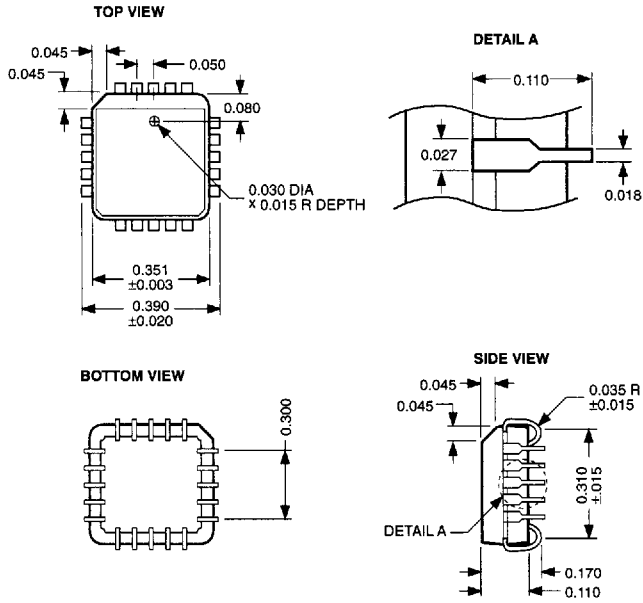


16-Pin Wide SOIC (WM)

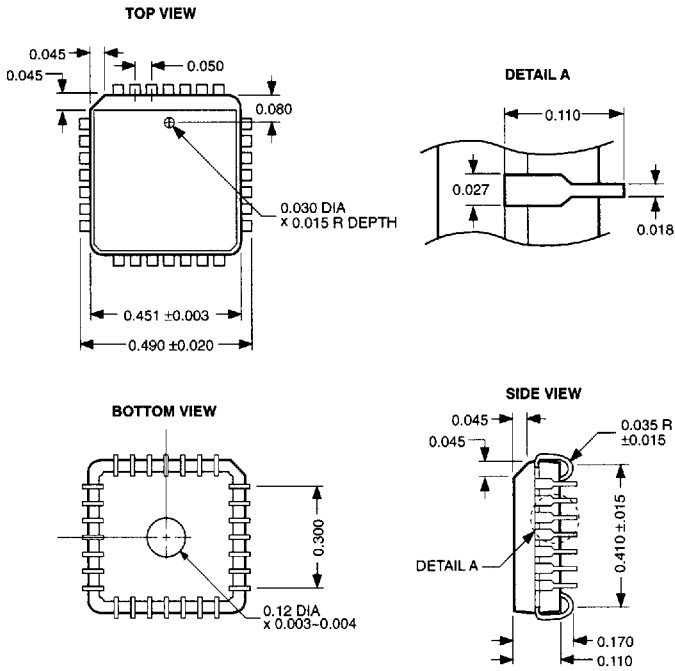


18-Pin Wide SOIC (WM)

Note: Pin 1 is denoted by one or more of the following: a notch, a printed triangle, or a mold mark.



20-Pin PLCC (V)



28-Pin PLCC (V)