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# HM5164400A Series HM5165400A Series

16777216-word × 4-bit Dynamic RAM

# HITACHI

ADE-203-490A (Z)  
Rev. 1.0  
Aug. 29, 1997

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## Description

The Hitachi HM5164400A Series, HM5165400A Series are CMOS dynamic RAMs organized as 16,777,216-word × 4-bit. They employ the most advanced CMOS technology for high performance and low power. The HM5164400A Series, HM5165400A Series offer Fast Page Mode as a high speed access mode. They have the package variations of standard 400-mil 32-pin plastic SOJ and standard 400-mil 32-pin plastic TSOPII.

## Features

- Single 3.3 V ( $\pm 0.3$  V)
- Access time: 50 ns/60 ns/70 ns (max)
- Power dissipation
  - Active mode : TBD/378 mW/324 mW (max) (HM5164400A Series)  
: TBD/558 mW/486 mW (max) (HM5165400A Series)
  - Standby mode : 7.2 mW (max)  
: TBD (L-version)
- Fast page mode capability
- Refresh cycles
  - $\overline{\text{RAS}}$ -only refresh  
8192 cycles/64 ms (HM5164400A)  
4096 cycles/64 ms (HM5165400A)  
/128 ms (HM5165400AL) (L-version)
  - CBR/Hidden refresh  
4096 cycles/64 ms (HM5164400A, HM5165400A)  
/128 ms (HM5165400AL) (L-version)
- 4 variations of refresh
  - $\overline{\text{RAS}}$ -only refresh
  - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh
  - Hidden refresh
  - Self refresh (L-version)

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## HM5164400A Series, HM5165400A Series

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- Battery backup operation (L-version)

### Ordering Information

Type No.	Access time	Package
HM5164400AJ-5	50 ns	400-mil 32-pin plastic SOJ (CP-32DC)
HM5164400AJ-6	60 ns	
HM5164400AJ-7	70 ns	
HM5164400ALJ-5	50 ns	
HM5164400ALJ-6	60 ns	
HM5164400ALJ-7	70 ns	
HM5165400AJ-5	50 ns	
HM5165400AJ-6	60 ns	
HM5165400AJ-7	70 ns	
HM5165400ALJ-5	50 ns	
HM5165400ALJ-6	60 ns	
HM5165400ALJ-7	70 ns	
HM5164400ATT-5	50 ns	400-mil 32-pin plastic TSOP II (TTP-32DC)
HM5164400ATT-6	60 ns	
HM5164400ATT-7	70 ns	
HM5164400ALTT-5	50 ns	
HM5164400ALTT-6	60 ns	
HM5164400ALTT-7	70 ns	
HM5165400ATT-5	50 ns	
HM5165400ATT-6	60 ns	
HM5165400ATT-7	70 ns	
HM5165400ALTT-5	50 ns	
HM5165400ALTT-6	60 ns	
HM5165400ALTT-7	70 ns	

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## HM5164400A Series, HM5165400A Series

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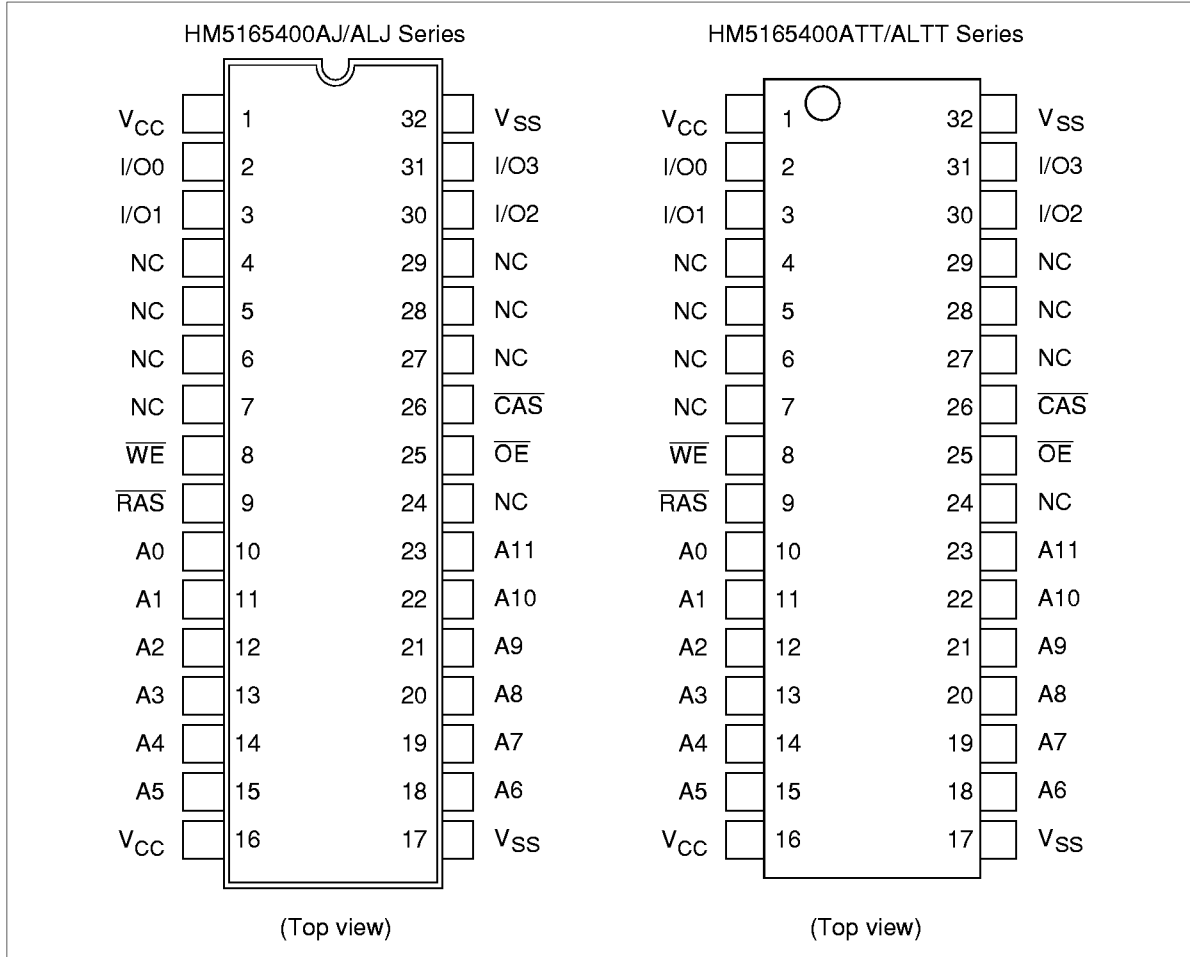
### Pin Description

Pin name	Function
A0 to A12	Address input — Row/Refresh address A0 to A12 — Column address A0 to A10
I/O0 to I/O3	Data input/Data output
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{CAS}}$	Column address strobe
$\overline{\text{WE}}$	Read/Write enable
$\overline{\text{OE}}$	Output enable
V <sub>cc</sub>	Power supply
V <sub>ss</sub>	Ground
NC	No connection

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# HM5164400A Series, HM5165400A Series

## Pin Arrangement



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## HM5164400A Series, HM5165400A Series

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### Pin Description

Pin name	Function
A0 to A11	Address input — Row/Refresh address A0 to A11 — Column address A0 to A11
I/O0 to I/O3	Data input/Data output
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{CAS}}$	Column address strobe
$\overline{\text{WE}}$	Read/Write enable
$\overline{\text{OE}}$	Output enable
V <sub>cc</sub>	Power supply
V <sub>ss</sub>	Ground
NC	No connection

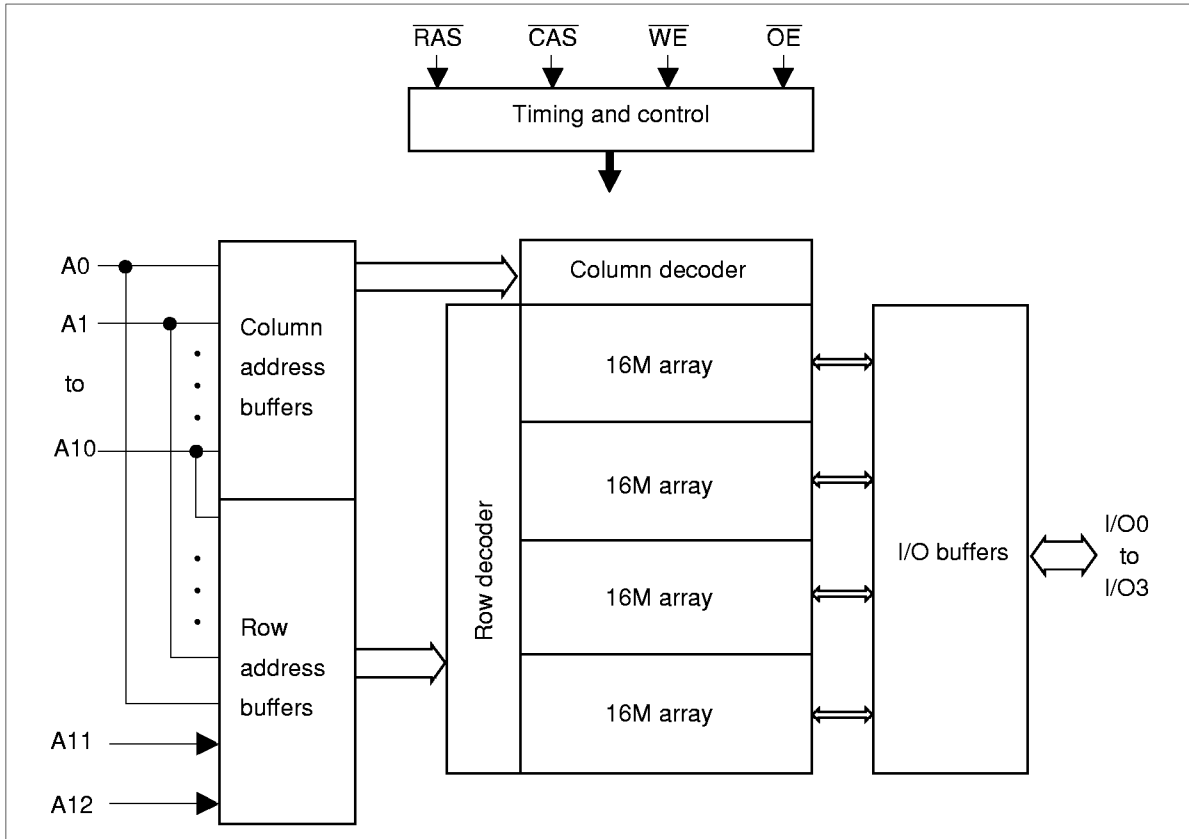
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## HM5164400A Series, HM5165400A Series

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**Block Diagram** (HM5164400A Series)

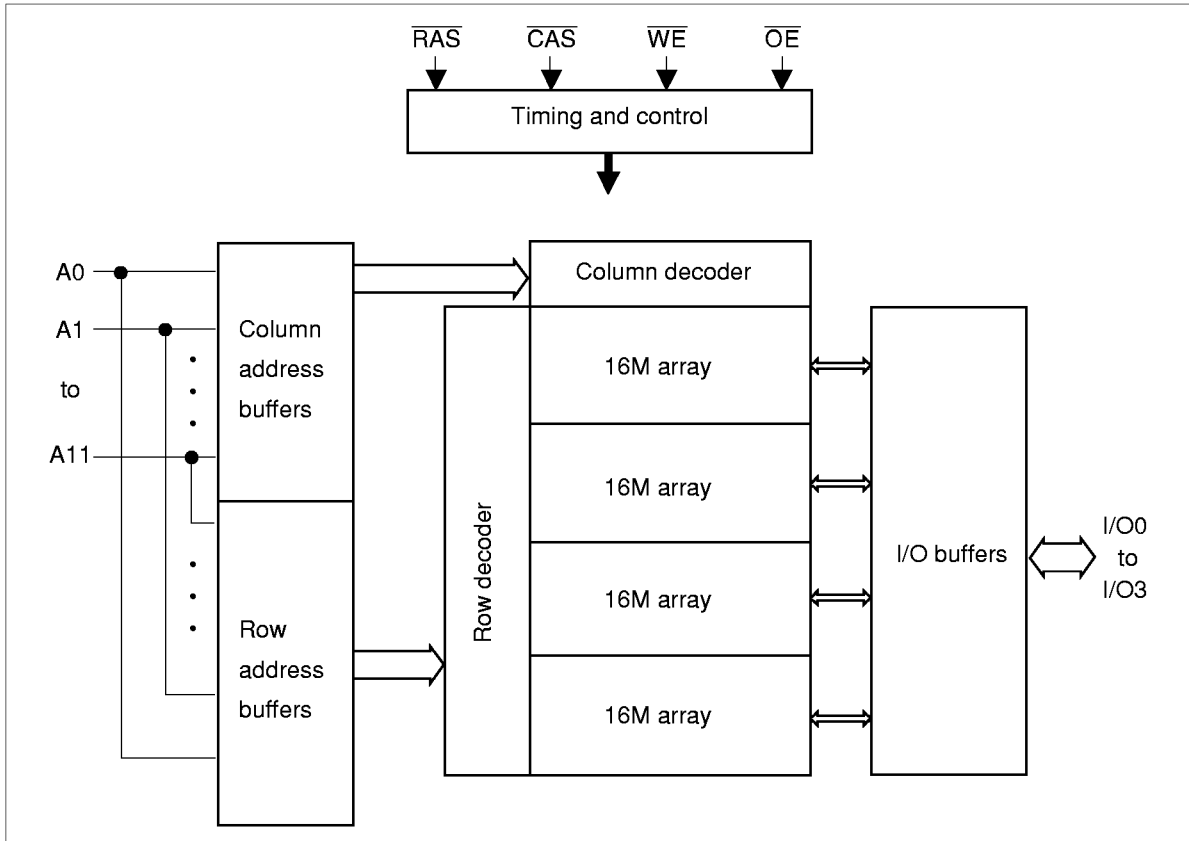


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## HM5164400A Series, HM5165400A Series

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### Block Diagram (HM5165400A Series)



## HM5164400A Series, HM5165400A Series

### Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to $V_{SS}$	$V_T$	-0.5 to $V_{CC} + 0.5$ ( $\leq 4.6$ V (max))	V
Supply voltage relative to $V_{SS}$	$V_{CC}$	-0.5 to +4.6	V
Short circuit output current	$I_{out}$	50	mA
Power dissipation	$P_T$	1.0	W
Operating temperature	$T_{opr}$	0 to +70	°C
Storage temperature	$T_{stg}$	-55 to +125	°C

### Recommended DC Operating Conditions ( $T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	$V_{CC}$	3.0	3.3	3.6	V	1, 2
Input high voltage	$V_{IH}$	2.0	—	$V_{CC} + 0.3$	V	1
Input low voltage	$V_{IL}$	-0.3	—	0.8	V	1

- Notes: 1. All voltage referred to  $V_{SS}$   
 2. The supply voltage with all  $V_{CC}$  pins must be on the same level. The supply voltage with all  $V_{SS}$  pins must be on the same level.

## HM5164400A Series, HM5165400A Series

### DC Characteristics

( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ ) (HM5164400A Series)

Parameter	Symbol	HM5164400A						Unit	Test conditions
		-5		-6		-7			
		Min	Max	Min	Max	Min	Max		
Operating current <sup>*1, *2</sup>	$I_{CC1}$	—	TBD	—	105	—	90	mA	$t_{RC} = \text{min}$
Standby current	$I_{CC2}$	—	TBD	—	2	—	2	mA	TTL interface $\overline{\text{RAS}}, \overline{\text{CAS}} = V_{IH}$ Dout = High-Z
		—	TBD	—	1	—	1	mA	CMOS interface $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$ Dout = High-Z
Standby current (L-version)	$I_{CC2}$	—	TBD	—	TBD	—	TBD	$\mu\text{A}$	CMOS interface $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$ Dout = High-Z
$\overline{\text{RAS}}$ -only refresh current <sup>*2</sup>	$I_{CC3}$	—	TBD	—	105	—	90	mA	$t_{RC} = \text{min}$
Standby current <sup>*1</sup>	$I_{CC5}$	—	TBD	—	5	—	5	mA	$\overline{\text{RAS}} = V_{IH}, \overline{\text{CAS}} = V_{IL}$ Dout = enable
$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh current	$I_{CC6}$	—	TBD	—	140	—	120	mA	$t_{RC} = \text{min}$
Fast page mode current <sup>*1, *3</sup>	$I_{CC7}$	—	TBD	—	80	—	70	mA	$t_{PC} = \text{min}$
Battery backup current <sup>*4</sup> (Standby with CBR refresh) (L-version)	$I_{CC10}$	—	TBD	—	TBD	—	TBD	$\mu\text{A}$	CMOS interface Dout = High-Z, CBR refresh: $t_{RC} = 31.3 \mu\text{s}$ $t_{RAS} \leq 0.3 \mu\text{s}$
Self refresh mode current (L-version)	$I_{CC11}$	—	TBD	—	TBD	—	TBD	$\mu\text{A}$	CMOS interface $\overline{\text{RAS}}, \overline{\text{CAS}} \leq 0.2 \text{ V}$ Dout = High-Z
Input leakage current	$I_{LI}$	TBD	TBD	-10	10	-10	10	$\mu\text{A}$	$0 \text{ V} \leq V_{in} \leq V_{CC} + 0.3 \text{ V}$
Output leakage current	$I_{LO}$	TBD	TBD	-10	10	-10	10	$\mu\text{A}$	$0 \text{ V} \leq V_{out} \leq V_{CC}$ Dout = disable
Output high voltage	$V_{OH}$	TBD	TBD	2.4	$V_{CC}$	2.4	$V_{CC}$	V	High Iout = -2 mA
Output low voltage	$V_{OL}$	TBD	TBD	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes: 1.  $I_{CC}$  depends on output load condition when the device is selected.  $I_{CC}$  max is specified at the output open condition.

2. Address can be changed once or less while  $\overline{\text{RAS}} = V_{IL}$ .

3. Address can be changed once or less within one page mode cycle  $t_{PC}$ .

4.  $V_{IH} \geq V_{CC} - 0.2 \text{ V}$ ,  $0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$ .

## HM5164400A Series, HM5165400A Series

### DC Characteristics

( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ ) (HM5165400A Series)

Parameter	Symbol	HM5165400A						Unit	Test conditions
		-5		-6		-7			
		Min	Max	Min	Max	Min	Max		
Operating current <sup>*1, *2</sup>	$I_{CC1}$	—	TBD	—	155	—	135	mA	$t_{RC} = \text{min}$
Standby current	$I_{CC2}$	—	TBD	—	2	—	2	mA	TTL interface $\overline{\text{RAS}}, \overline{\text{CAS}} = V_{IH}$ Dout = High-Z
		—	TBD	—	1	—	1	mA	CMOS interface $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$ Dout = High-Z
Standby current (L-version)	$I_{CC2}$	—	TBD	—	TBD	—	TBD	$\mu\text{A}$	CMOS interface $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$ Dout = High-Z
$\overline{\text{RAS}}$ -only refresh current <sup>*2</sup>	$I_{CC3}$	—	TBD	—	155	—	135	mA	$t_{RC} = \text{min}$
Standby current <sup>*1</sup>	$I_{CC5}$	—	TBD	—	5	—	5	mA	$\overline{\text{RAS}} = V_{IH}, \overline{\text{CAS}} = V_{IL}$ Dout = enable
$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh current	$I_{CC6}$	—	TBD	—	140	—	120	mA	$t_{RC} = \text{min}$
Fast page mode current <sup>*1, *3</sup>	$I_{CC7}$	—	TBD	—	95	—	85	mA	$t_{PC} = \text{min}$
Battery backup current <sup>*4</sup> (Standby with CBR refresh) (L-version)	$I_{CC10}$	—	TBD	—	TBD	—	TBD	$\mu\text{A}$	CMOS interface Dout = High-Z, CBR refresh: $t_{RC} = 31.3 \mu\text{s}$ $t_{RAS} \leq 0.3 \mu\text{s}$
Self refresh mode current (L-version)	$I_{CC11}$	—	TBD	—	TBD	—	TBD	$\mu\text{A}$	CMOS interface $\overline{\text{RAS}}, \overline{\text{CAS}} \leq 0.2 \text{ V}$ Dout = High-Z
Input leakage current	$I_{LI}$	TBD	TBD	-10	10	-10	10	$\mu\text{A}$	$0 \text{ V} \leq V_{in} \leq V_{CC} + 0.3 \text{ V}$
Output leakage current	$I_{LO}$	TBD	TBD	-10	10	-10	10	$\mu\text{A}$	$0 \text{ V} \leq V_{out} \leq V_{CC}$ Dout = disable
Output high voltage	$V_{OH}$	TBD	TBD	2.4	$V_{CC}$	2.4	$V_{CC}$	V	High Iout = -2 mA
Output low voltage	$V_{OL}$	TBD	TBD	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes: 1.  $I_{CC}$  depends on output load condition when the device is selected.  $I_{CC}$  max is specified at the output open condition.

2. Address can be changed once or less while  $\overline{\text{RAS}} = V_{IL}$ .

3. Address can be changed once or less within one page mode cycle  $t_{PC}$ .

4.  $V_{IH} \geq V_{CC} - 0.2 \text{ V}$ ,  $0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$ .

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## HM5164400A Series, HM5165400A Series

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Capacitance ( $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ )

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	$C_{11}$	—	5	pF	1
Input capacitance (Clocks)	$C_{12}$	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	7	pF	1, 2

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.  
2.  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}} = V_{IH}$  to disable Dout.

## HM5164400A Series, HM5165400A Series

**AC Characteristics** ( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ ) \*1, \*2, \*17

### Test Conditions

- Input rise and fall time: 5 ns
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate +  $C_L$  (100 pF) (Including scope and jig)

### Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HM5164400A/HM5165400A							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	$t_{RC}$	TBD	—	110	—	130	—	ns	
$\overline{\text{RAS}}$ precharge time	$t_{RP}$	TBD	—	40	—	50	—	ns	
$\overline{\text{CAS}}$ precharge time	$t_{CP}$	TBD	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ pulse width	$t_{RAS}$	TBD	TBD	60	10000	70	10000	ns	
$\overline{\text{CAS}}$ pulse width	$t_{CAS}$	TBD	TBD	15	10000	18	10000	ns	
Row address setup time	$t_{ASR}$	TBD	—	0	—	0	—	ns	
Row address hold time	$t_{RAH}$	TBD	—	10	—	10	—	ns	
Column address setup time	$t_{ASC}$	TBD	—	0	—	0	—	ns	
Column address hold time	$t_{CAH}$	TBD	—	10	—	15	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	$t_{RCD}$	TBD	TBD	20	45	20	52	ns	3
$\overline{\text{RAS}}$ to column address delay time	$t_{RAD}$	TBD	TBD	15	30	15	35	ns	4
$\overline{\text{RAS}}$ hold time	$t_{RSH}$	TBD	—	15	—	18	—	ns	
$\overline{\text{CAS}}$ hold time	$t_{CSH}$	TBD	—	60	—	70	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	$t_{CRP}$	TBD	—	5	—	5	—	ns	
$\overline{\text{OE}}$ to Din delay time	$t_{OED}$	TBD	—	15	—	18	—	ns	5
$\overline{\text{OE}}$ delay time from Din	$t_{DZO}$	TBD	—	0	—	0	—	ns	6
$\overline{\text{CAS}}$ delay time from Din	$t_{DZC}$	TBD	—	0	—	0	—	ns	6
Transition time (rise and fall)	$t_T$	TBD	TBD	3	50	3	50	ns	7

## HM5164400A Series, HM5165400A Series

### Read Cycle

Parameter	Symbol	HM5164400A/HM5165400A						Unit	Notes
		-5		-6		-7			
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	$t_{\text{RAC}}$	—	TBD	—	60	—	70	ns	8, 9
Access time from $\overline{\text{CAS}}$	$t_{\text{CAC}}$	—	TBD	—	15	—	18	ns	9, 10, 16
Access time from address	$t_{\text{AA}}$	—	TBD	—	30	—	35	ns	9, 11, 16
Access time from $\overline{\text{OE}}$	$t_{\text{OEA}}$	—	TBD	—	15	—	18	ns	9, 19
Read command setup time	$t_{\text{RCS}}$	TBD	—	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	$t_{\text{RCH}}$	TBD	—	0	—	0	—	ns	12
Read command hold time to $\overline{\text{RAS}}$	$t_{\text{RRH}}$	TBD	—	5	—	5	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	$t_{\text{RAL}}$	TBD	—	30	—	35	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	$t_{\text{CAL}}$	TBD	—	30	—	35	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	$t_{\text{CLZ}}$	TBD	—	0	—	0	—	ns	
Output data hold time	$t_{\text{OH}}$	TBD	—	3	—	3	—	ns	
Output data hold time from $\overline{\text{OE}}$	$t_{\text{OHO}}$	TBD	—	3	—	3	—	ns	
Output buffer turn-off time	$t_{\text{OFF}}$	—	TBD	—	15	—	15	ns	13
Output buffer turn-off to $\overline{\text{OE}}$	$t_{\text{OEZ}}$	—	TBD	—	15	—	15	ns	13
$\overline{\text{CAS}}$ to Din delay time	$t_{\text{CDD}}$	TBD	—	15	—	18	—	ns	5

### Write Cycle

Parameter	Symbol	HM5164400A/HM5165400A						Unit	Notes
		-5		-6		-7			
		Min	Max	Min	Max	Min	Max		
Write command setup time	$t_{\text{WCS}}$	TBD	—	0	—	0	—	ns	14
Write command hold time	$t_{\text{WCH}}$	TBD	—	10	—	15	—	ns	
Write command pulse width	$t_{\text{WP}}$	TBD	—	10	—	10	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	$t_{\text{RWL}}$	TBD	—	15	—	18	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	$t_{\text{CWL}}$	TBD	—	15	—	18	—	ns	
Data-in setup time	$t_{\text{DS}}$	TBD	—	0	—	0	—	ns	
Data-in hold time	$t_{\text{DH}}$	TBD	—	10	—	15	—	ns	

## HM5164400A Series, HM5165400A Series

### Read-Modify-Write Cycle

		HM5164400A/HM5165400A							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	$t_{RWC}$	TBD	—	155	—	181	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	$t_{RWD}$	TBD	—	85	—	98	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	$t_{CWD}$	TBD	—	40	—	46	—	ns	14
Column address to $\overline{WE}$ delay time	$t_{AWD}$	TBD	—	55	—	63	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	$t_{OEH}$	TBD	—	15	—	18	—	ns	

### Refresh Cycle

		HM5164400A/HM5165400A							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time (CBR refresh cycle)	$t_{CSR}$	TBD	—	5	—	5	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	$t_{CHR}$	TBD	—	10	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	$t_{WRP}$	TBD	—	0	—	0	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	$t_{WRH}$	TBD	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	$t_{RPC}$	TBD	—	0	—	0	—	ns	

### Fast Page Mode Cycle

		HM5164400A/HM5165400A							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode cycle time	$t_{PC}$	TBD	—	40	—	45	—	ns	
Fast page mode $\overline{RAS}$ pulse width	$t_{RASP}$	—	TBD	—	100000	—	100000	ns	15
Access time from $\overline{CAS}$ precharge	$t_{CPA}$	—	TBD	—	35	—	40	ns	9, 16
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	$t_{CPRH}$	TBD	—	35	—	40	—	ns	

## HM5164400A Series, HM5165400A Series

### Fast Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM5164400A/HM5165400A						Unit	Notes
		-5		-6		-7			
		Min	Max	Min	Max	Min	Max		
Fast page mode read-modify-write cycle time	$t_{PRWC}$	TBD	—	85	—	96	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	$t_{CPW}$	TBD	—	60	—	68	—	ns	14

### Refresh (HM5164400A Series)

Parameter	Symbol	Max	Unit	Note
Refresh period	$t_{REF}$	64	ms	8192 cycles
Refresh period (L-version)	$t_{REF}$	TBD	ms	8192 cycles

### Refresh (HM5165400A Series)

Parameter	Symbol	Max	Unit	Note
Refresh period	$t_{REF}$	64	ms	4096 cycles
Refresh period (L-version)	$t_{REF}$	128	ms	4096 cycles

## HM5164400A Series, HM5165400A Series

### Self Refresh Mode (L-version)

Parameter	Symbol	HM5164400AL/HM5165400AL						Unit	Notes
		-5		-6		-7			
		Min	Max	Min	Max	Min	Max		
RAS pulse width (Self refresh)	$t_{RASS}$	TBD	—	100	—	100	—	$\mu s$	20
$\overline{RAS}$ precharge time (Self refresh)	$t_{RPS}$	TBD	—	110	—	130	—	ns	
CAS hold time (Self refresh)	$t_{CHS}$	TBD	—	-50	—	-50	—	ns	

- Notes:
1. AC measurements assume  $t_T = 5$  ns.
  2. An initial pause of 200  $\mu s$  is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing  $\overline{RAS}$ -only refresh or  $\overline{CAS}$ -before- $\overline{RAS}$  refresh).
  3. Operation with the  $t_{RCD}$  (max) limit insures that  $t_{RAC}$  (max) can be met,  $t_{RCD}$  (max) is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (max) limit, then access time is controlled exclusively by  $t_{CAC}$ .
  4. Operation with the  $t_{RAD}$  (max) limit insures that  $t_{RAC}$  (max) can be met,  $t_{RAD}$  (max) is specified as a reference point only; if  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (max) limit, then access time is controlled exclusively by  $t_{AA}$ .
  5. Either  $t_{OED}$  or  $t_{ODD}$  must be satisfied.
  6. Either  $t_{DZO}$  or  $t_{DZC}$  must be satisfied.
  7.  $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  (min) and  $V_{IL}$  (max).
  8. Assumes that  $t_{RCD} \leq t_{RCD}$  (max) and  $t_{RAD} \leq t_{RAD}$  (max). If  $t_{RCD}$  or  $t_{RAD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  exceeds the value shown.
  9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
  10. Assumes that  $t_{RCD} \geq t_{RCD}$  (max) and  $t_{RCD} + t_{CAC}$  (max)  $\geq t_{RAD} + t_{AA}$  (max).
  11. Assumes that  $t_{RAD} \geq t_{RAD}$  (max) and  $t_{RCD} + t_{CAC}$  (max)  $\leq t_{RAD} + t_{AA}$  (max).
  12. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycles.
  13.  $t_{OFF}$  (max) and  $t_{OEZ}$  (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
  14.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{AWD}$  and  $t_{CPW}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if  $t_{WCS} \geq t_{WCS}$  (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{RWD} \geq t_{RWD}$  (min),  $t_{CWD} \geq t_{CWD}$  (min), and  $t_{AWD} \geq t_{AWD}$  (min), or  $t_{CWD} \geq t_{CWD}$  (min),  $t_{AWD} \geq t_{AWD}$  (min) and  $t_{CPW} \geq t_{CPW}$  (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
  15.  $t_{RASP}$  defines  $\overline{RAS}$  pulse width in fast page mode cycles.
  16. Access time is determined by the longest among  $t_{AA}$ ,  $t_{CAC}$  and  $t_{CPA}$ .
  17. All the  $V_{CC}$  and  $V_{SS}$  pins shall be supplied with the same voltages.
  18. In delayed write or read-modify-write cycles,  $\overline{OE}$  must disable output buffer prior to applying data to the device.
  19. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large  $V_{CC}/V_{SS}$  line noise, which causes to degrade  $V_{IH}$  min/ $V_{IL}$  max level.
  20. Please do not use  $t_{RASS}$  timing,  $10 \mu s \leq t_{RASS} \leq 100 \mu s$ . During this period, the device is in transition state from normal operation mode to self refresh mode. If  $t_{RASS} \geq 100 \mu s$ , then  $\overline{RAS}$  precharge time should use  $t_{RPS}$  instead of  $t_{RP}$ .

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## HM5164400A Series, HM5165400A Series

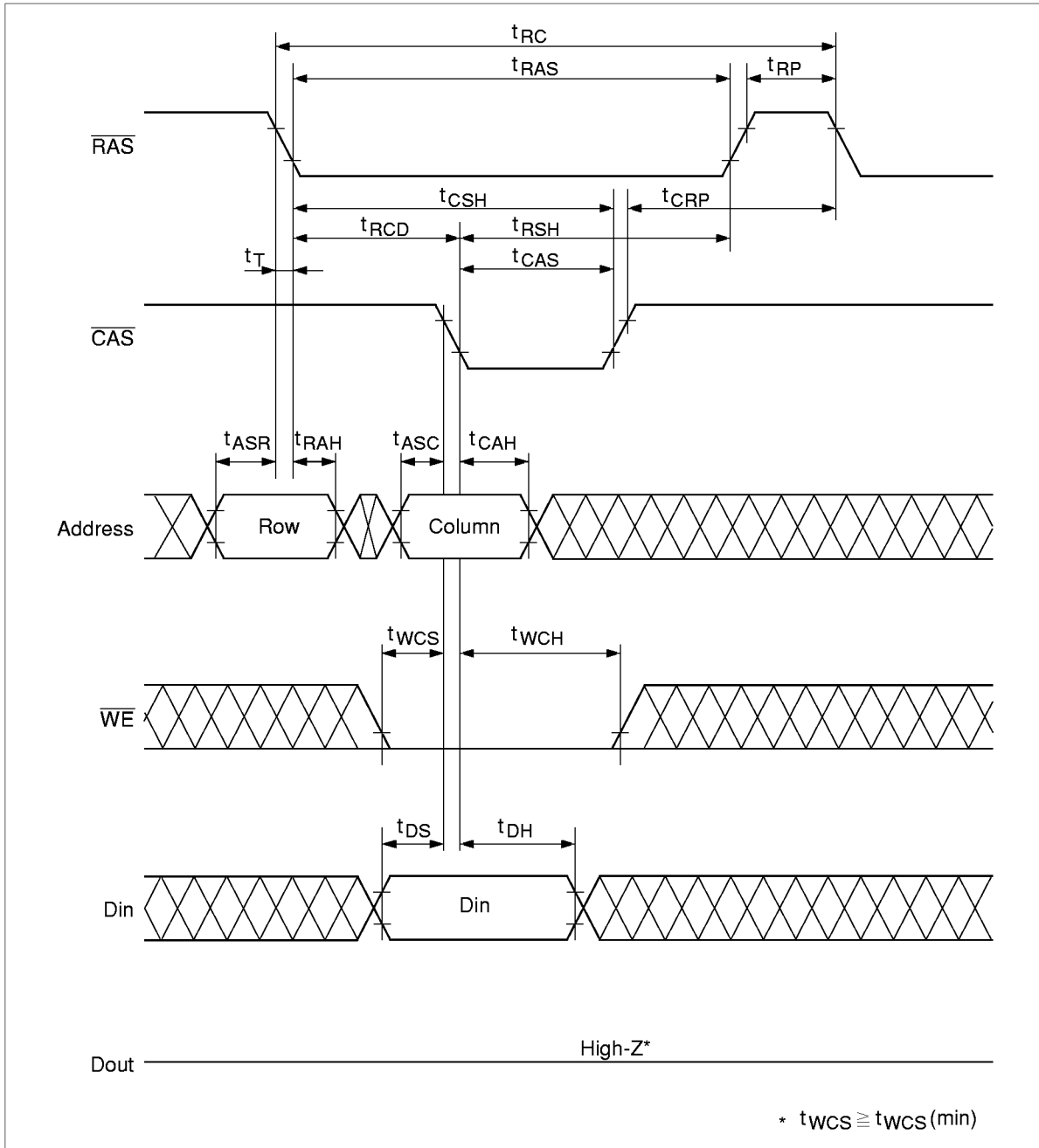
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21. CBR burst refresh or 4096 cycles of distributed CBR refresh with 15.6  $\mu$ s interval should be executed within 64 ms immediately after exiting from and before entering into the self refresh mode.
22. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
23. XXX: H or L (H:  $V_{IH}(\min) \leq V_{IN} \leq V_{IH}(\max)$ , L:  $V_{IL}(\min) \leq V_{IN} \leq V_{IL}(\max)$ )  
/////: Invalid Dout  
When the address, clock and input pins are not described on timing waveforms, their pins must be applied  $V_{IH}$  or  $V_{IL}$ .



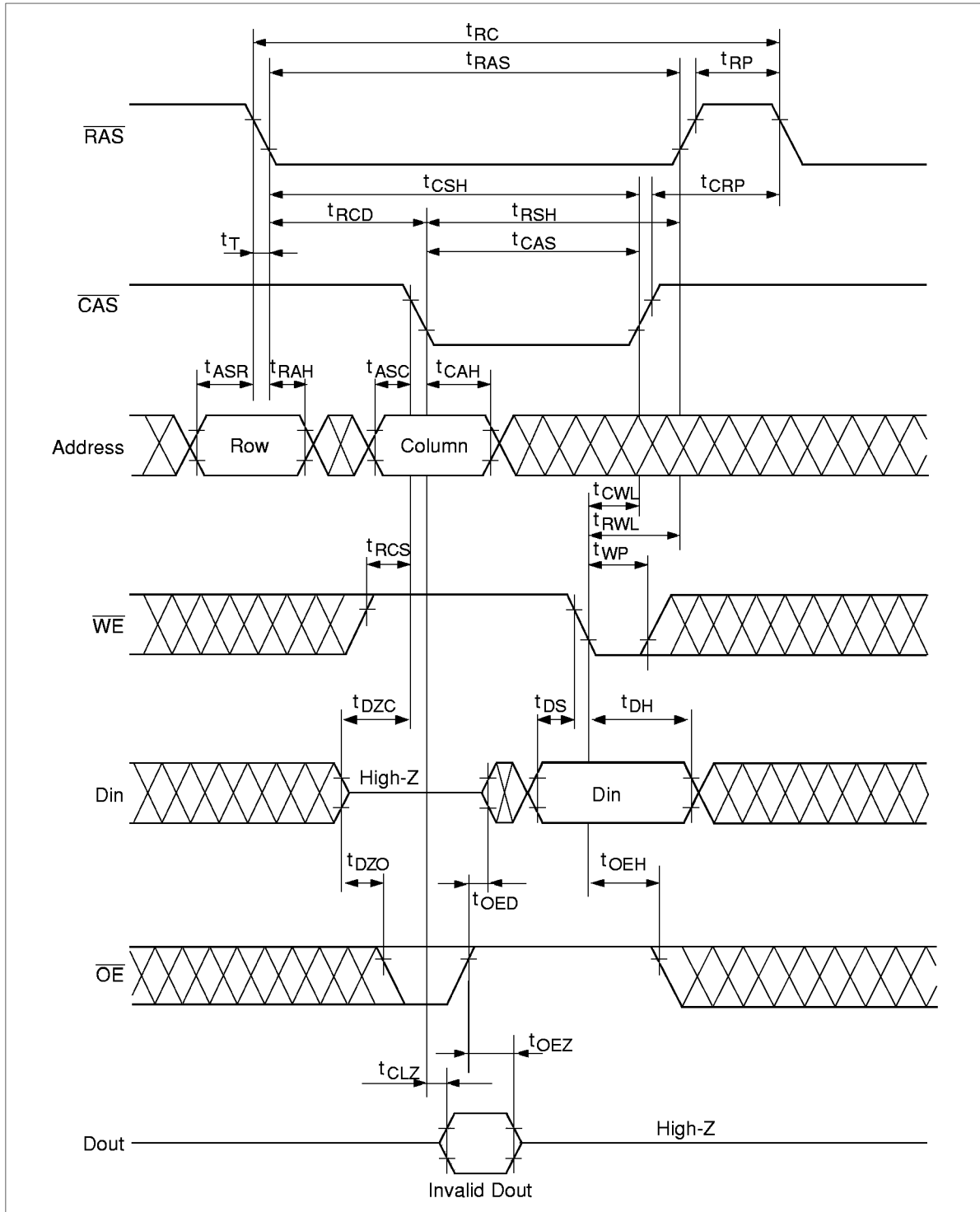
# HM5164400A Series, HM5165400A Series

## Early Write Cycle



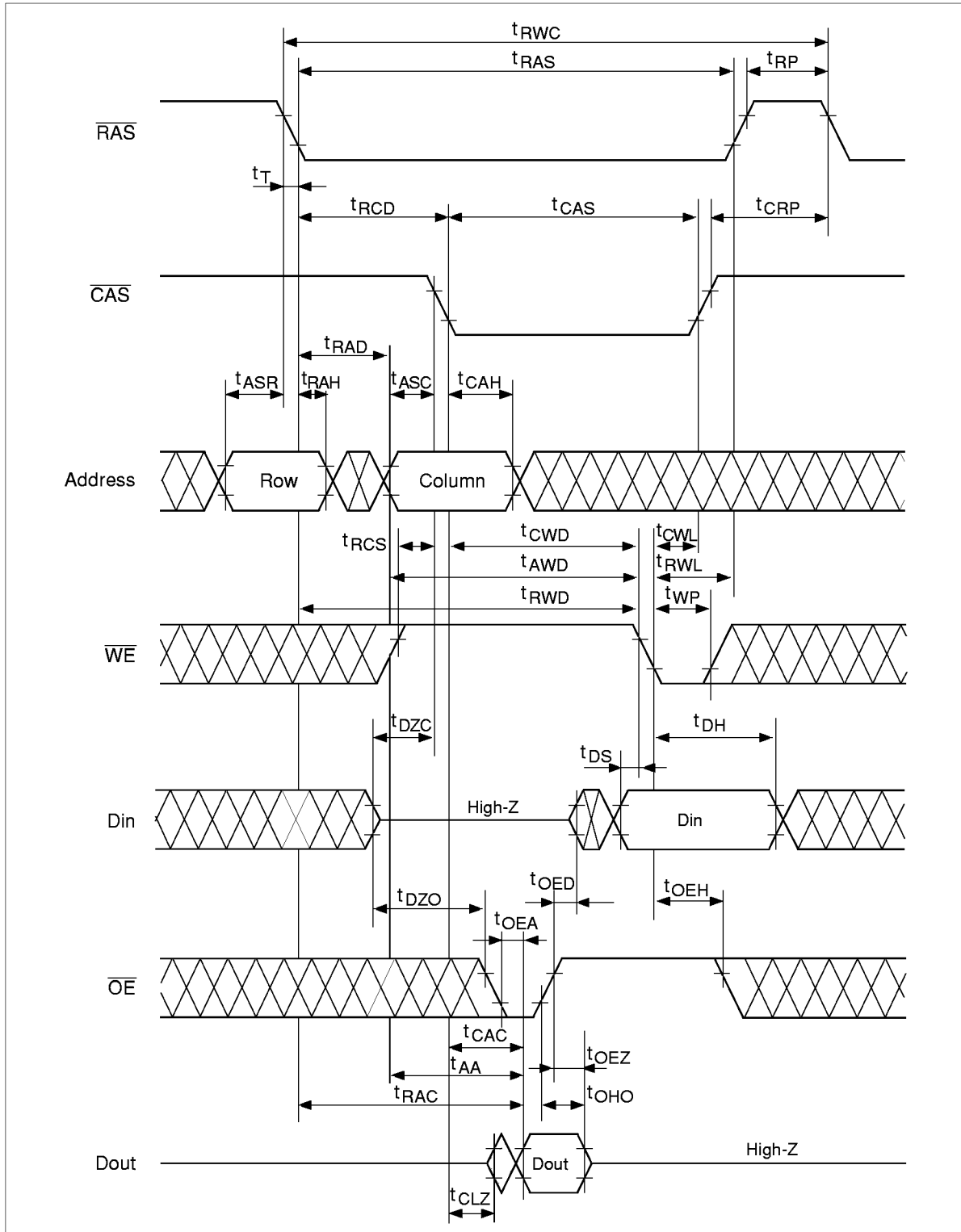
# HM5164400A Series, HM5165400A Series

## Delayed Write Cycle\*18

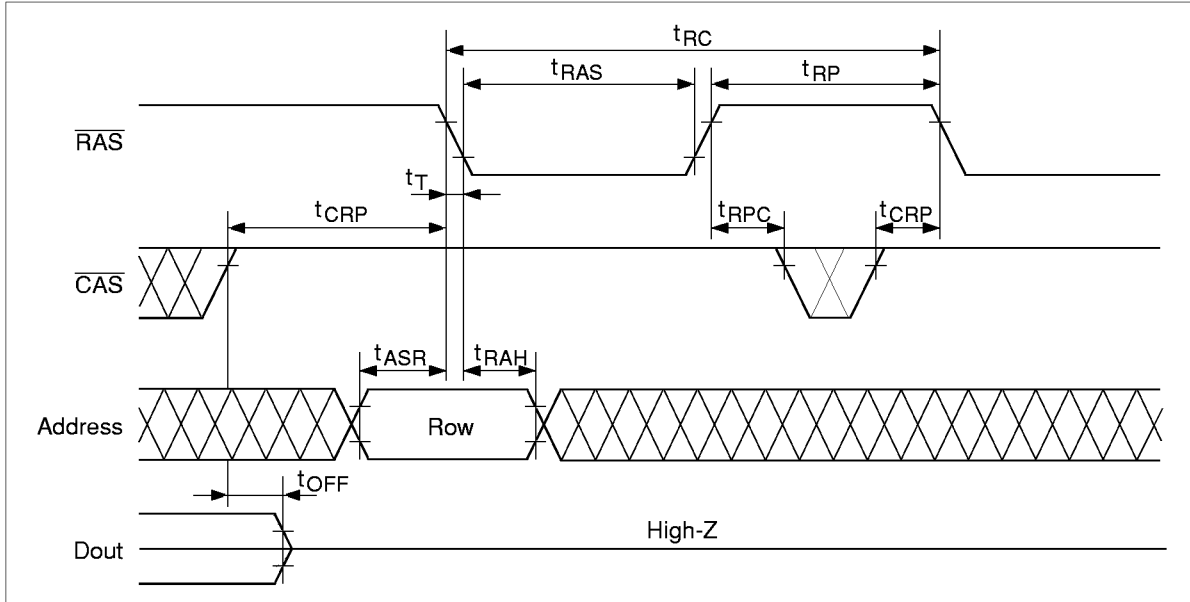


# HM5164400A Series, HM5165400A Series

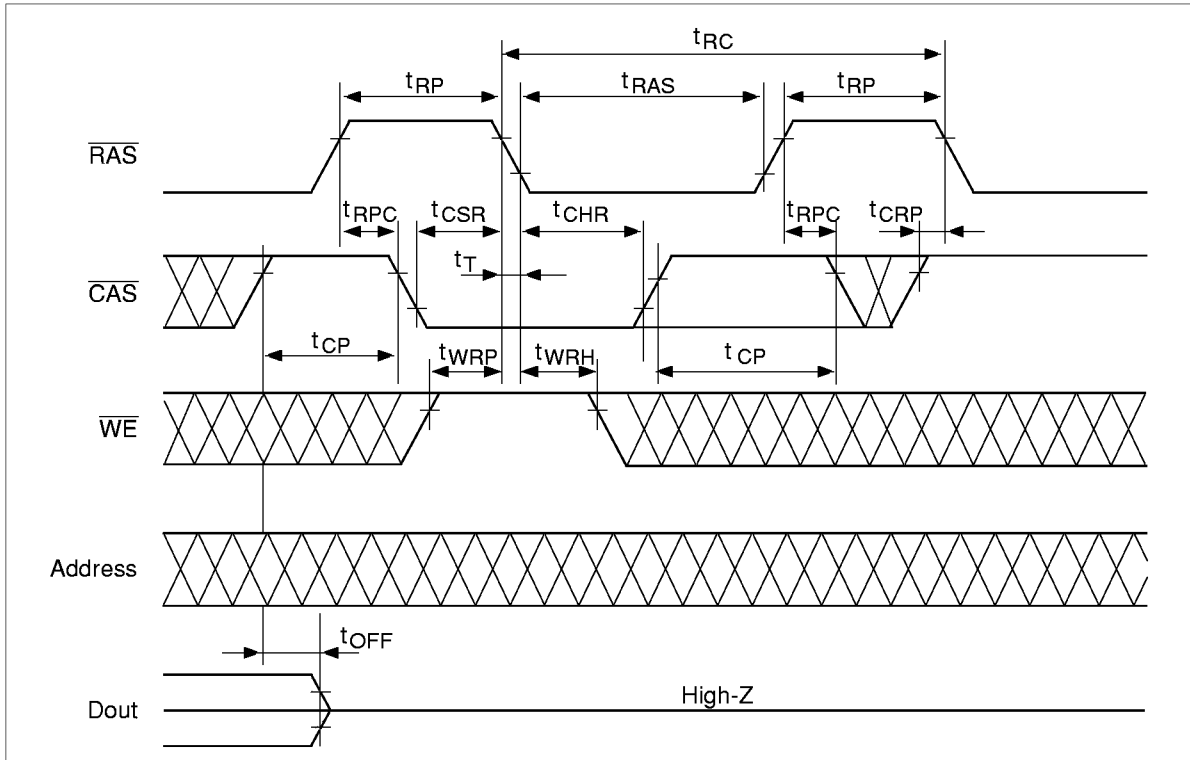
## Read-Modify-Write Cycle\*18



**$\overline{\text{RAS}}$ -Only Refresh Cycle**

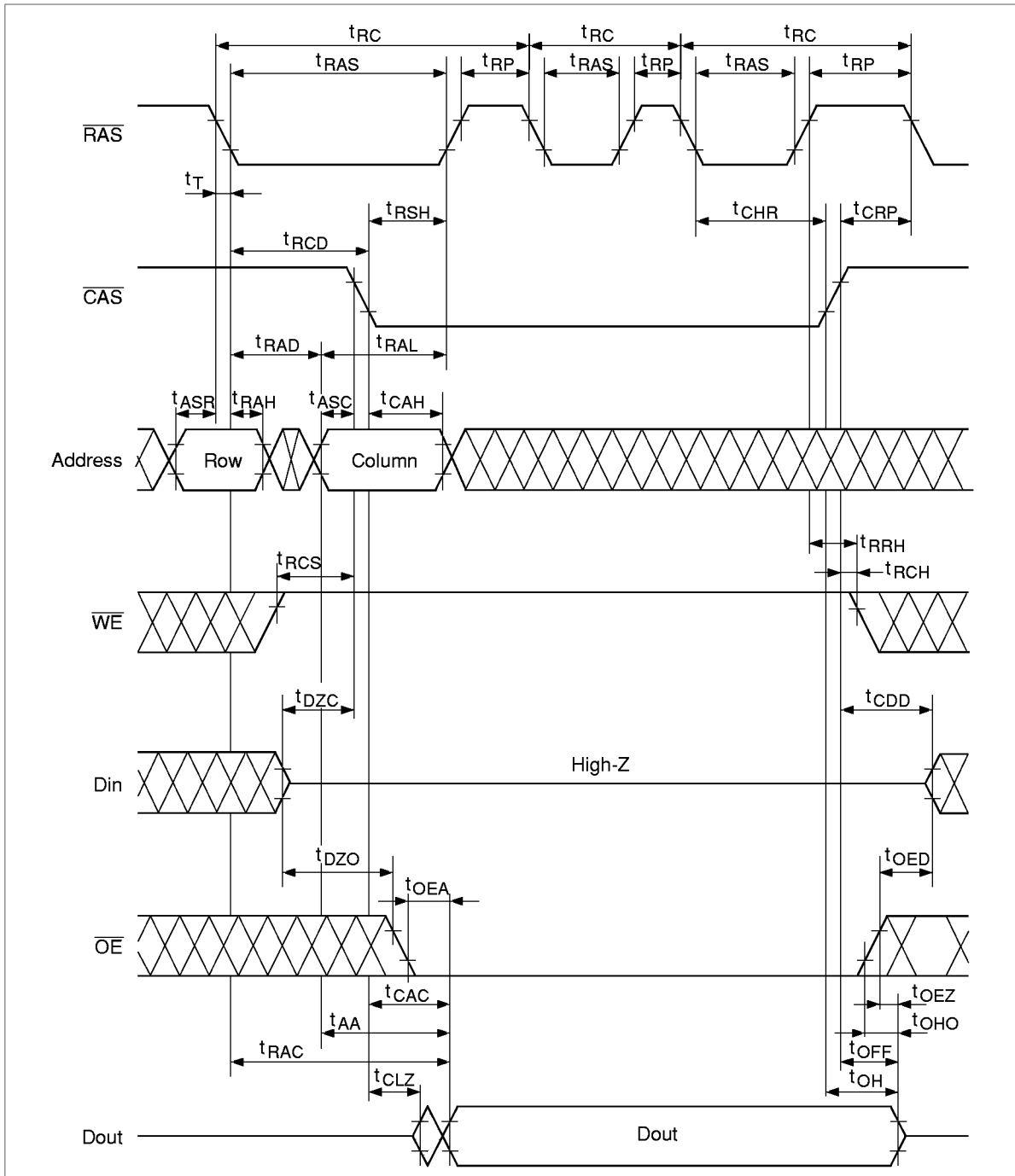


**$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$  Refresh Cycle**



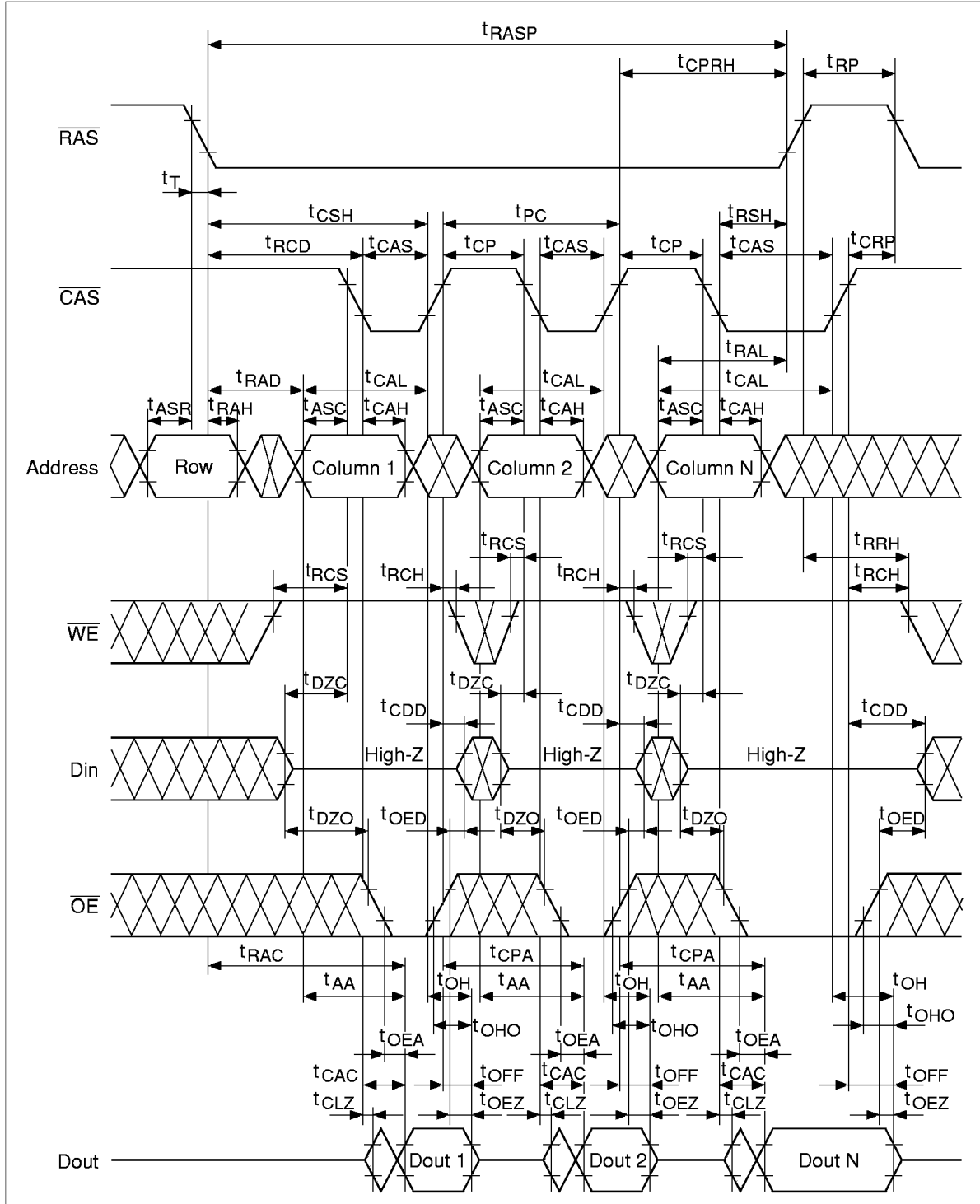
# HM5164400A Series, HM5165400A Series

## Hidden Refresh Cycle



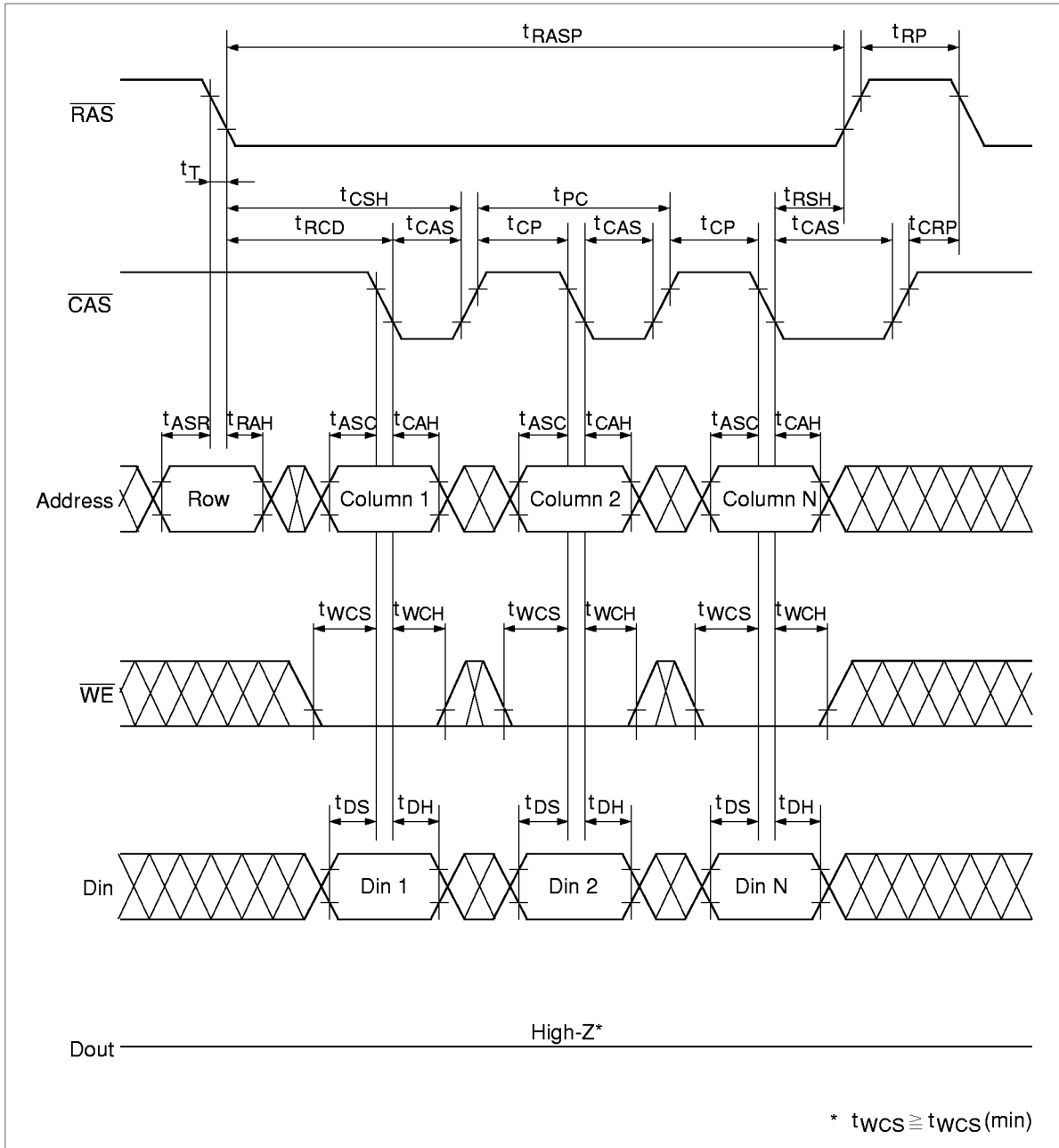
# HM5164400A Series, HM5165400A Series

## Fast Page Mode Read Cycle



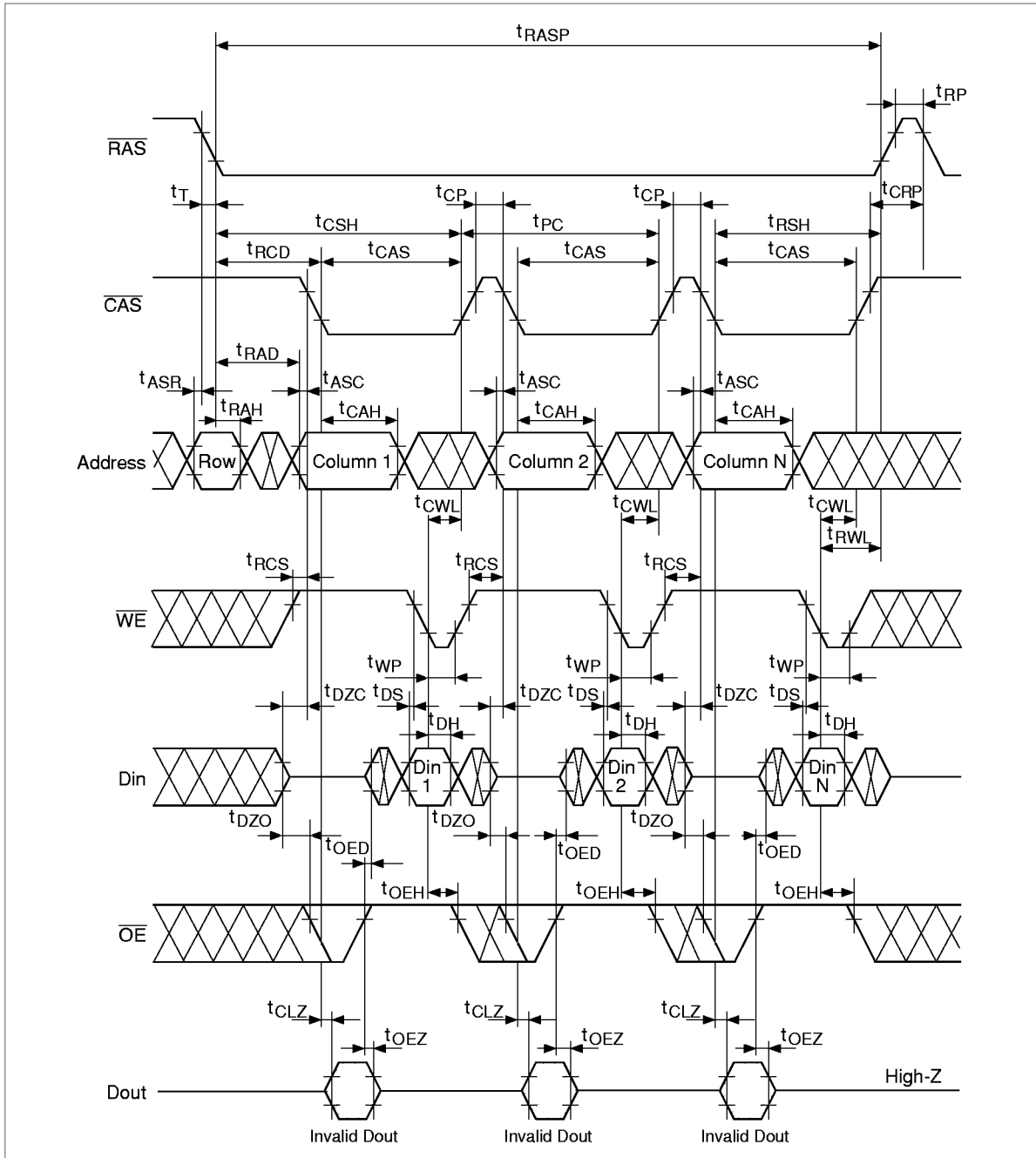
# HM5164400A Series, HM5165400A Series

## Fast Page Mode Early Write Cycle



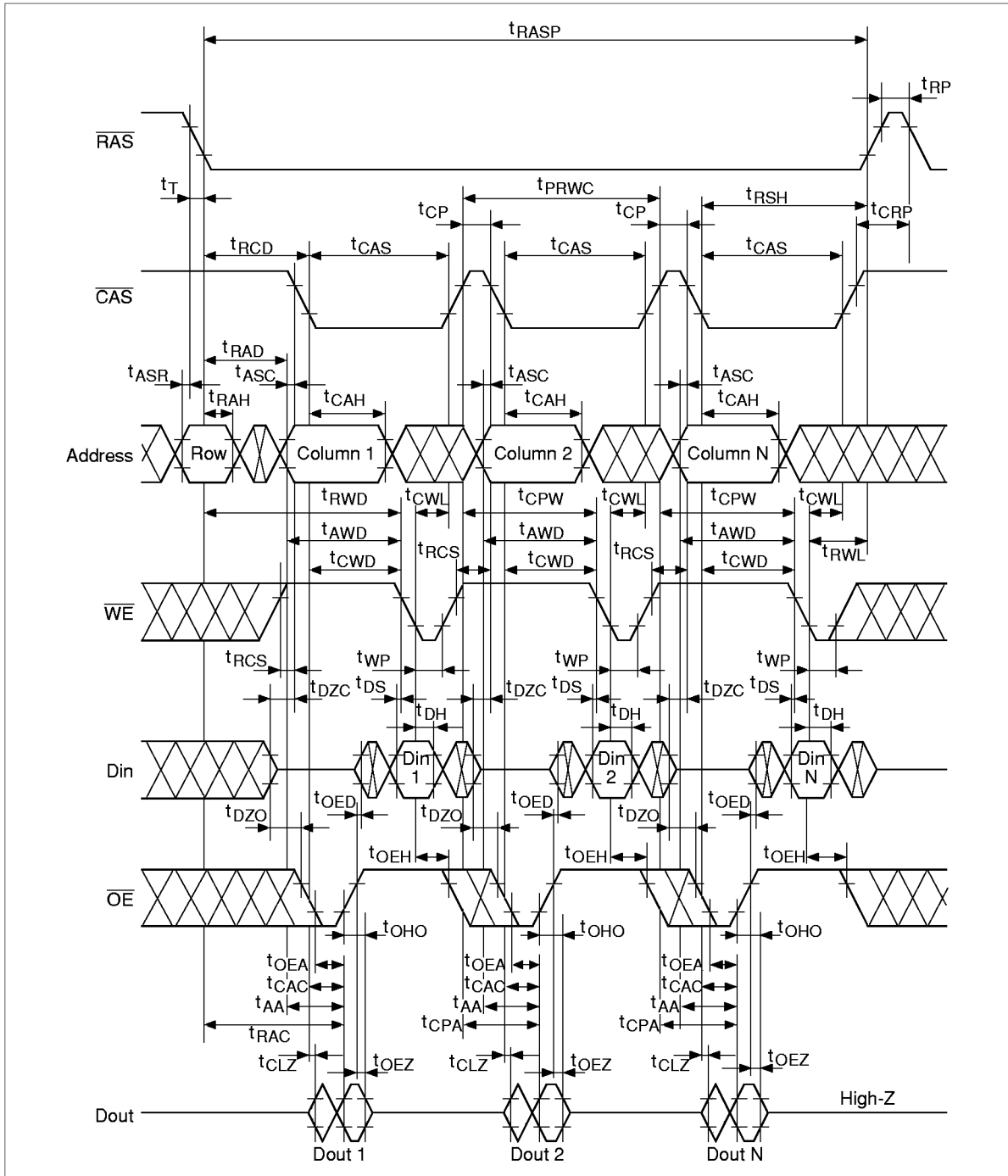
# HM5164400A Series, HM5165400A Series

## Fast Page Mode Delayed Write Cycle\*18



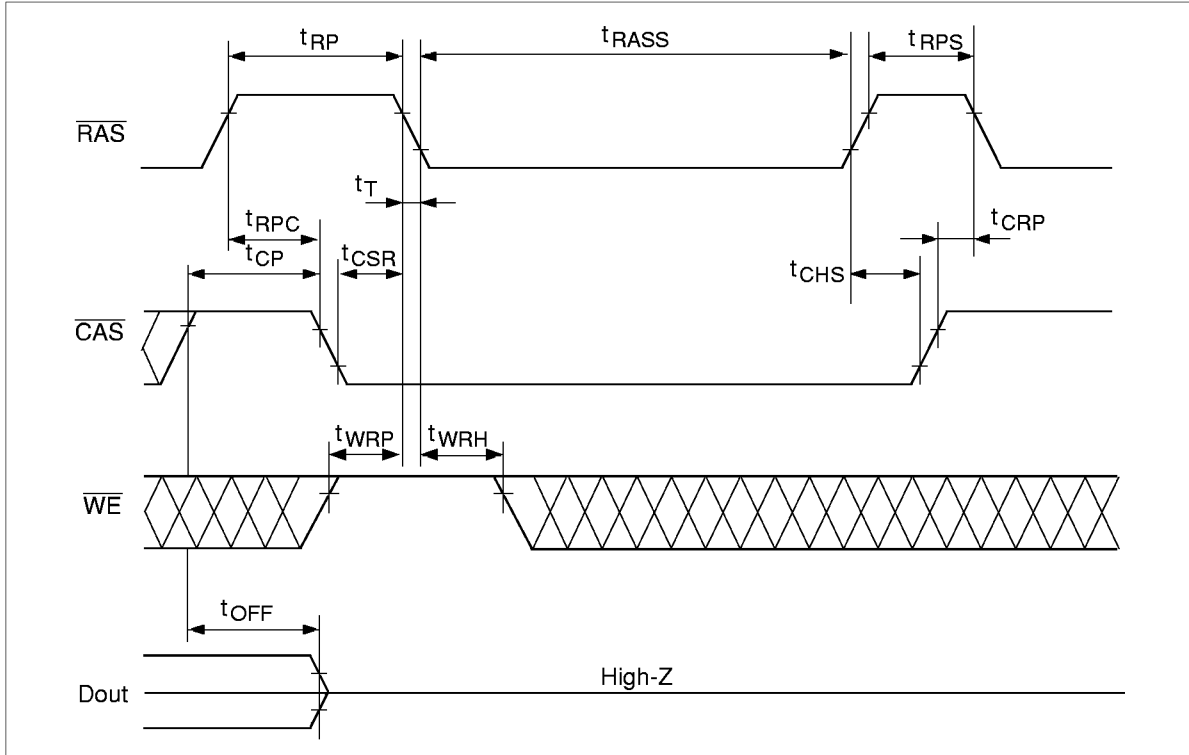
# HM5164400A Series, HM5165400A Series

## Fast Page Mode Read-Modify-Write Cycle\*18



# HM5164400A Series, HM5165400A Series

## Self Refresh Cycle (L-version)\*20, 21, 22



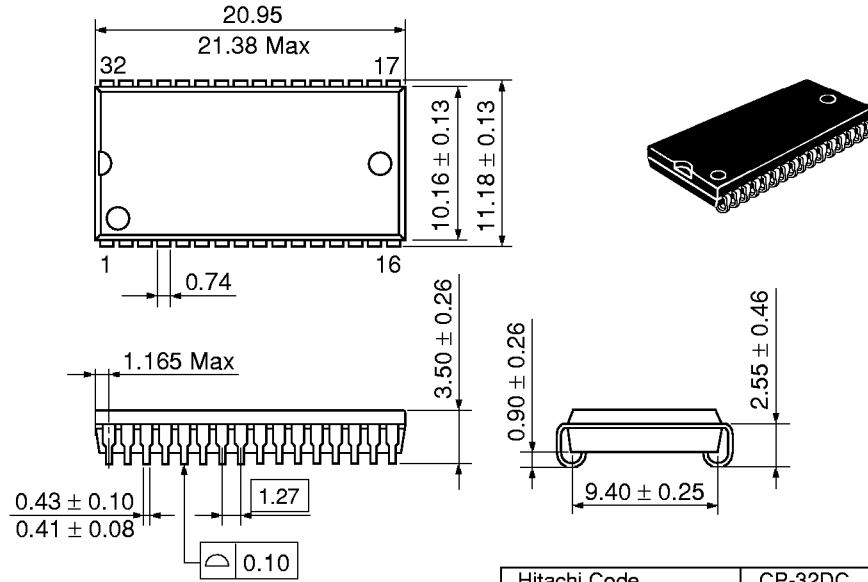
# HM5164400A Series, HM5165400A Series

## Package Dimensions

HM5164400AJ/ALJ Series

HM5165400AJ/ALJ Series (CP-32DC)

Unit: mm



Dimension including the plating thickness  
Base material dimension

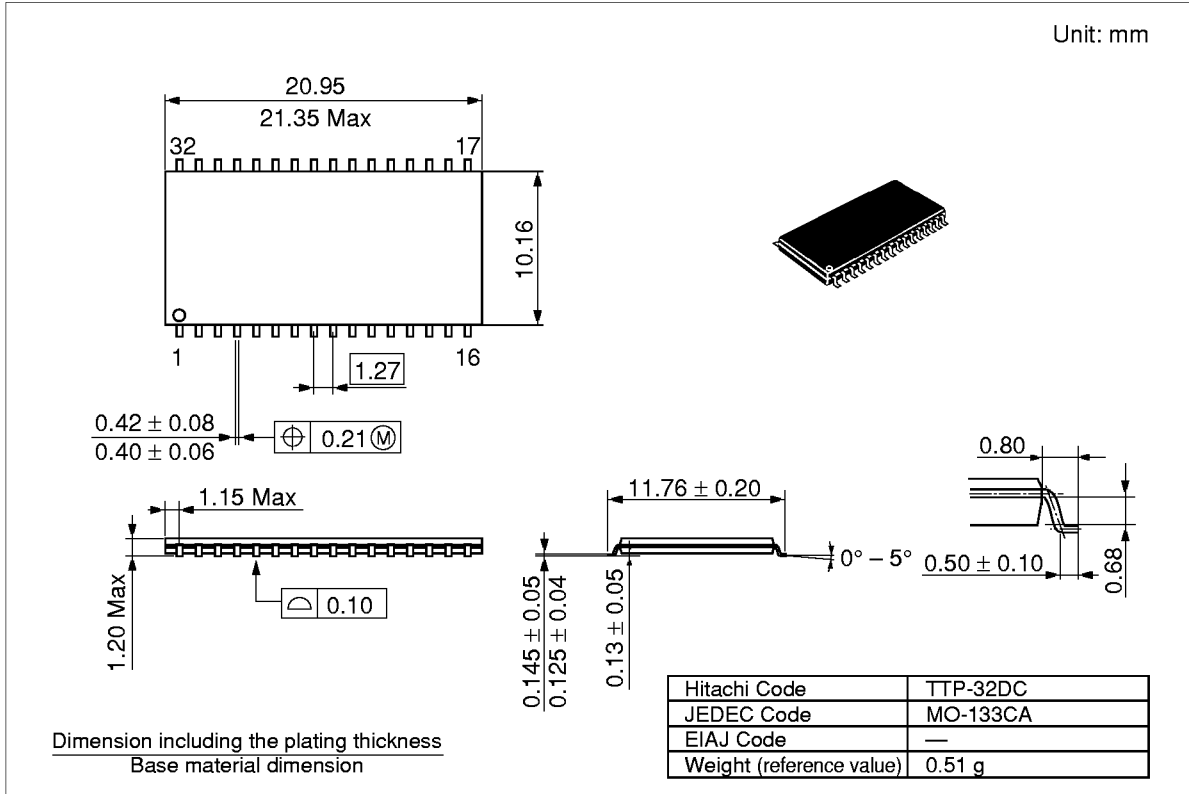
Hitachi Code	CP-32DC
JEDEC Code	—
EIAJ Code	SC-637-B
Weight (reference value)	1.2 g

# HM5164400A Series, HM5165400A Series

HM5164400ATT/ALTT Series

HM5165400ATT/ALTT Series (TTP-32DC)

Unit: mm



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## HM5164400A Series, HM5165400A Series

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## HM5164400A Series, HM5165400A Series

### Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Jan. 22, 1996	Initial issue	S. Ikenaga	J. Kitano
0.1	Jun. 3, 1996	Change format  Unification of HM5164400A Series and HM5165400A Series  Addition of HM5164400A/HM5165400A-5 Series  Addition of HM5164400AJ/ALJ Series, HM5165400AJ/ALJ Series (CP-32DC) HM5165400AT/ALTT Series (TTP-32DC)  Pin Descriptions Addition of Row/Refresh address and Column address to address input  Addition of Block Diagrams  DC Characteristics (HM5164400A) $I_{CC1}$ max: 100/90 mA to TBD/130/110 mA $I_{CC3}$ max: 120/105 mA to TBD/130/110 mA $I_{CC6}$ max: 120/105 mA to TBD/150/130 mA $I_{CC7}$ max: 100/90 mA to TBD/130/110 mA Addition of note 4  AC Characteristics $t_{RCD}$ max: 38/45 ns to TBD/45/52 ns Addition of notes 20 to 23 Change of notes 3 Change of notes 18  Timing waveforms Deletion of note: $t_{OEH} \geq t_{CWL}$ Deletion of notes about undefined pins	S. Ikenaga	J. Kitano
0.2	Jan. 22, 1997	Power dissipation  TBD/540/468 mW to TBD/378/324 mW (max) (HM5164400A Series) TBD/648/576 mW to TBD/558/486 mW (max) (HM5165400A Series)  DC Characteristics (HM5164400A Series) $I_{CC1}$ (max): TBD/130/110 mA to TBD/105/90 mA $I_{CC3}$ (max): TBD/130/110 mA to TBD/105/90 mA $I_{CC6}$ (max): TBD/150/130 mA to TBD/140/120 mA $I_{CC7}$ (max): TBD/120/110 mA to TBD/80/70 mA $I_{LO}$ test conditions: $0 V \leq V_{out} \leq V_{CC} + 0.3$ to $0 V \leq V_{out} \leq V_{CC}$  DC Characteristics (HM5165400A Series) $I_{CC1}$ (max): TBD/180/160 mA to TBD/155/135 mA $I_{CC3}$ (max): TBD/180/160 mA to TBD/155/135 mA $I_{CC6}$ (max): TBD/150/130 mA to TBD/140/120 mA $I_{CC7}$ (max): TBD/120/110 mA to TBD/95/85 mA $I_{LO}$ test conditions: $0 V \leq V_{out} \leq V_{CC} + 0.3$ to $0 V \leq V_{out} \leq V_{CC}$	J. Kitano	J. Kitano

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## HM5164400A Series, HM5165400A Series

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### Revision Record

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Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Aug. 29, 1997	Deletion of preliminary Correct errors (HM5164400A Series) $t_{REF}$ (L-version): 128 ms to TBD (for suspension of L-version), 4096 cycles to 8192 cycles		

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