

M-986-1R1 & -2R1 MF Transceivers

Teltone M-986-1R1 and -2R1 MF Transceivers contain all the logic necessary to transmit and receive R1 multifrequency signals on one integrated circuit (IC). M-986-1R1 is a single-channel version; M-986-2R1 provides two channels. CCITT R2 single and dual multifrequency transceivers are also available as M-986-1R2 and -2R2.

Operating with a 20.48 MHz crystal, the M-986 is capable of providing a direct digital interface to a μ -law-encoded PCM digital input. Each channel can be connected to an analog source using a coder-decoder (codec) as shown in Figure 1.

For the R1 versions of the M-986, μ -law is used for coding/decoding. The M-986 is configured and controlled through an integral coprocessor port.

Features

- Direct μ -Law PCM digital input
- 2.048 Mb/s clocking
- Operates with standard codecs for analog interfacing
- Microprocessor read/write interface
- Binary or 2-of-6 data formats
- Single- or dual-channel versions
- 5 volt power

Applications

- Test equipment
- Trunk adapters
- Paging terminals
- Traffic recorders
- PBXs

Options

- PLCC: Plastic Leaded Chip Carrier
 - Ceramic Leaded Chip Carrier
- (Specifications on request.)

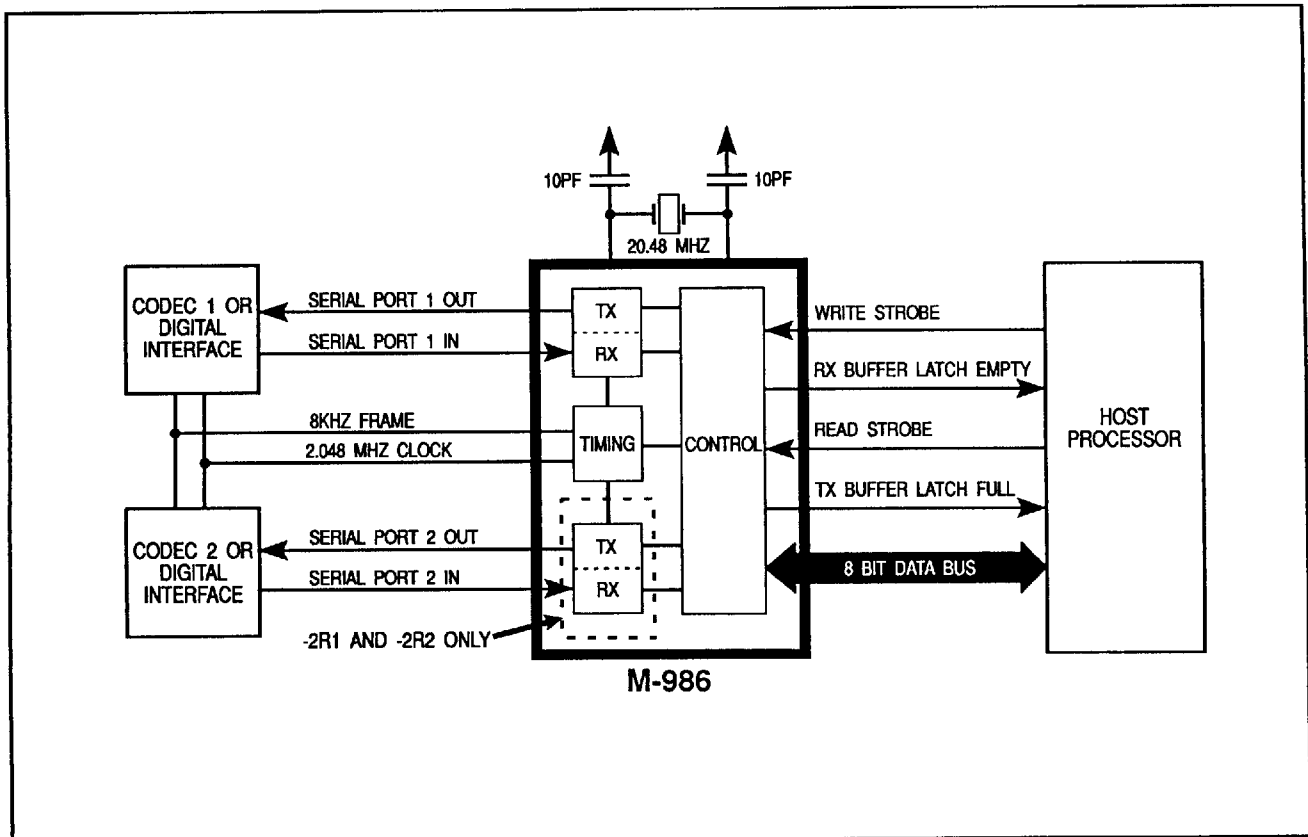


Figure 1 Block Diagram

Functional Description

The M-986-XR1 can be set up for various modes of operation by writing two configuration bytes to the coprocessor port. The format of the two configuration bytes is shown in Table 1 and the configuration options are described in the following paragraphs.

Configuration Options

External/Internal Codec Clock (ECLK): If external codec clocking is selected, an external clocking source provides an 8kHz transmit framing clock and an 8kHz receive framing clock. It also provides a serial bit clock with a frequency that is a multiple of 8 kHz between 216 kHz and 2.496 MHz for exchange of data via the serial ports. When internal codec clocking is selected, the M-986-XR1 provides an 8kHz framing clock and a 2.048 MHz serial bit clock.

2 of 6/Binary Input/Output (IOM): When the 2-of-6 input/output is selected, the M-986-XR1 encodes the received R1 MF tone pair into a 6-bit format, where each bit represents one of the six possible frequencies. A logic high level indicates the presence of a frequency. The digital input to the M-986-XR1

that selects the transmitted R1 MF tone pair must also be coded in the 2-of-6 format. See Table 2.

When binary input/output is selected, the M-986-XR1 encodes the received R1 MF tone pair into a 4 bit binary format. The digital input to the M-986-XR1 that selects the transmitted R1 MF tone pair must also be coded in a 4 bit binary format. See Table 3.

Enable/Disable Channel (ENC): When a channel is disabled, the receiver does not process its codec input for R1 MF tones, and the transmitter does not respond to transmit commands. If a transmit command is given while the channel is enabled, the "tone off" command must be given before the channel is disabled. Disabling the channel does not automatically shut off the transmitter. When a channel is enabled, the receiver and transmitter for that channel function normally.

Long/Short KP Tone Detection Time (KPL): When long KP tone detection is selected, the minimum on time for the KP tone to be detected is 55 milliseconds. When short KP tone detection is selected, the minimum on time for the KP tone to be detected is 30 milliseconds (the same as the minimum on time for the rest of the MF tones).

Table 1 Configuration Bytes

CONFIGURATION BYTE 1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	ECLK	IOM	ENC1	KPL1	KPEN1	0
ECLK	Channels 1 & 2	1 = External codec clock; 0 = Internal codec clock					
IOM	Channels 1 & 2	1 = Binary input/output; 0 = 2-of-6 input/output					
ENC1	Channel 1	1 = Enable channel; 0 = Disable channel					
KPL1	Channel 1	1 = 55 ms detection time for KP; 0 = 30 ms detection time for KP					
KPEN1	Channel 1	1 = Enable MF tone detection after KP detection; 0 = MF tone detection always on					
CONFIGURATION BYTE 2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	ENC2	KPL2	KPEN2	0
ENC2	Channel 2	1 = Enable channel; 0 = Disable channel					
KPL2	Channel 2	1 = 55 ms detection time for KP; 0 = 30 ms detection time for KP					
KPEN2	Channel 2	1 = Enable MF tone detection after KP detection; 0 = MF tone detection always on					

Enable MF Tone Detection After Reception of KP (KPEN):

When this feature is enabled, MF tone detection is enabled after reception of the KP tone, and disabled after reception of ST, ST1, ST2, or ST3 tones. When this feature is disabled, MF tone detection is always enabled.

Initial Configuration: The configuration of the M-986-XR1 immediately after a reset will be as follows:

- channel disabled
- 2-of-6 input/output
- external serial and serial frame clocks.

Also, the M-986-XR1 will place a 00 hex on the coprocessor port to indicate to the host processor that it is working.

Transmit Tone Command

The transmit tone command allows the host processor to transmit any two of the 6 R1 MF frequencies. The format of the command depends on whether the M-986 is configured for binary format or 2-of-6 format. See Tables 2 and 3.

Received Tone Detection

When a tone is detected by the M-986, the $\overline{\text{TBLF}}$ output goes low, indicating reception of the tone to the host processor. The host processor can determine which tone was detected and which channel the tone was detected on by reading data

Table 2 2 of 6 Coding Format

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit tone command	1	CHN	F6	F5	F4	F3	F2	F1
Receive tone return	0	CHN	F6	F5	F4	F3	F2	F1

CHN: 1 = channel 2; 0 = channel 1

R1 MF Frequencies:

Bit name	Frequency (Hz)	Bit name	Frequency (Hz)
F6	1700	F3	1100
F5	1500	F2	900
F4	1300	F1	700

Table 3 Binary Coding Format

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit tone command	1	CHN	0	0	A	B	C	D
Receive tone return	0	CHN	0	0	A	B	C	D

CHN: 1 = channel 2; 0 = channel 1

R1 MF Frequencies:

ABCD	Frequencies (Hz)	Name	ABCD	Frequencies (Hz)	Name
0000	Tone off	—	1000	900 & 1500	Digit 8
0001	700 & 900	Digit 1	1001	1100 & 1500	Digit 9
0010	700 & 1100	Digit 2	1010	1300 & 1500	Digit 0
0011	900 & 1100	Digit 3	1011	700 & 1700	ST3
0100	700 & 1300	Digit 4	1100	900 & 1700	ST1
0101	900 & 1300	Digit 5	1101	1100 & 1700	KP
0110	1100 & 1300	Digit 6	1110	1300 & 1700	ST2
0111	700 & 1500	Digit 7	1111	1500 & 1700	ST

from the M-986 coprocessor port. The M-986 will return a single byte indicating the tone received and the channel that the tone was received on. The format of the returned byte depends on whether the M-986 is configured for binary or 2-of-6 coding. See Tables 2 and 3.

Coprocessor Port

Commands are written to the M-986 via the coprocessor port, and data indicating the received R1 MF tone is read from the coprocessor port.

Writing to the Coprocessor Port: The following sequence describes writing a command to the M-986.

- (1) The \overline{WR} signal is driven low by the host processor.
- (2) The \overline{RBLE} (receive buffer latch empty) signal transitions to a logic high level.
- (3) Data is written from D7-D0 to the receive buffer latch (D7-D0) when the WR signal goes high.
- (4) The \overline{RBLE} signal transitions to a logic low level after the M-986 reads the data. This signals the host processor that the receive buffer is empty.

Note: The \overline{RBLE} should be low before writing to the coprocessor.

Reading the Coprocessor Port: The following sequence describes reading received tone information from the coprocessor port.

- (1) The \overline{TBLF} (transmit buffer latch full) port pin on the M-986 goes low indicating the reception of a tone.
- (2) The host processor detects the low logic level on the \overline{TBLF} pin either by polling a connected port pin or by an interrupt.
- (3) The host processor drives the \overline{RD} signal low.
- (4) The \overline{TBLF} (transmit buffer latch full) signal transitions to a logic high level.
- (5) Data is driven onto D7-D0 by the M-986 until the \overline{RD} signal is driven high by the host processor.

Clock Characteristics and Timing

Internal Clock Option: The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN. The frequency of CLKOUT is one-fourth the crystal fundamental frequency. The crystal should be 20.48 MHz, fundamental mode, and parallel resonant, with an effective series resistance of 30 ohms, a power dissipation of 1 mW, and be specified at a load capacitance of 20 pF.

External Clock Option: An external frequency source can be used by injecting the frequency directly in X2/CLKIN with X1 left unconnected. The external frequency injected must conform to the specifications listed in Table 8.

See Section 9 for PLCC package information.

Table 4 Signal Descriptions

SIGNAL	PIN	I/O/Z	DESCRIPTION
D15-D8	18-11	I/O/Z	Unused. Leave open.
D7-D0	19-26	I/O/Z	8-bit coprocessor latch.
\overline{TBLF}	40	O	Transmit buffer latch full flag.
\overline{RBLE}	1	O	Receive buffer latch empty flag
HI/LO	2	I	Latch byte select pin. Tie low.
BIO	9	I	Unused. Leave open.
\overline{RD}	32	I/O	Used by the external processor to read from the coprocessor latch by driving the \overline{RD} line active (low), thus enabling the output latch to drive the latched data. When the data has been read, the external device must bring the \overline{RD} line high.
\overline{EXINT}	5	I	Unused. Leave open.
MC	3	I	Microcomputer mode select pin. Tie low.
MC/PM	27	I	Coprocessor mode select pin. Tie low.
\overline{RS}	4	I	Reset input for initializing the device. When an active low is placed on \overline{RS} pin for a minimum of five clock cycles, \overline{RD} and \overline{WR} are forced high, and the data bus (LD7 through LD0) goes to a high impedance state. The serial port clock and transmit outputs also go to the high impedance state.
\overline{WR}	31	I/O	Used by the external processor to write data to the coprocessor port. To write data the external processor drives the \overline{WR} line low, places data on the data bus, and then drives the \overline{WR} line high to clock the data into the on-chip latch.

Table 4 Signal Descriptions (continued)

SIGNAL	PIN	I/O/Z	DESCRIPTION
XF	28	O	Watchdog signal. Toggles at least once every 10 milliseconds when the processor is functioning properly. If the pin is not toggled at least once every 10 ms, the processor is lost and should be reset.
CLKOUT	6	O	System clock output (one-fourth crystal/CLKIN frequency, nominally 5.12 MHz).
V _{cc}	30	I	5V supply pin.
V _{ss}	10	I	Ground pin.
X1	7	O	Crystal output pin for internal oscillator. If the internal oscillator is not used, this pin should be left unconnected.
X2/CLKIN	8	I	Input pin to the internal oscillator (X2) from the crystal. Alternatively, an input pin for the external oscillator (CLKIN).
DR1 & DR0	33 & 29	I	Serial-port receive-channel inputs. 2.048 MHz serial data is received in the receive registers via these pins. DR0 = channel 1; DR1 = channel 2
DX1 & DX0	36 & 35	O	Serial-port transmit-channel outputs. 2.048 MHz serial data is transmitted from the transmit registers on these pins. These outputs are in the high-impedance state when not transmitting. DX0 = channel 1; DX1 = channel 2
FR	37	O	8 kHz internal serial-port framing output. If internal clocking is selected, serial-port transmit and receive operations occur simultaneously on an active (high) FR framing pulse.
$\overline{\text{FSR}}$	39	I	8 kHz external serial-port receive-framing input. If external clocking is selected, data is received via the receive pins (DR1 and DR0) on the active (low) FSR input. The falling edge of FSR initiates the receive process, and the rising edge causes the M-986 to process the data.
$\overline{\text{FSX}}$	38	I	8 kHz external serial-port transmit-framing input. If external clocking is enabled, data is transmitted on the transmit pins (DX1, DX0) on the active (low) input. The falling edge of FSX initiates the transmit process, and the rising edge causes the M-986 to internally load data for the next cycle.
SCLK	34	I/O/Z	2.048 MHz serial-port clock. Master clock for transmitting and receiving serial-port data. Configured as an input in external clocking mode or output in internal clocking mode. Reset (RS) forces SCLK to the high-impedance state.

Table 5 Absolute Maximum Ratings Over Specified Temperature Range

Supply voltage range, V _{cc}	-0.3 V to 7 V
Input voltage range	-0.3 V to 15 V
Output voltage range	-0.3 V to 15 V
Ambient air temperature range	0 °C to 70 °C
Storage temperature range	-45 °C to 150 °C

Table 6 Recommended Operating Conditions

Parameter		Min	Nom	Max	Unit
V _{CC}	Supply voltage	4.75	5	5.25	V
V _{SS}	Supply voltage		0		V
V _{IH}	High-level input voltage	All inputs except CLKIN	2		V
		CLKIN	3		V
		MC/PM	2.2		V
V _{IL}	Low-level input voltage	All inputs except MC/MP		0.8	V
		MC/MP		0.6	V
I _{OH}	High-level output current (all outputs)			-300	μA
I _{OL}	Low-level output current (all outputs)			2	mA
T _A	Operating free-air temperature	0		70	°C

Table 7 Electrical Characteristics Over Specified Temperature Range

Parameter		Test Conditions	Min	Typ	Max	Unit
I _{CC}	Supply current	f = 20.5 MHz, V _{CC} = 5.5V, T _A = 0 ° to 70 ° C		50	75	mA
V _{OH}	High-level output voltage	I _{OH} = MAX	2.4	3		V
		I _{OH} = 20 μA	V _{CC} - 0.4			V
V _{OL}	Low-level output voltage	I _{OL} = MAX		0.3	0.6	V
I _{OZ}	Off-state output current	V _{CC} = MAX	V _O = 2.4 V		20	μA
			V _O = 0.4 V		-20	μA
I _I	Input current	V _I = V _{SS} to V _{CC}	Except CLKIN		±20	μA
			CLKIN		±50	μA
C _I	Input capacitance	Data bus	f = 1 MHz, all other pins 0 V	25		pF
		All others		15		pF
C _O	Output capacitance	Data bus		25		pF
		All others		10		pF

Table 8 External Frequency Specifications

Parameter		Min	Nom	Max	Unit
t _{C(MC)}	Master clock cycle time	48.818	48.828	48.838	ns
t _{r(MC)}	Rise time master clock input		5	10	ns
t _{p(MC)}	Pulse duration master clock	20			ns

Table 9 Serial Port Timing

Parameter		Min	Nom	Max	Unit
t_d (CH-FR)	Internal framing delay from SCLK rising edge			70	ns
t_d (DX1-CL)	DX bit 1 valid before SCLK falling edge	20			ns
t_d (DX2-CL)	DX bit 2 valid before SCLK falling edge	20			ns
t_h (DX)	DX hold time after SCLK falling edge	244			ns
t_{su} (DR)	DR setup time before SCLK falling edge	20			ns
t_h (DR)	DR hold time after SCLK falling edge	20			ns
t_c (SCLK)	Serial port clock cycle time	399	488.28	4770	ns
t_f (SCLK)	Serial port clock fall time			30	ns
t_r (SCLK)	Serial port clock rise time			30	ns
t_w (SCLKL)	Serial port clock low-pulse duration*	220	244.14	2500	ns
t_w (SCLKH)	Serial port clock high-pulse duration*	220	244.14	2500	ns
t_{su} (FS)	FSX/FSR setup time before SCLK falling edge	100			

* The duty cycle of the serial port clock must be within 45% to 55%.

Table 10 Coprocessor Interface Timing

Parameter		Min	Nom	Max	Unit
t_d (R-A)	RD low to TBLF high			75	ns
t_d (W-A)	WR low to RBLE high			75	ns
t_a (RD)	RD low to data valid			80	ns
t_h (RD)	Data hold time after RD high	25			ns
t_{su} (WR)	Data setup time prior to WR high	30			ns
t_h (WR)	Data hold time after WR high	25			ns
t_w (RDL)	RD low-pulse duration	80			ns
t_w (WRL)	WR low-pulse duration	60			ns
t_{wr} (RBLE)	RBLE \uparrow to RBLE \downarrow			1	ms

Table 11 Reset (RS) Timing

Parameter		Test Conditions	Min	Max	Unit
t_{dis} (R)	Data bus disable time after RS	$R_L = 825 \Omega$ $C_L = 100 \text{ pF}$		75	ns
t_{d12}	Delay time from RS \downarrow to high-impedance SCLK			200	ns
t_{d13}	Delay time from RS \downarrow to high-impedance DX1, DX0			200	ns
t_{su} (R)	Reset (\overline{RS}) setup time prior to CLKOUT		50		ns
t_w (R)	RS pulse duration		245		ns

Table 12 CLKOUT Timing Parameters

Parameter		Test Conditions	Min	Nom	Max	Unit
$t_{c(C)}$	CLKOUT cycle time	$R_L = 825 \Omega$ $C_L = 100 \text{ pF}$	195.27	195.31	195.35	ns
$t_r(C)$	CLKOUT rise time			10		ns
$t_f(C)$	CLKOUT fall time			8		ns
$t_d(MCC)$	Delay time CLKIN \uparrow to CLKOUT \downarrow		25		60	ns
t_{dS}	Delay time CLKOUT \downarrow to data bus OUT valid				$\frac{1}{4} t_{c(C)} + 75$	ns

Table 13 Transmitter Characteristics

	Parameter	Test Conditions	Min	Typ	Max	Unit
FOS	Frequency offset	From nominal			± 1	Hz
TW	Twist	High/low			± 0.5	dB
AS	Signal amplitude	Per component	-7.40	-7.00	-6.60	dBm0
T _S	Time skew	Between components			0	ms
Phi	Power due to extraneous components				-30	dB

Table 14 Receiver Characteristics

	Parameter	Test Conditions	Min	Max	Unit
A _d	Detect amplitude	Per frequency	-30	-5	dBm0
A _{nd}	No-detect amplitude	Per frequency	-40	-30	dBm0
F _d	Detect with frequency offset	From nominal	$\pm 1.5\%$ $+5\text{Hz}$		Hz
TW _d	Detect with twist	High tone/low tone	± 6		dB
T _{on}	Tone time	Reject	10		ms
T _{int}	Interrupted tone time	Reject	10		ms
T _i	Tone interpulse time		25		ms
KPL _d	KP long tone detect time	Long detect time enabled	55		ms
KP _d	KP short tone detect time	Long detect time disabled	30		ms
T _d	Tone detect time		30		ms
N _t	Noise tolerance	≤ 1 error in 25,000 digits		-20	dB
N _i	Impulse noise	≤ 1 error in 25,000 digits		-12	dB
P ₆₀	60 Hz tolerance	≤ 1 error in 25,000 digits		81	dB _{Brnc0}
T ₁₈₀	180 Hz tolerance	≤ 1 error in 25,000 digits		68	dB _{Brnc0}
M _t	Modulation products tolerance	2A-B and 2B-A products		-28	dB

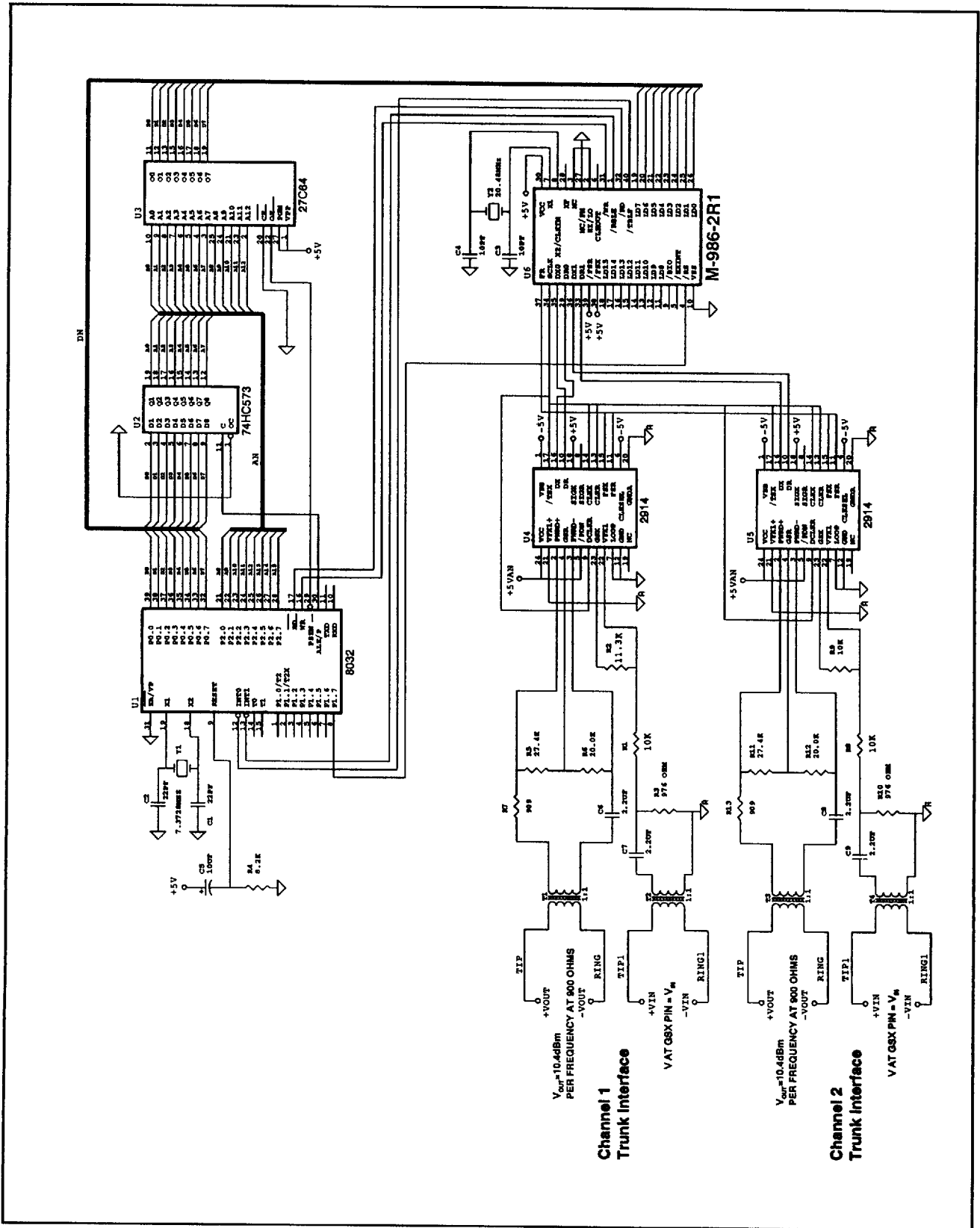
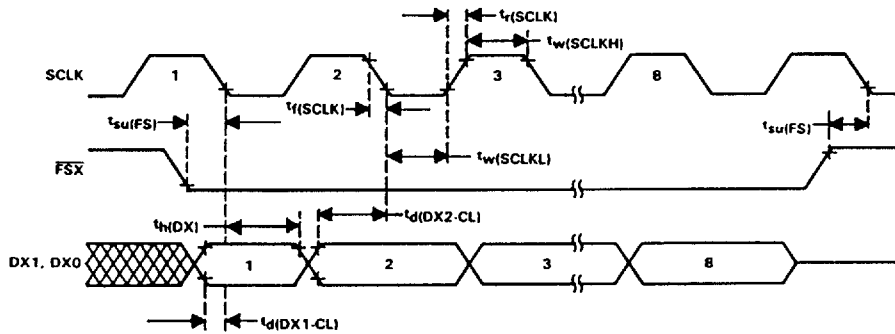


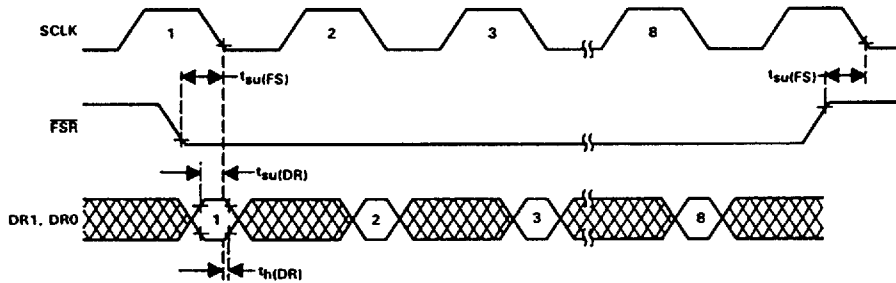
Figure 2 M-986 Dual Channel 4-wire Interface Application Circuit

External Framing: Transmit Timing



NOTES: Data valid on transmit outputs until SCLK rises.
The most significant bit is shifted first.

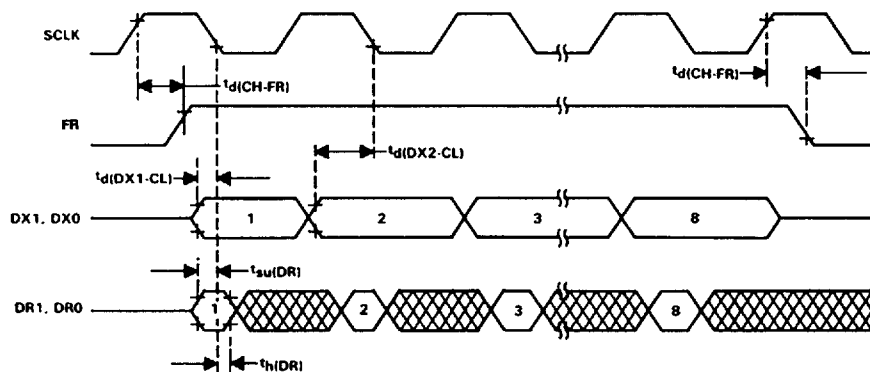
External Framing: Receive Timing



NOTE: The most significant bit is shifted first.

Figure 3 External Framing Timing Diagrams

Internal Framing



NOTE: The most significant bit is shifted first.

Figure 4 Internal Framing Timing

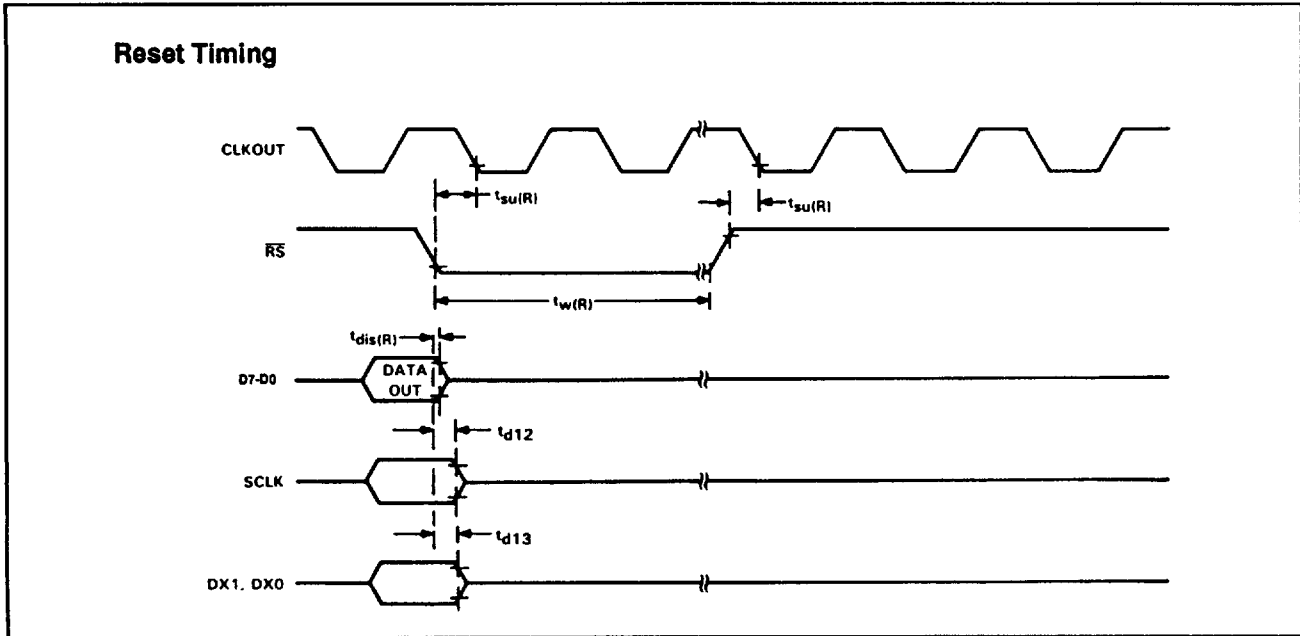


Figure 5 Reset Timing

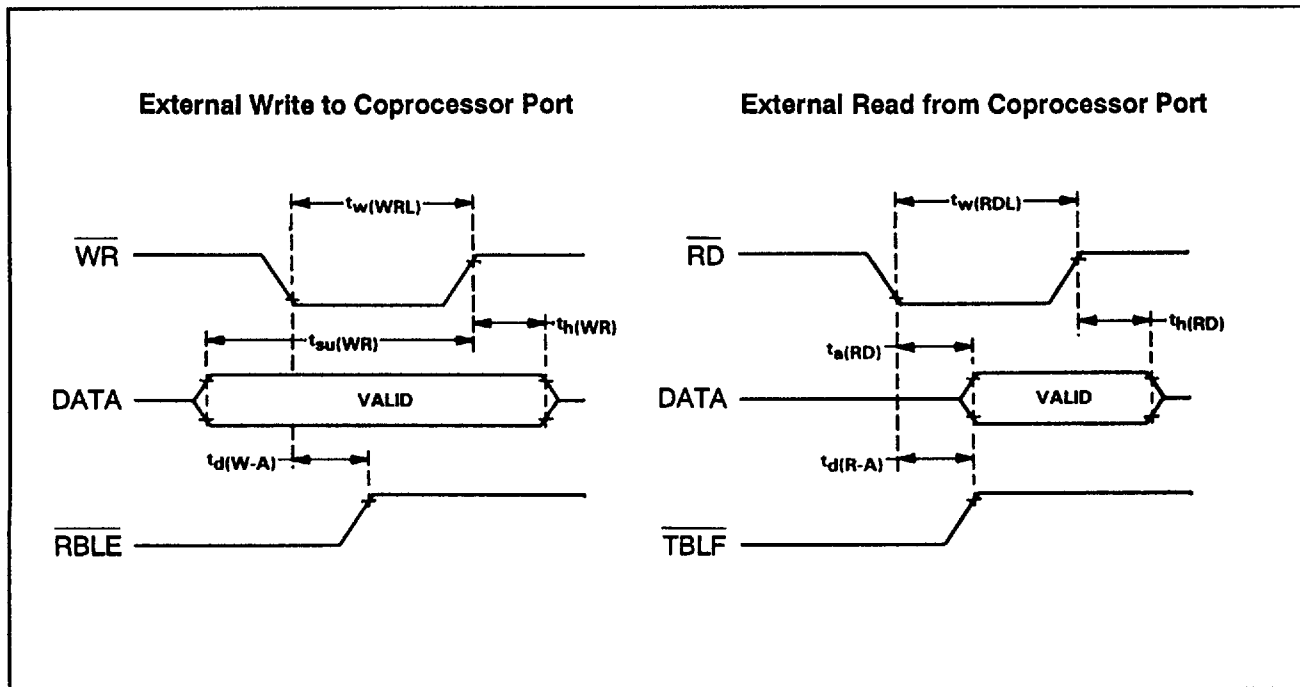


Figure 6 Coprocessor Timing

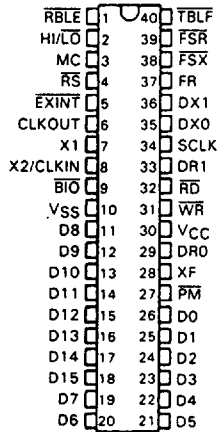
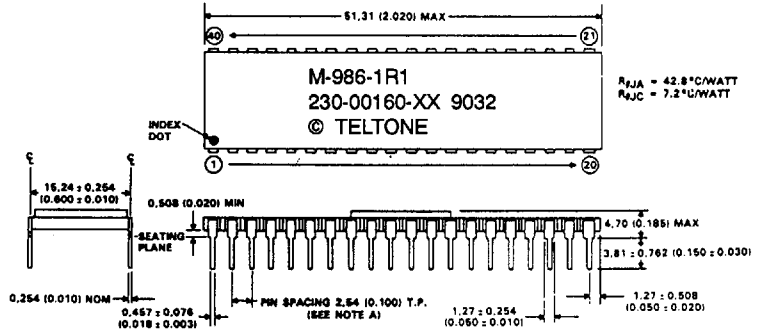


Figure 7 Pin Assignments



NOTE A: Each pin centerline is located within 0.254 (0.010) of its true longitudinal position.
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

PLCC, CLCC 44-PIN PACKAGES AVAILABLE.
CALL TELTONE FOR PIN CONFIGURATION DETAILS.

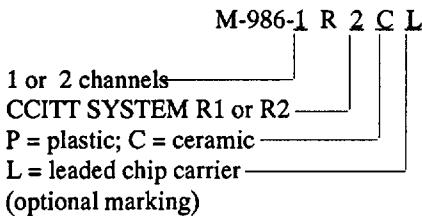
Figure 8 Package Dimensions

See Section 9 for PLCC package information.

Flammability/Reliability Specifications

Reliability: 185 FITS failures/billion hours
Flammability: Passes UL 94 V-0 tests

Ordering Information



A-law/ μ -law version available.
Call for information.

MF Signaling References

1. CCITT Blue Book, Fascicle VI.4 Q.310 - Q.490. Contains specifications of signaling systems R1 and R2. If not available at your local university library, contact:
OMNICOM
115 Park Street S.E.
Vienna, VA 22180
1-703 -281-1135
2. Bellcore Technical Publications. 1-800-521-2673
TR-NPL-000275—Notes on the Network (primarily deals with MF R1 because it pertains to the U.S. domestic Telco market.
3. Reference Manual for Telecommunications by Roger L. Freeman, ISBN-0-471-86753-5