4M × 1 Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

- **Performance range:**

	t_{RAC}	t_{CAC}	t_{RC}
KM41C4002C-5	50ns	13ns	90ns
KM41C4002C-6	60ns	15ns	110ns
KM41C4002C-7	70ns	20ns	130ns
KM41C4002C-8	80ns	20ns	150ns

- **Static Column Mode operation**
- **$\overline{\text{CS}}$-before-$\overline{\text{RAS}}$ refresh capability**
- **$\overline{\text{RAS}}$-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Commom I/O using Early Write**
- **Single +5.0V±10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**
- **Available in plastic SOJ, ZIP and TSOP(II) Packages**

GENERAL DESCRIPTION

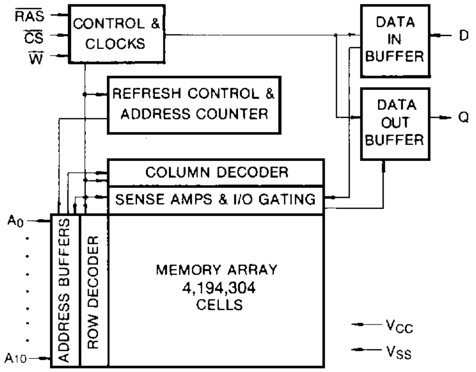
The Samsung KM41C4002C is a CMOS high speed 4,194,304 × 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C4002C features Static Column Mode operation which allows high speed random or Sequential access within a row. Static Column Mode operation offers high performance while relaxing many critical system timing requirements for fast usable speed.

$\overline{\text{CS}}$-before-$\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$-only refresh. All inputs and output are fully TTL compatible.

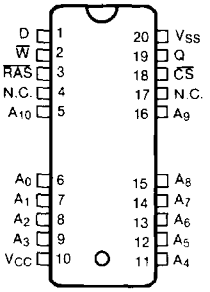
The KM41C4002C is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

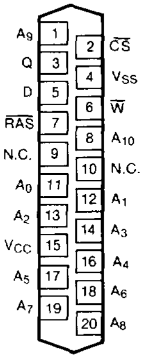


PIN CONFIGURATION (Top Views)

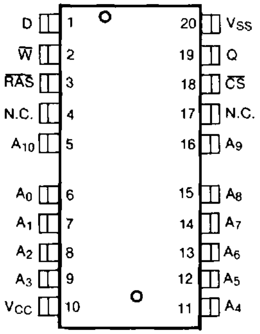
• **KM41C4002CJ**



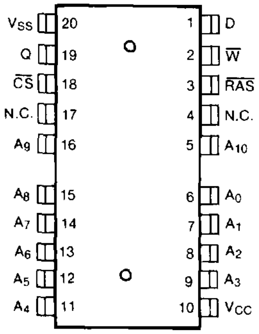
• **KM41C4002CZ**



• **KM41C4002CT**



• **KM41C4002CTR**



Pin Names	Pin Function
A_0-A_{10}	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1	V
Input Low Voltage	V_{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @t_{RC}=min.)	KM41C4002C-5	I_{CC1}	-	85	mA
	KM41C4002C-6		-	75	mA
	KM41C4002C-7		-	65	mA
	KM41C4002C-8		-	55	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$=V_{IH})		I_{CC2}	-	2	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CS}$=V_{IH}, $\overline{RAS}$, Address Cycling @t_{RC}=min.)	KM41C4002C-5	I_{CC3}	-	85	mA
	KM41C4002C-6		-	75	mA
	KM41C4002C-7		-	65	mA
	KM41C4002C-8		-	55	mA
Static Column Mode Current* ($\overline{RAS}$=$\overline{CS}$=V_{IL}, Address Cycling @t_{PC}=min.)	KM41C4002C-5	I_{CC4}	-	65	mA
	KM41C4002C-6		-	55	mA
	KM41C4002C-7		-	45	mA
	KM41C4002C-8		-	35	mA
Standby Current ($\overline{RAS}$=$\overline{CS}$=$\overline{W}$=V_{CC}-0.2V)		I_{CC5}	-	1	mA
$\overline{CS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CS}$ Cycling @t_{RC}=min.)	KM41C4002C-5	I_{CC6}	-	85	mA
	KM41C4002C-6		-	75	mA
	KM41C4002C-7		-	65	mA
	KM41C4002C-8		-	55	mA
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{CC}$+0.5V, all other pins not under test=0 volts.)		$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)		$I_{O(L)}$	-10	10	μA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. I_{CC1}, I_{CC3}, I_{CC6} Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. In I_{CC4}, Address can be changed maximum once during a Static Column mode cycle.

CAPACITANCE (T_A=25 C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance(D)	C_{IN1}	-	5	pF
Input Capacitance (A_0~A_{10})	C_{IN2}	-	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{W}$)	C_{IN3}	-	7	pF
Input Capacitance (Q)	C_{OUT}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	108		130		150		170		ns	
Static column mode cycle time	t_{SC}	30		35		40		45		ns	
Static column mode read-write cycle time	t_{SRWC}	53		65		75		85		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
Access time from last write	t_{ALW}		50		55		65		75	ns	3
$\overline{CS}$ to output in Low-Z	t_{CLZ}	0		0		0		0		ns	7
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	20	0	20	ns	2
Output data hold time from column address	t_{AOH}	5		5		5		5		ns	
Output data enable time from $\overline{W}$	t_{OW}		35		40		45		55	ns	
Output data hold time from $\overline{W}$	t_{WOH}	0		0		0		0		ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ pulse width(static column mode)	t_{RASC}	50	100,000	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15		20		20		ns	
$\overline{CS}$ hold time	t_{CSH}	50		60		70		80		ns	
$\overline{CS}$ pulse width	t_{CS}	13	10,000	15	10,000	20	10,000	20	10,000	ns	
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	13	100,000	15	100,000	20	100,000	20	100,000	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	11
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		5		ns	
$\overline{CS}$ precharge time (static column mode)	t_{CP}	10		10		10		10		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold	t_{CAH}	10		10		15		15		ns	
Write address hold time referenced to $\overline{RAS}$	t_{AWR}	40		45		55		60		ns	6

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Column address hold time referenced to $\overline{\text{RAS}}$	t_{AR}	60		70		80		90		ns	
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	25		30		35		40		ns	
Column address hold time referenced to $\overline{\text{RAS}}$ rise.	t_{AH}	5		5		5		5		ns	
Last Write to column address to delay time	t_{LWAD}	20	25	20	30	20	35	20	40	ns	12
Last write to column address gold time	t_{AHLW}	50		55		65		75		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time referenced to $\overline{\text{CS}}$	t_{RCH}	0		0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	t_{RRH}	0		0		0		0		ns	9
Write command hold time	t_{WCH}	10		10		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	t_{WCR}	40		45		55		60		ns	6
Write command pulse width	t_{WP}	10		10		15		15		ns	
Write command inactive time	t_{WI}	10		10		10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	15		15		15		15		ns	
Write command to $\overline{\text{CS}}$ lead time	t_{CWL}	13		15		15		15		ns	
Data-in set-up time	t_{DS}	0		0		0		0		ns	10
Data-in hold time	t_{DH}	10		10		15		15		ns	10
Data-in hold time referenced to $\overline{\text{RAS}}$	t_{DHR}	40		45		55		60		ns	6
Refresh period (1024 cycles)	t_{REF}		16		16		16		16	ms	
Write command set-up time	t_{WCS}	0		0		0		0		ns	8
$\overline{\text{CS}}$ to $\overline{\text{W}}$ delay time	t_{CWD}	13		15		15		15		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	t_{RWD}	50		60		70		80		ns	8
Column address to $\overline{\text{W}}$ delay time	t_{AWD}	25		30		35		40		ns	8
$\overline{\text{CS}}$ setup time ($\overline{\text{CS}}$-before-$\overline{\text{RAS}}$ refresh)	t_{CSR}	10		10		10		10		ns	
$\overline{\text{CS}}$ hold time ($\overline{\text{CS}}$-before-$\overline{\text{RAS}}$ refresh)	t_{CHR}	10		10		10		10		ns	
Write command set-up time (test mode in)	t_{WTS}	10		10		10		10		ns	
Write command hold time (test mode in)	t_{WTH}	10		10		10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time ($\overline{\text{CS}}$-before-$\overline{\text{RAS}}$ cycle)	t_{WRP}	10		10		10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time ($\overline{\text{CS}}$-before-$\overline{\text{RAS}}$ cycle)	t_{WRH}	10		10		10		10		ns	
$\overline{\text{RAS}}$ precharge to $\overline{\text{CS}}$ hold time	t_{RPC}	5		5		5		5		ns	
Refresh counter test $\overline{\text{CS}}$ precharge time	t_{CPT}	20		20		25		30		ns	

TEST MODE CYCLE

(Note.13)

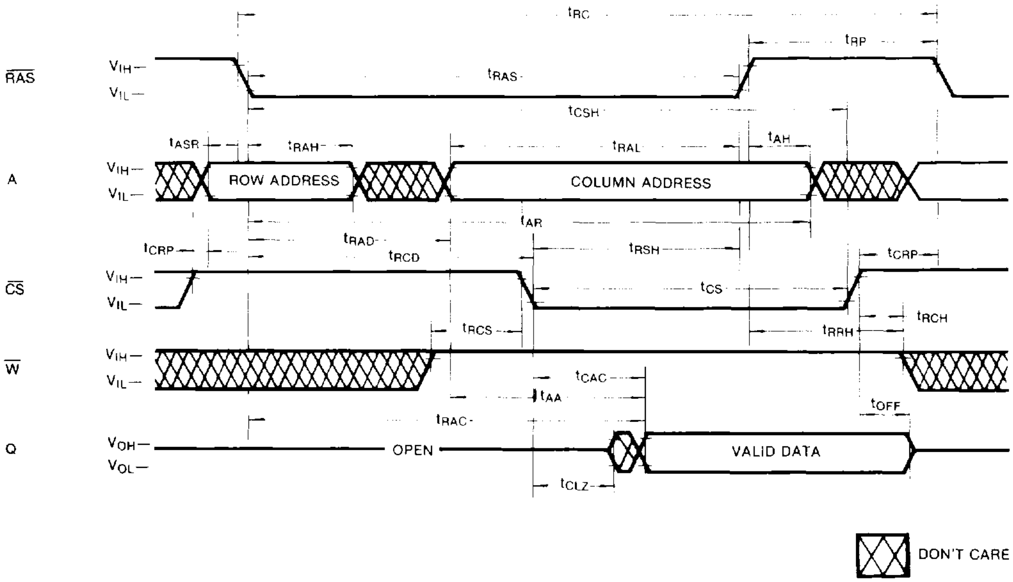
Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	95		115		135		155		ns	
Read-modify-write cycle time	t_{RWC}	113		135		155		175		ns	
Access time from $\overline{RAS}$	t_{RAC}		55		65		75		85	ns	3,4,11
Access time from $\overline{CS}$	t_{CAC}		18		20		25		25	ns	3,4,5
Access time from column address	t_{AA}		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	t_{RAS}	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CS}$ pulse width	t_{CS}	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		20		25		25		ns	
$\overline{CS}$ hold time	t_{CSH}	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		45		ns	
$\overline{CS}$ to Write enable delay	t_{CWD}	18		20		20		20		ns	8
$\overline{RAS}$ to Write enable delay	t_{RWD}	55		65		75		85		ns	8
Column address to $\overline{W}$ delay time	t_{AWD}	30		35		40		45		ns	8
Static column mode cycle time	t_{SC}	35		40		45		50		ns	
Static column mode read-modify-write	t_{SRWC}	58		70		80		90		ns	
$\overline{RAS}$ pulse width (Static column mode)	t_{RASC}	55	100,000	65	100,000	75	100,000	85	100,000	ns	
Access time from last write	t_{ALW}		55		65		75		85	ns	3,12
$\overline{CS}$ pulse width (static column mode)	t_{CSC}	18	100,000	20	100,000	25	100,000	25	100,000	ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{CBR}$ or $\overline{ROR}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AWR}, t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$
7. This parameter defines the time at which the output achieves the open circuit condition and is not refernced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(min)$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
12. Operation within the $t_{LWAD(max)}$ limit insures that $t_{ALW(max)}$ can be met. $t_{LWAD(max)}$ is specified as a reference point only. t_{LWAD} is greater than the specified $t_{LWAD(max)}$ limit, then access time is controlled by t_{AA}.
13. These specifications are applied in the test mode.

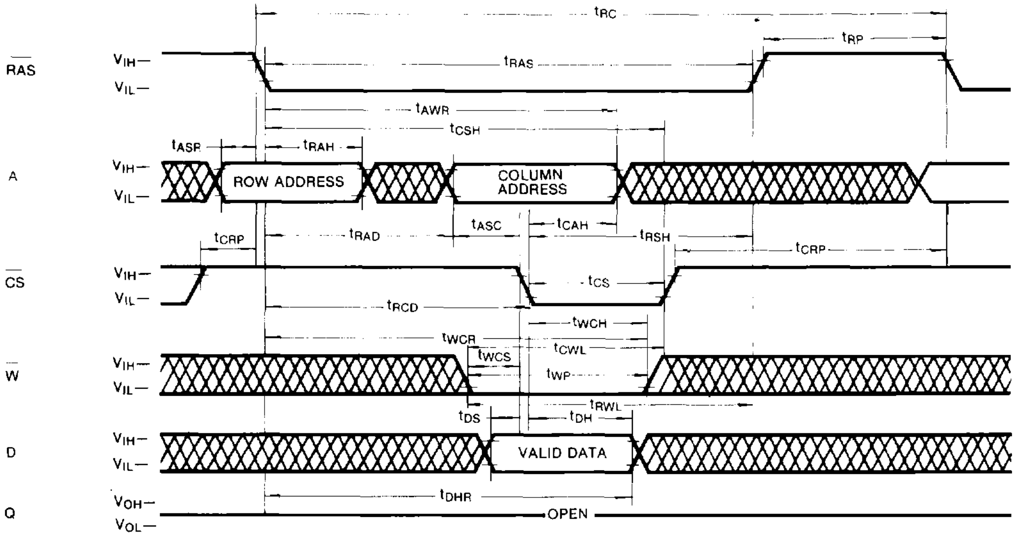
TIMING DIAGRAMS

READ CYCLE

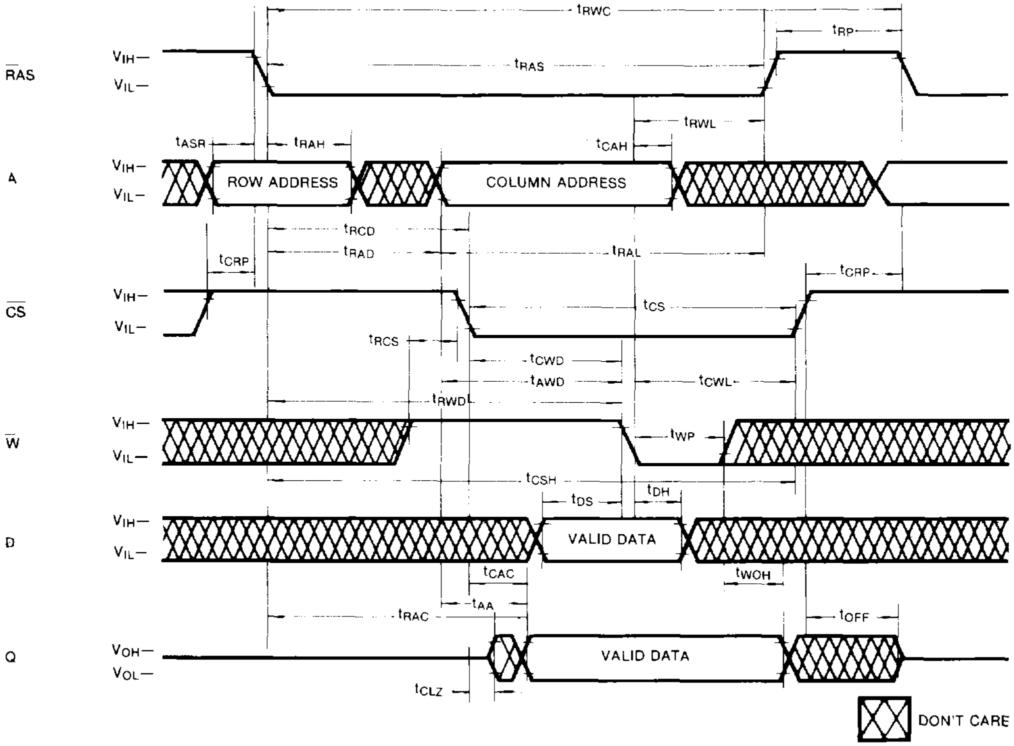


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)

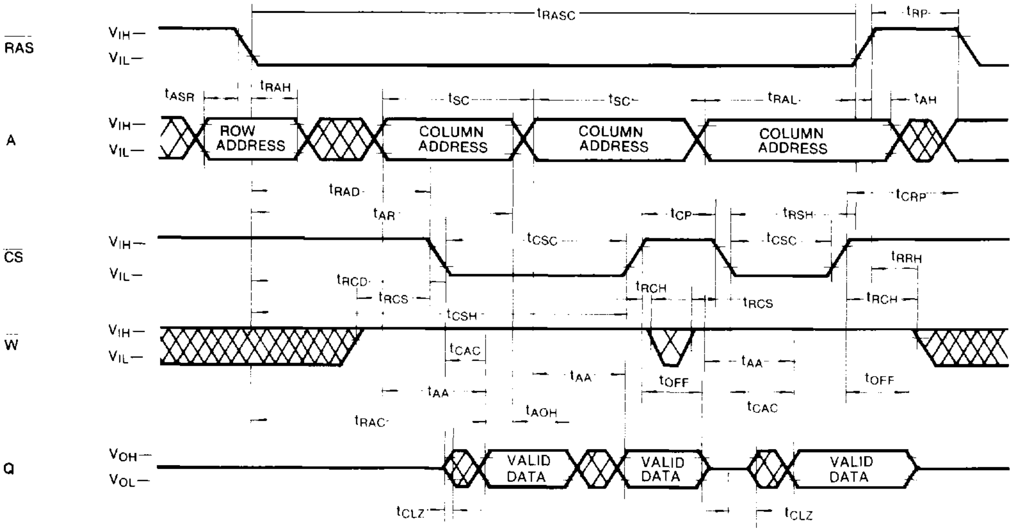


READ-WRITE/READ-MODIFY-WRITE CYCLE

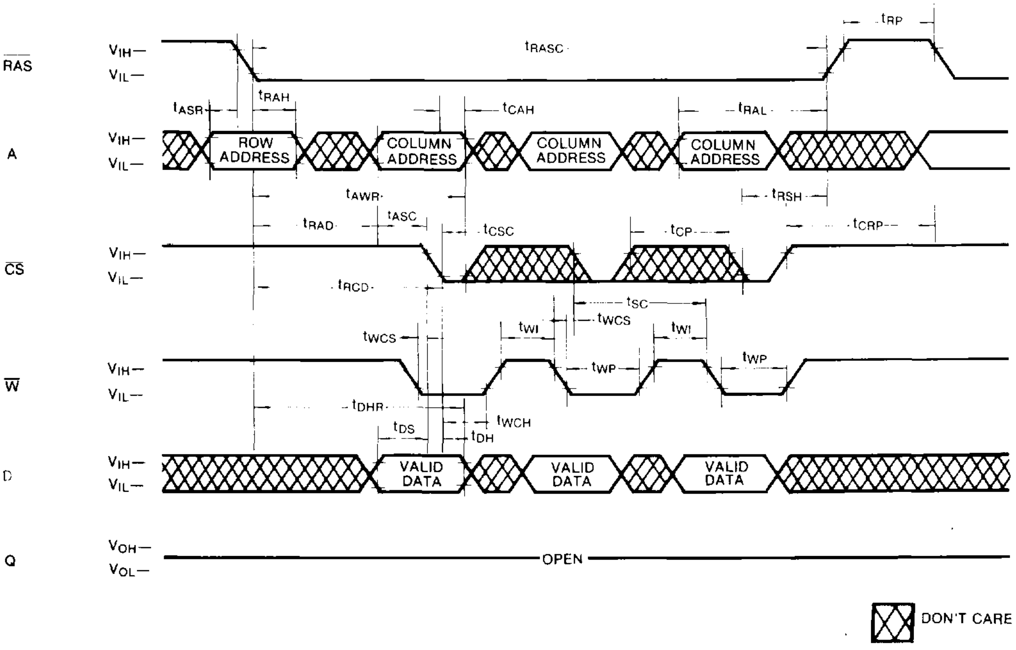


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ CYCLE

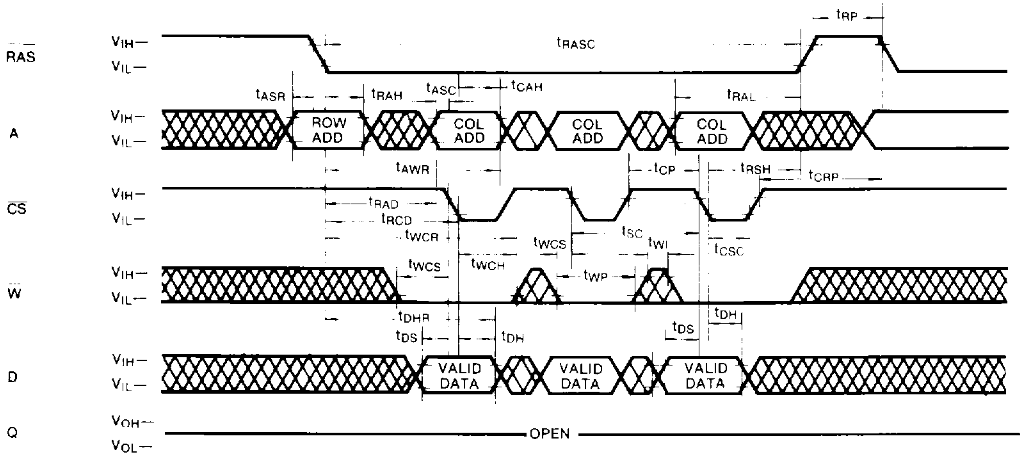


STATIC COLUMN MODE WRITE CYCLE ($\overline{W}$ controlled early write)

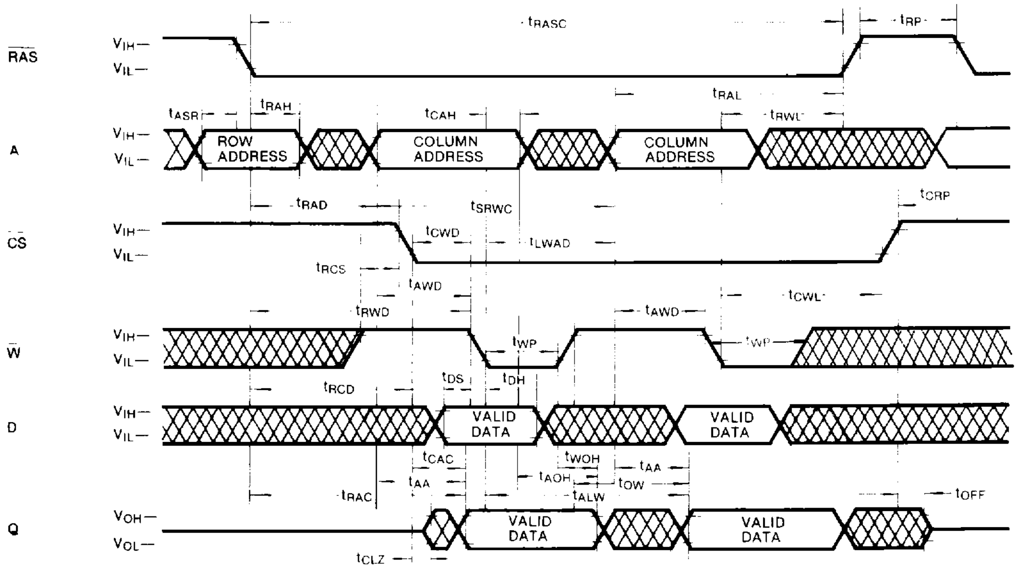


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE ($\overline{CS}$ controlled early write)



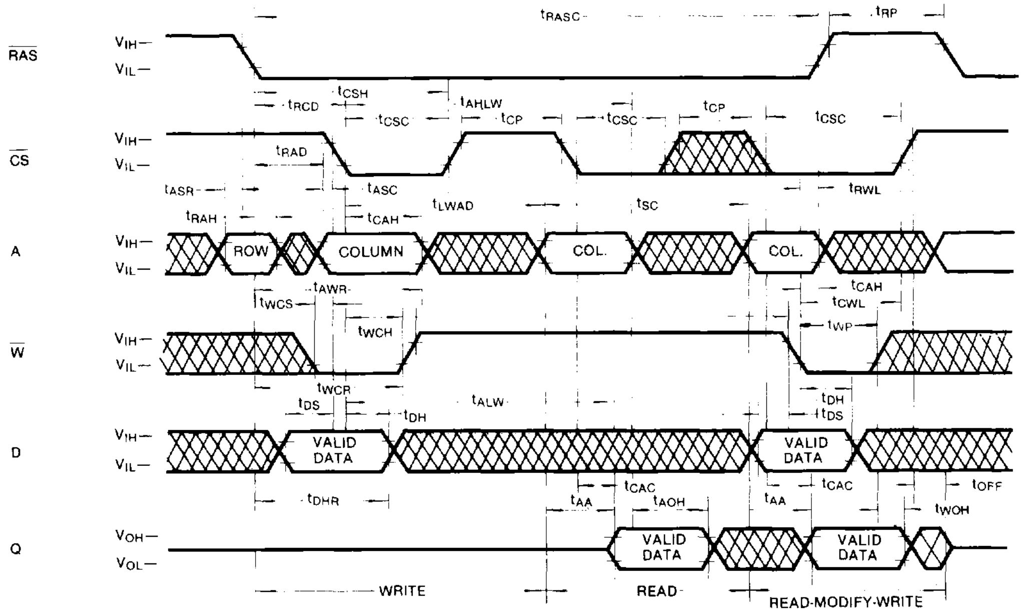
STATIC COLUMN MODE READ-WRITE CYCLE



▨ DON'T CARE

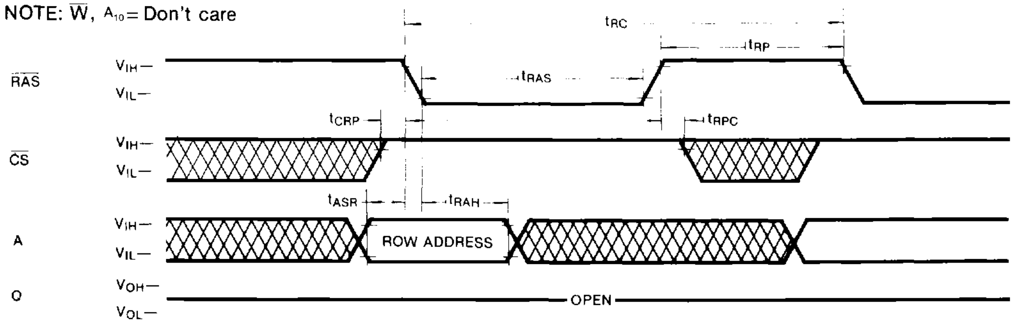
TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE MIXED CYCLE



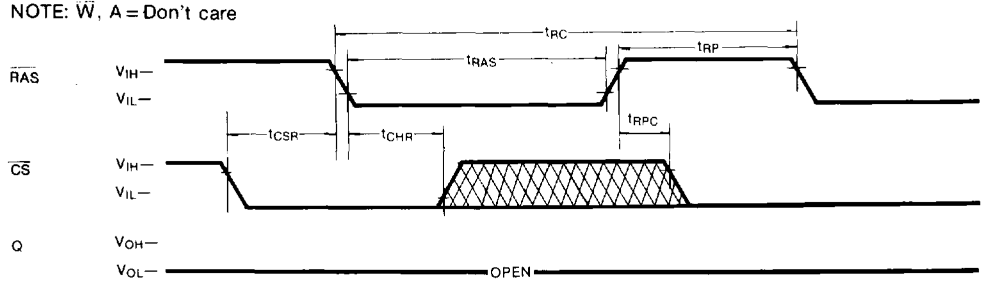
RAS-ONLY REFRESH CYCLE

NOTE: W, A_{10} = Don't care



CS-BEFORE-RAS REFRESH CYCLE

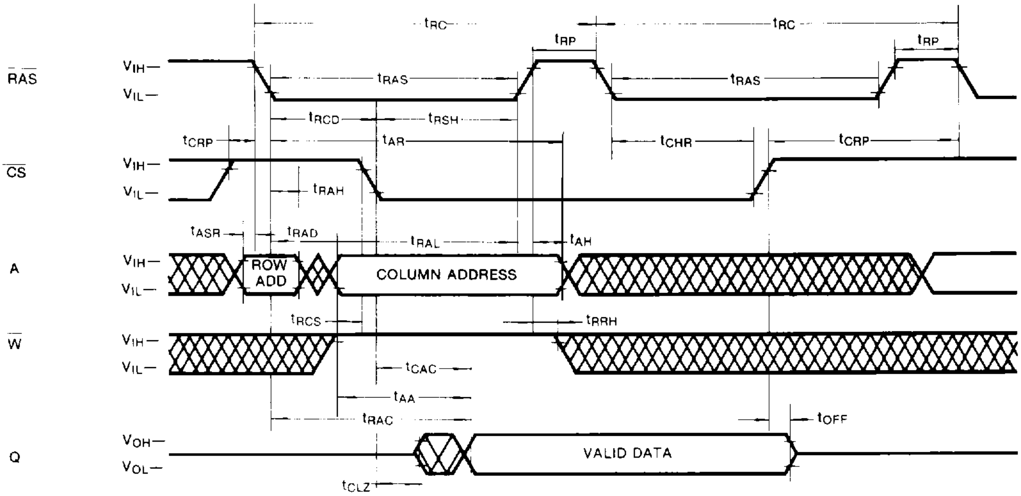
NOTE: W, A = Don't care



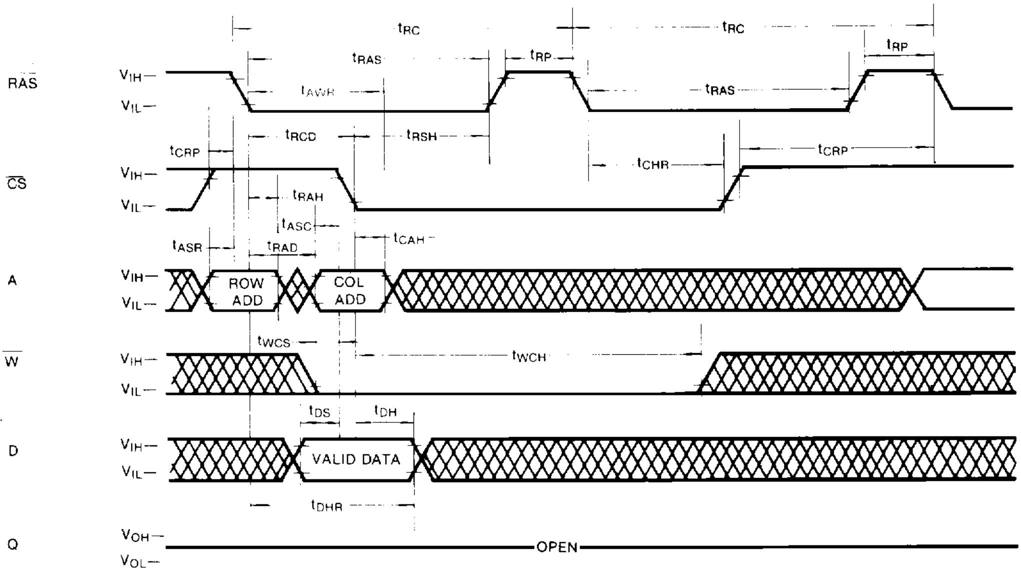
▨ DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



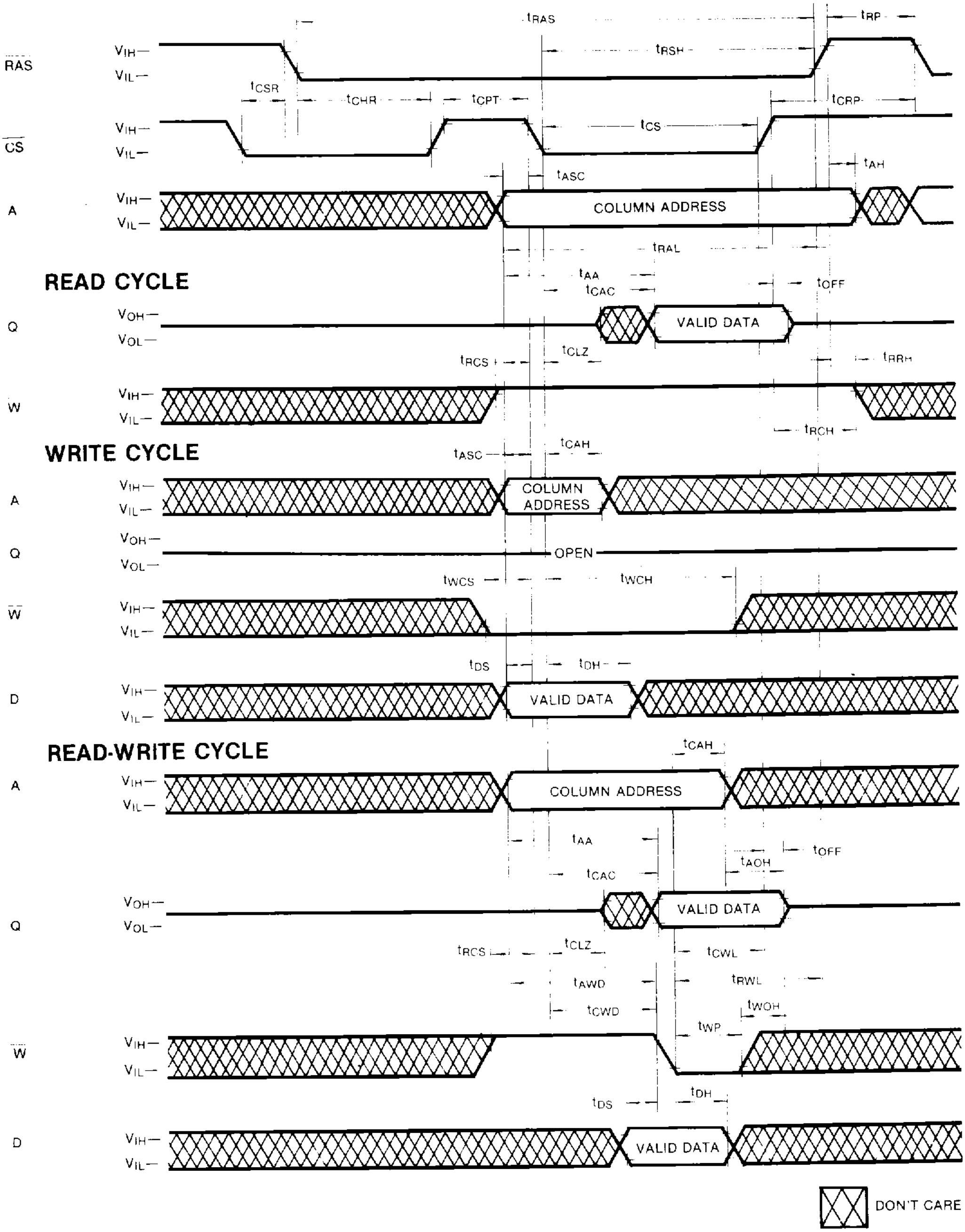
HIDDEN REFRESH CYCLE (WRITE)



▨ DON'T CARE

TIMING DIAGRAMS (Continued)

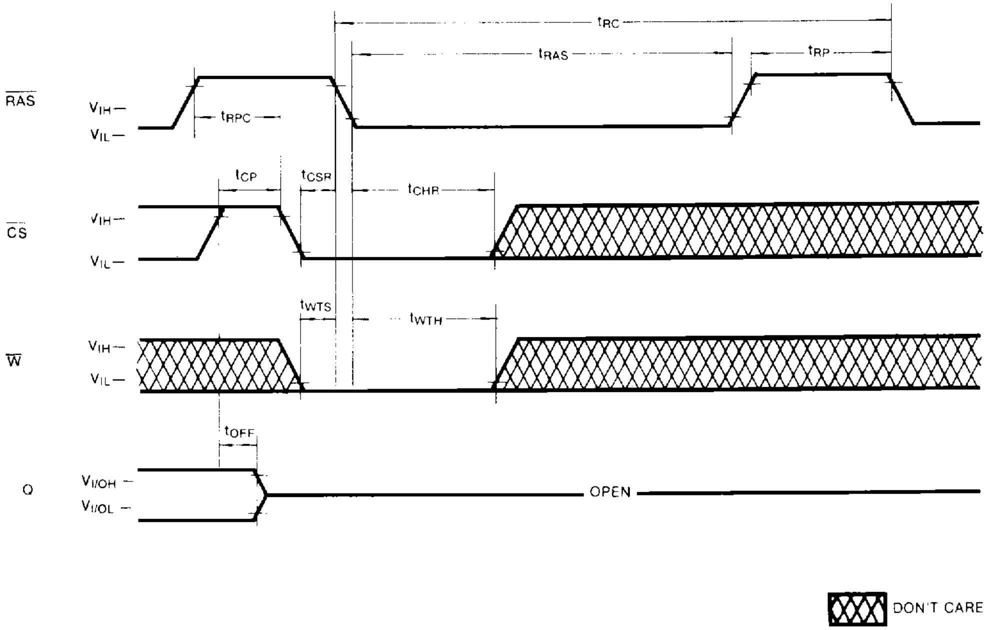
$\overline{\text{CS}}$-BEFORE-$\overline{\text{RAS}}$ BEFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D, Address=Don't Care



TEST MODE DESCRIPTION

The KM41C4002C is the RAM organized 4,194,304 words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A_{10R}, A_{10C} and A_{0C} are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed, the data output pin would indicate a "0" in "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM. $\overline{W}$, $\overline{CS}$-Before-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CS}$-Before-$\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/8 in cases of N test pattern).

DEVICE OPERATION

Device Operation

The KM41C4002C contains 4,194,304 memory locations. Twenty-two address bits are required to address a particular memory location. Since the KM41C4002C has only 11 address input pins, time multiplexed addressing is used to input 11 row and 11 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{\text{RAS}}$), the chip select input($\overline{\text{CS}}$) and the valid row and column address inputs.

Operation of the KM41C4002C begins by strobing in a valid row address with $\overline{\text{RAS}}$ while $\overline{\text{CS}}$ remains high. Then the address on the 11 address input pins is changed from a row address to a column address and is strobed in by $\overline{\text{CS}}$. This is the beginning of any KM41C4002C cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{\text{RAS}}$ and $\overline{\text{CS}}$ have returned to the high sta5e. Another cycle can be initiated after $\overline{\text{RAS}}$ remains high long enough to satisfy the $\overline{\text{RAS}}$ precharge time (tRP) requirement.

$\overline{\text{RAS}}$ and $\overline{\text{CS}}$ Timing

The minimum $\overline{\text{RAS}}$ and $\overline{\text{CS}}$ pulse widths are specified by tRAS(min) and tCS(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initated by bringing $\overline{\text{RAS}}$ low, it must not be aborted prior to satisfying the minimum $\overline{\text{RAS}}$ and $\overline{\text{CS}}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{\text{RAS}}$ precharge time, tRP, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C4002C bigin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input($\overline{\text{W}}$) high during a $\overline{\text{RAS}}$/$\overline{\text{CS}}$ cycle. If $\overline{\text{CS}}$ goes low before tRCD(max), the access time to valid data is specified with respect to the falling edge of $\overline{\text{RAS}}$. But the addess time also depends on the falling edge of $\overline{\text{CS}}$ and on the valid column address transition.

If $\overline{\text{CS}}$ goes low before tRCD(max) and if the column address is valid before tRAD(max) then the access time to valid data is specified by tRAC(min). However, if $\overline{\text{CS}}$ goes low after tRCD(max) or if the column address becomes valid after tRAD(max), access is specified by tCAC or tAA. In order to achieve the minimum access time, tRAC(min), it is necessary to meet both tRCD(max) and tRAD(max).

Write

The KM41C4002C can perform early write, late write and read-modify-write cycles. The differece between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{\text{W}}$ and $\overline{\text{CS}}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{\text{W}}$ or $\overline{\text{CS}}$, whichever is later.

Early Write: An early write cycle is performed by bringing W low before $\overline{\text{CS}}$. The data at the data input pin(D) is wirtten into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the daaressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{\text{W}}$ low after $\overline{\text{CS}}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{\text{W}}$ is brought low after $\overline{\text{CS}}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, tCWD and tAWD are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C4002C has a three-state output buffer which is controlled by $\overline{\text{CS}}$. Whenever $\overline{\text{CS}}$ is high(VIH) the output is in the high impedance(Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by tCLZ after the falling edge of $\overline{\text{CS}}$. Invalid data may be present at the output during the time after tCLZ and before the valid data appears at the output. The timing parameters tCAC, tRAC and tAA specify when the valid data will be present at the output. The valid data remains at the output until $\overline{\text{CS}}$ returns high. This is true even if a new $\overline{\text{RAS}}$ cycle occurs (as in hidden refresh). Each of the KM41C4002C operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Static Column Mode Read, Static Column Mode Read-Modify-Write.

DEVICE OPERATION (Continued)

Hi-Z Output State: Early Write, RAS-only Refresh, Static Column Mode Write, CS-before-RAS Refresh, CS-only cycle.
Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C4002C is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16ms. There are several ways to accomplish this.

RAS-Only-Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with RAS while CS remains high. This cycle must be repeated for each row.

CS-before-RAS Refresh: The KM41C4002C has CS-Before-RAS on-chip refresh capability that eliminates the need for external refresh addresses. If CS is held low for the specified set up time (t_{CSR}) before RAS goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next CS-before-RAS refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the CS active time and cycling RAS. The KM41C4002C hidden refresh cycle is actually CS-before-RAS refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C4002C by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantateous to perform refresh in this mammer but in gheneral RAS-only or CS-before-RAS refresh is the preferred method.

Static Column Mode

Static Column Mode allows high speed read, write or read-modity-write random access to all the memory cells within a selected row. Operation within a selected row is similar to a static RAM. The read, write or readmodify-write cycles may be mixed in any order.
A Static Column mode read cycles starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while W=V_{IH} and RAS=V_{IL}.

A Static Column mode write cycle starts as a normal cycle. Additional cells within the selected ro are written by applying a new column address while RAS=V_{IL} and toggiling either W or CS. The data is written into the cell trigered by the latter fallin edge of W or CS.

CS-before-RAS Refresh Counter Test Cycle

A special timing sequence using the CS-before-RAS refresh counter test cycle provides a convenient method of verifying the functionality of the CS-befofore-RAS refresh activated circuitry.

After the CS-before-RAS refresh operation, is cs goes high and then low again while RAS is held low, the read and write operations are enabled.

This is shown in the CS-before-RAS counter test cycle timing diagram. A memory cell can be addressed with 11 row address bits and 11 column address bits defined as follows.

Row Address — Bits A0 through A9 are supplied by the on-chip refresh counter. The A10 bit is set High internally.

Column Address — Bits A0 through A10 are strobed-in by the falling edge of CS as in a normal memory cycle.

Suggested CS-before-RAS Counter Test Procedure

The CS-before-RAS refresh counter test cycle timing is used in each of the following steps:

1. nitialize the internal refresh counter by performing 8 cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 512 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 512 times so that highs are written into the 512 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2,3 and 4

Power-up

If RAS= Vss during power-up, the KM41C4002C could begin an active cycle. This coundition results in higher than necessary current demands from the power supplu during power-up. It is recommended that RAS and CS track with Vcc during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

DEVICE OPERATION (Continued)

An initial pause of 200μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{\text{RAS}}$ cycles. An initialization cycle is any cycle in which $\overline{\text{RAS}}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM41C4002C inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short sa possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41C4002C input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and verticaooy and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the Vcc line can cause loss of data integrity (soft erros). It is recommended that the total combined voltage changes over time in the Vcc to Vss voltage (measured at the device pins) should not exceed 500mV.

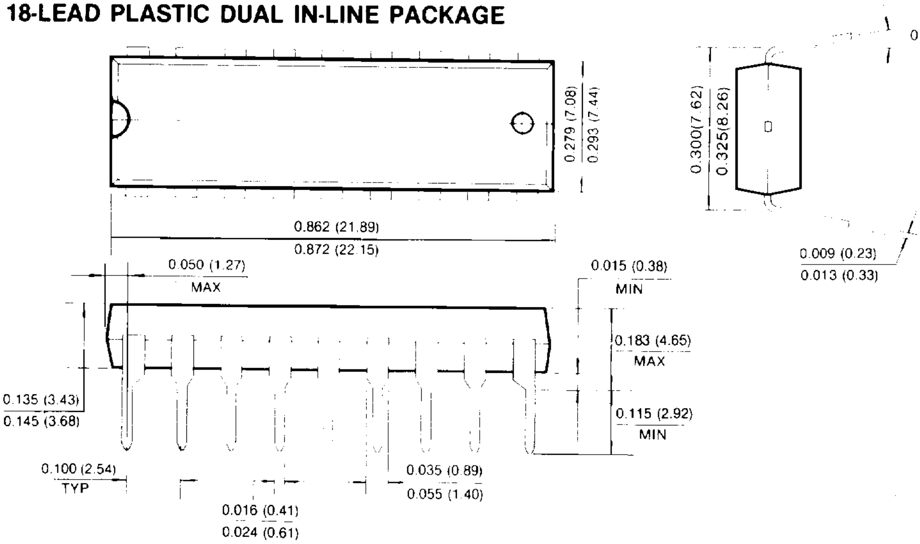
A high frequency 0.1μF ceramic decoupling capacitor should be connected between the Vcc and ground pins of each KM41C4002C using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41C4002C and they supply much of the current used by the KM41C4002C during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

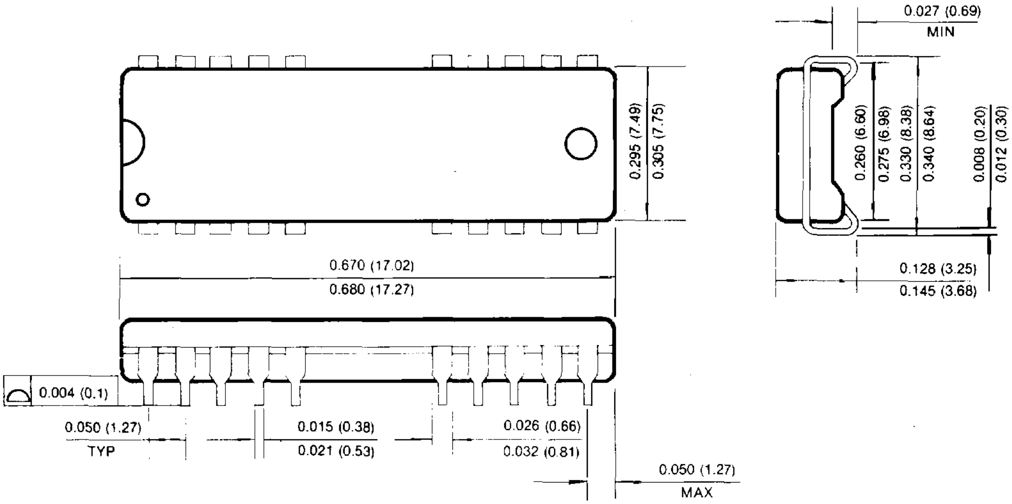
Units: Inches (Millimeters)



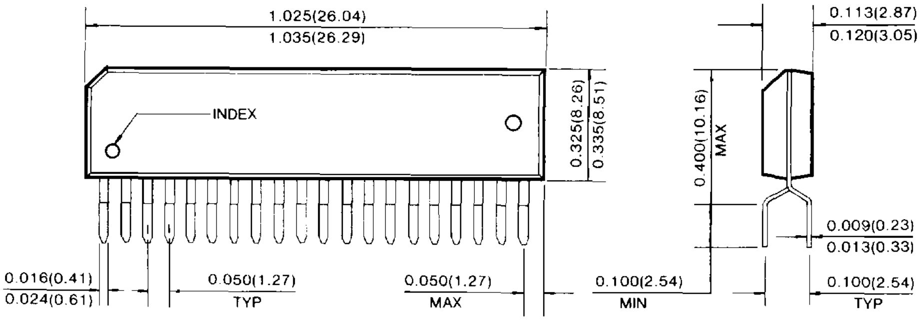
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)