Signetics

74190, 191, LS191
Counters

'190 Presettable BCD/Decade Up/Down Counter
'191 Presettable 4-Bit Binary Up/Down Counter
Product Specification

Logic Products

FEATURES

- **Synchronous, reversible counting**
- **BCD/decade—'190**
  4-bit binary—'191
- **Synchronous, reversible counting**
- **Asynchronous parallel load capability**
- **Count enable control for synchronous expansion**
- **Single Up/Down control input**

DESCRIPTION

The '190 is an asynchronously presettable up/down BCD decade counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation. The '191 is similar, but is a 4-bit binary counter.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74190	25MHz	65mA
74191	25MHz	65mA
74LS191	25MHz	20mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$
Plastic DIP	N74190N, N74191N, N74LS191N
Plastic SOL-16	N74LS191D

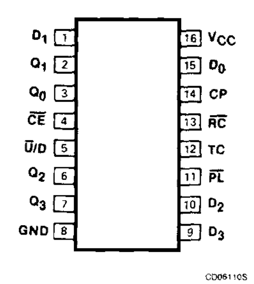
NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

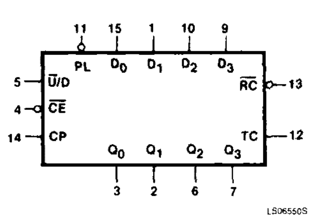
PINS	DESCRIPTION	74	74S
$\overline{CE}$	Input	3ul	3LSul
Other	Inputs	1ul	1LSul
All	Outputs	10ul	10LSul

NOTE:
Where a 74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

PIN CONFIGURATION

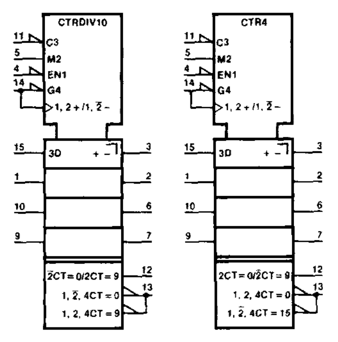


LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)



Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel Data inputs ($D_0 - D_3$) is loaded into the counter and appears on the outputs when the Parallel Load ($\overline{PL}$) input is LOW. As indicated in the Mode Select Table, this operation overrides the counting function.

Counting is inhibited by a HIGH level on the Count Enable ($\overline{CE}$) input. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the Clock input. The Up/Down ($\overline{U}$/D) input signal determines the direction of counting as indicated in the Mode Select Table. The $\overline{CE}$ input may go LOW when the clock is in either state, however, the LOW-to-HIGH $\overline{CE}$ transition must occur only when the clock is HIGH. Also, the $\overline{U}$/D input should be changed only when either $\overline{CE}$ or CP is HIGH.

Overflow/underflow indications are provided by two types of outputs, the Terminal Count (TC) and Ripple Clock ($\overline{RC}$). The TC output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches "9" in the count-up mode for 74190, and reaches "15" in the count-up mode for 74191/74LS191. The TC output will remain HIGH until a state change occurs, either by counting or presetting, or until $\overline{U}$/D is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes.

The TC signal is used internally to enable the $\overline{RC}$ output. When TC is HIGH and $\overline{CE}$ is LOW, the RC follows the Clock Pulse (CP) delayed by two gate delays. The $\overline{RC}$ output essentially duplicates the LOW clock pulse width, although delayed in time by two gate delays. This feature simplifies the design of multistage counters, as indicated in Figures A and B. In Figure A, each $\overline{RC}$ output is used as the Clock input for the next higher stage. When the clock source has a limited drive capability this configuration is particularly advantageous, since the clock source drives only the first stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a HIGH signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse as indicated in the Mode Select Table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This is a disadvantage of the configuration in some applications.

Figure B shows a method of causing state changes to occur simultaneously in all stages. The $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion and all Clock inputs are driven in parallel. The LOW state duration of the clock in this configuration must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. Since the $\overline{RC}$ output of any package goes HIGH shortly after its CP input goes HIGH, there is no such restriction on the HIGH state duration of the clock.

In Figure C, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the $\overline{CE}$ input signal for a given stage. An enable signal must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own $\overline{CE}$, therefore, the simple inhibit scheme of Figure A and B does not apply.

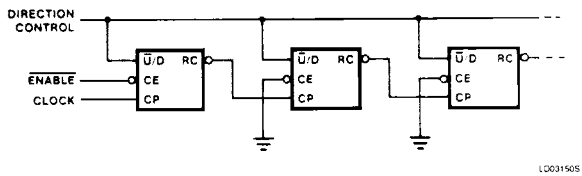


Figure 1. N-Stage Counter Using Ripple Clock

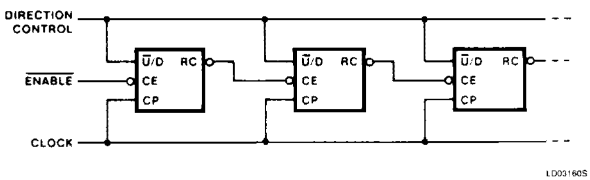


Figure 2. Synchronous N-Stage Counter Using Ripple Carry Borrow

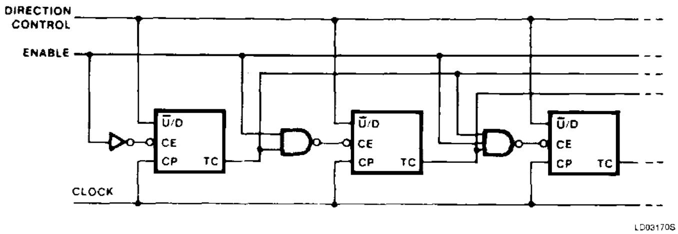
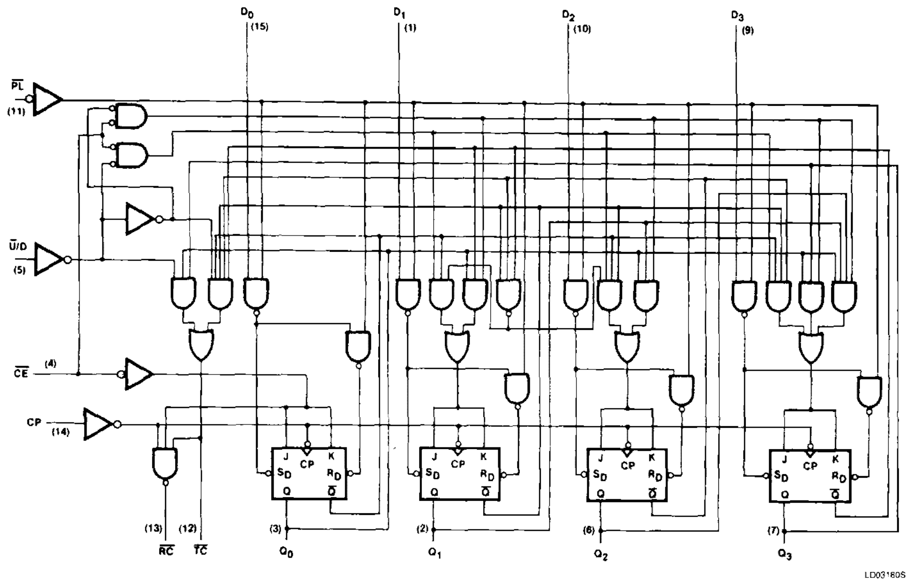


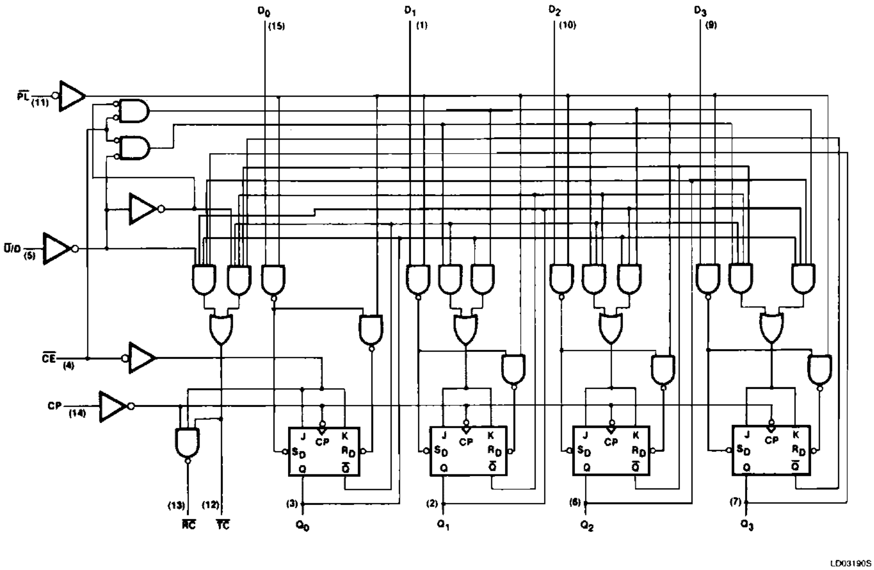
Figure 3. Synchronous N-Stage Counter With Parallel Gated Carry Borrow

LOGIC DIAGRAM '190



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

LOGIC DIAGRAM '191



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

MODE SELECT — FUNCTION TABLE, '190, '191

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{PL}$	$\overline{U}$/D	$\overline{CE}$	CP	D_n	Q_n
Parallel load	L L	X X	X X	X X	L H	L H
Count up	H	L	l	↑	X	count up
Count down	H	H	l	↑	X	count down
Hold "do nothing"	H	X	H	X	X	no change

TC AND $\overline{RC}$ FUNCTION TABLE, '190

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}$/D	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	⊔	H	X	X	H	⊓	⊔
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊔	L	L	L	L	⊓	⊔

TC AND $\overline{RC}$ FUNCTION TABLE, '191

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}/D$	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	⊔	H	H	H	H	_⌐	⊔
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊔	L	L	L	L	_⌐	⊔

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.
⊔ = LOW pulse.
_⌐ = TC goes LOW on a LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to $+V_{CC}$	-0.5 to $+V_{CC}$	V
T_A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			2.0			V
V_{IL}	LOW-level input voltage			+0.8			+0.8	V
I_{IK}	Input clamp current			-12			-18	mA
I_{OH}	HIGH-level output current			-800			-400	µA
I_{OL}	LOW-level output current			16			8	mA
T_A	Operating free-air temperature	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			74190, 191			74LS191			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MIN, I_{OH} = MAX			2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX			0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA (74LS)						0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5			−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V	$\overline{CE}$ input						0.3	mA
				Other inputs						0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V	$\overline{CE}$ input			120				μA
				Other inputs			40				μA
			V_I = 2.7V	$\overline{CE}$ input						60	μA
				Other inputs						20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V	$\overline{CE}$ input			−4.8			−1.2	mA
				Other inputs			−1.6			−0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−18		−65	−20		−100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				65	105		20	35	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all inputs grounded and all outputs open.

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AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

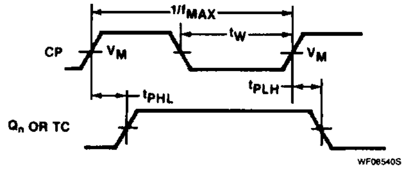
PARAMETER		TEST CONDITIONS	74		74LS		UNIT
			$C_L = 15pF$, $R_L = 400\Omega$		$C_L = 15pF$, $R_L = 2k\Omega$		
			Min	Max	Min	Max	
f_{MAX}	Maximum input count frequency	Waveform 1	20		20		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to Q output	Waveform 1		24 36		24 36	ns
t_{PLH} t_{PHL}	Propagation delay Clock to $\overline{RC}$ output	Waveform 2		20 24		20 24	ns
t_{PLH} t_{PHL}	Propagation delay Clock to TC output	Waveform 1		42 52		42 52	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$ output	Waveform 7		45 45		45 45	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to TC output	Waveform 7		33 33		33 33	ns
t_{PLH} t_{PHL}	Propagation delay Data to Q outputs	Waveform 3		22 50		32 40	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to any output	Waveform 4		33 50		33 50	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$ output	Waveform 2		33 33		33 33	ns

NOTE:
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SET-UP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

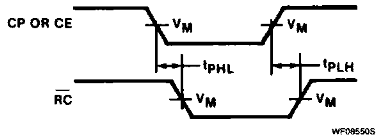
PARAMETER		TEST CONDITIONS	74		74LS		UNIT
			Min	Max	Min	Max	
t_W	CP pulse width	Waveform 1	25		25		ns
t_W	$\overline{PL}$ pulse width	Waveform 5	35		35		ns
t_s	Set-up time, data to $\overline{PL}$	Waveform 6	20		20		ns
t_h	Hold time, data to $\overline{PL}$	Waveform 6	4		5		ns
t_{rec}	Recovery time, $\overline{PL}$ to CP	Waveform 5	40		40		ns
$t_s(L)$	Set-up time, LOW $\overline{CE}$ to clock	Waveform 8	40		40		ns
$t_h(L)$	Hold time, LOW $\overline{CE}$ to clock	Waveform 8	0		0		ns

AC WAVEFORMS



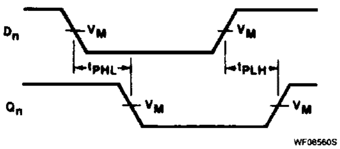
V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.

Waveform 1



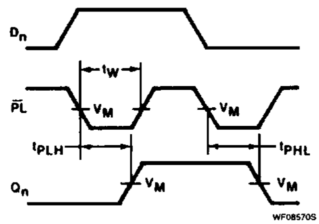
V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.

Waveform 2



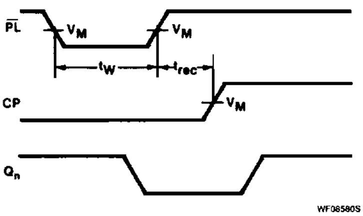
V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.

Waveform 3



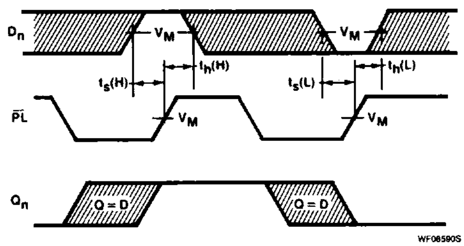
V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.

Waveform 4



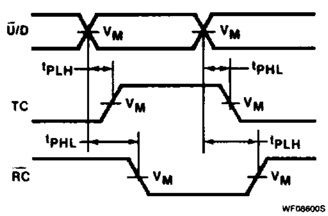
V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.

Waveform 5



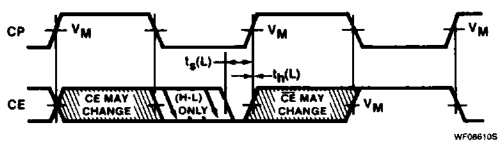
V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 6



V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.

Waveform 7

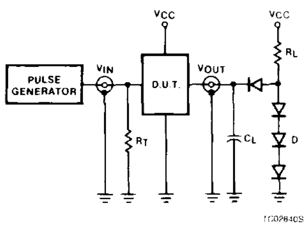


V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

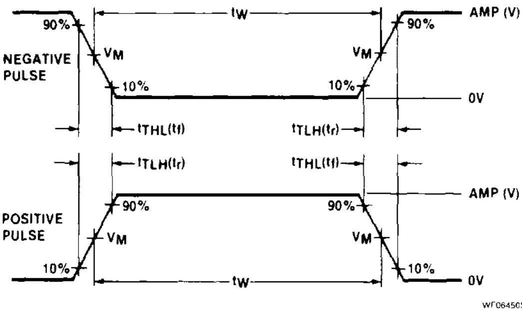
Waveform 8

Counters — 74190, 191, LS191

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Totem-Pole Outputs



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns