SECTION 5: ELECTRICAL CHARACTERISTICS

5.1 Timing Diagrams

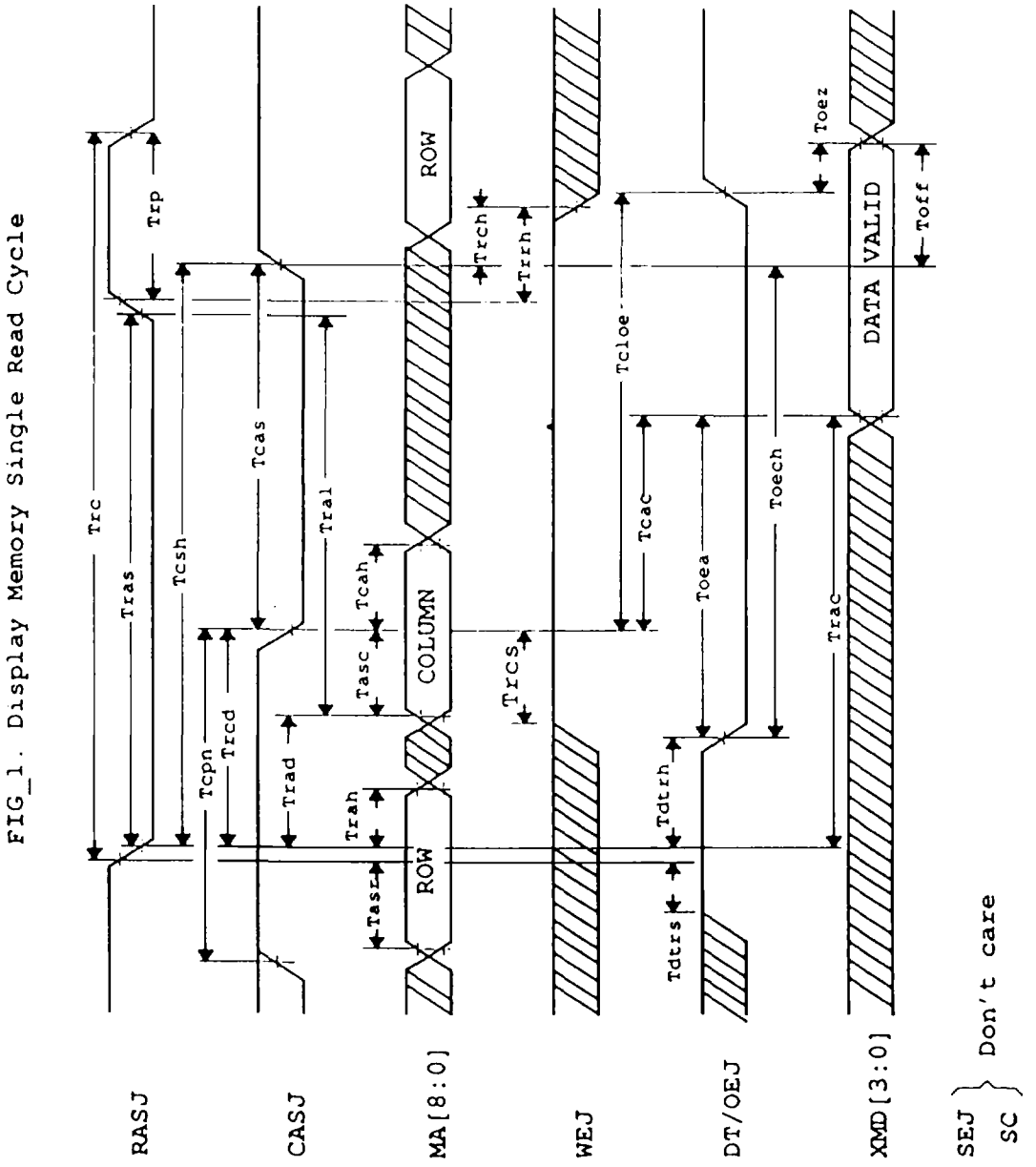

FIG_1. Display Memory Single Read Cycle

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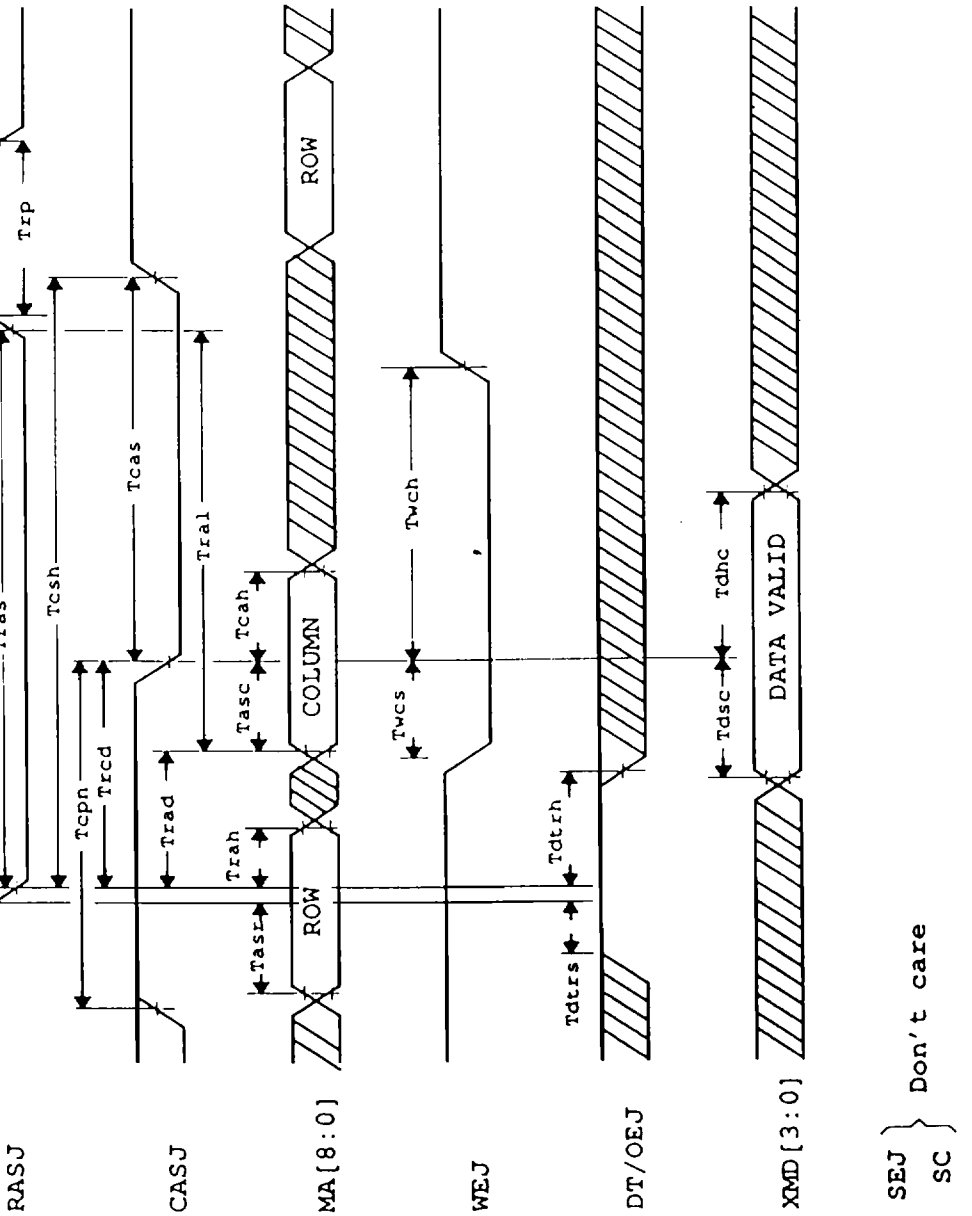
FIG_2. Display Memory Single Write Cycle (Early Write)



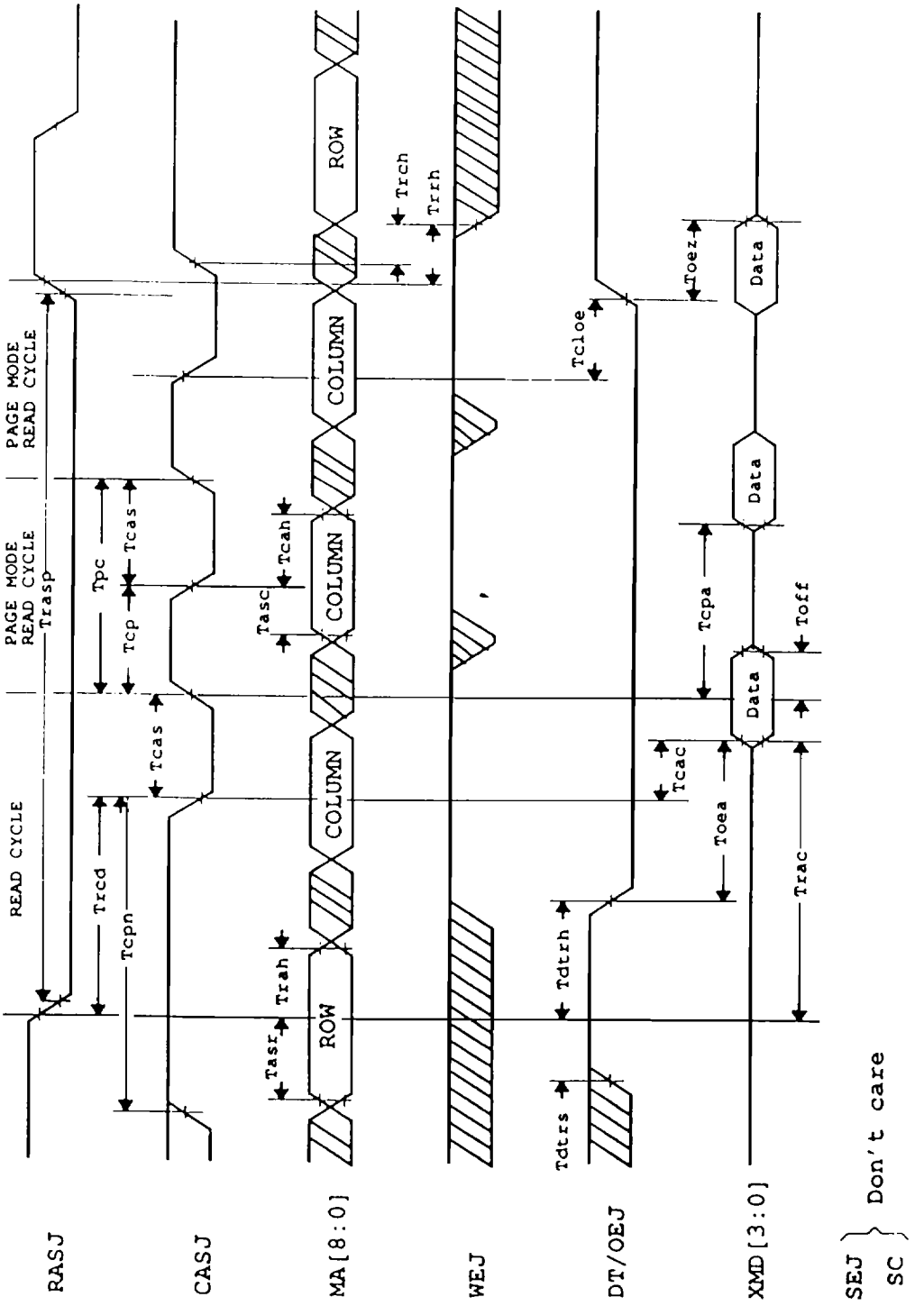


FIG_3. Display Memory Page Mode Read Cycle

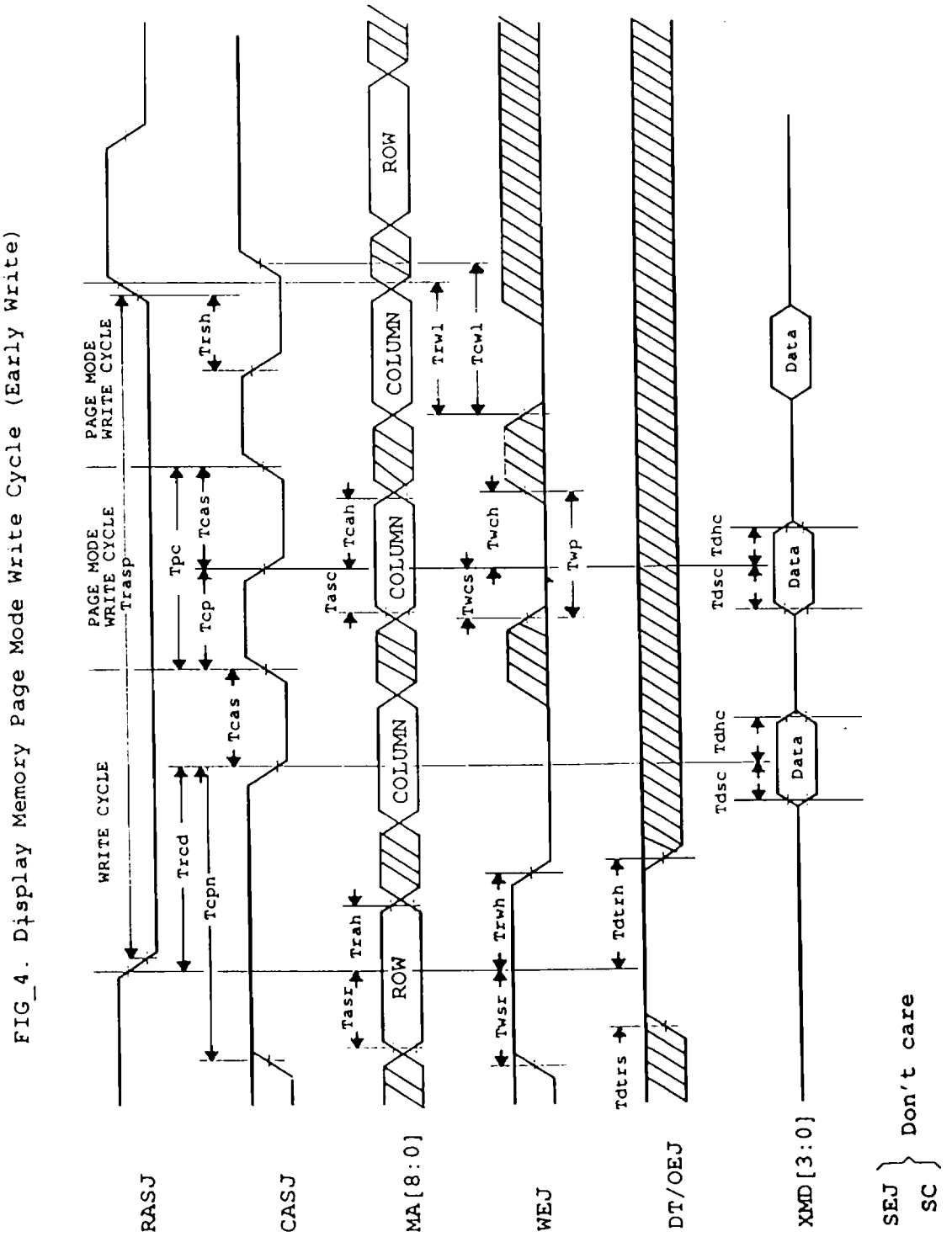


FIG_4. Display Memory Page Mode Write Cycle (Early Write)

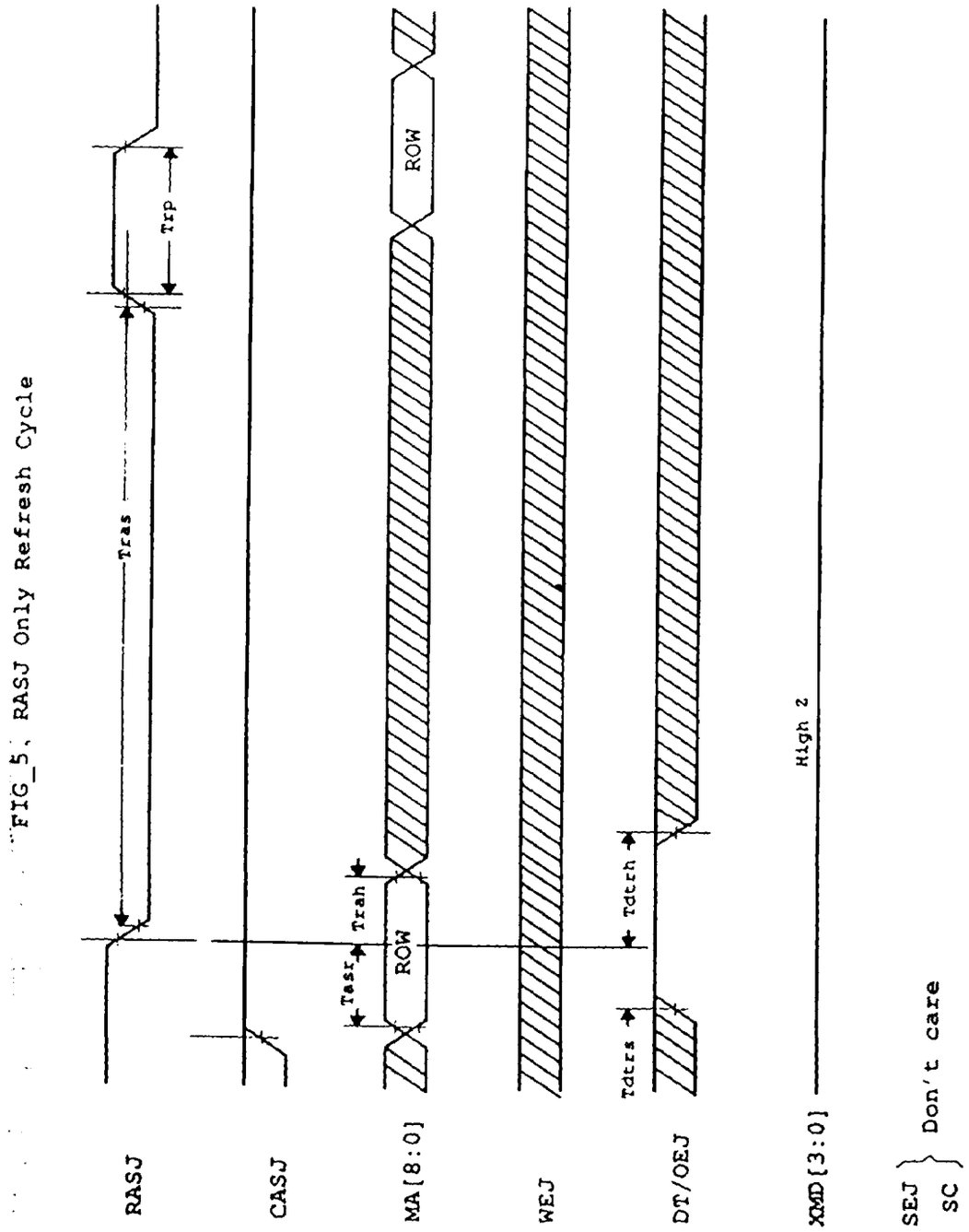
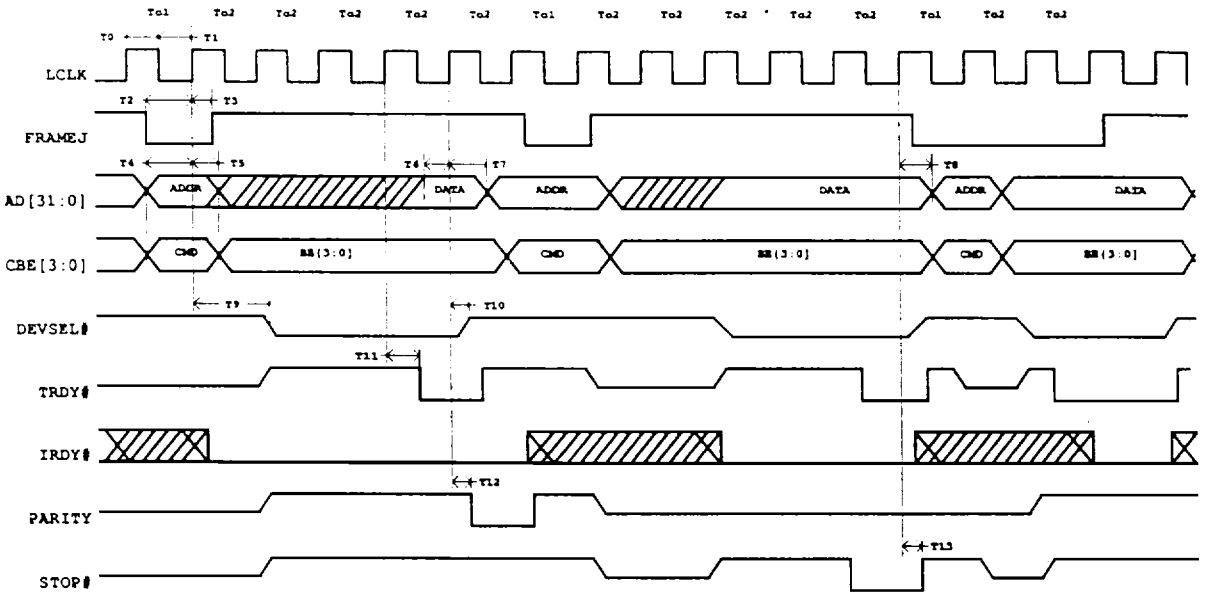


FIG_5, RASJ Only Refresh Cycle

VIDEO RAM Specifications :

SYMBOL	Parameter	-60 m M	-70 m M	-80 m M
Tcac	Access time from CASJ	15	20	20
Trac	Access time from RASJ	60	70	80
Tcaa	Column address access time	30	35	40
Toea	Access time from OEJ	15	20	20
Toff	Output disable Time after CASJ high	0 15	0 20	0 20
Toez	Output disable time after OEJ high	0 15	0 20	0 20
Tsca	Access time from SCJ high		25	25
Tsoh	Serial output hold time after SCJ high		5	5
Trc	Read/Write cycle time	110	130	150
Tras	RASJ low pulse width	60	70	80
Tcas	CASJ low pulse width	15	20	20
Tcsh	CASJ hold time after RASJ	60	70	80
Trsh	RASJ hold time after CASJ low	15	25	25
Trp	RASJ high pulse width	40	50	60
Trcd	Delay time RASJ low to CASJ low	20 45	20 50	25 60
Tcpn	CASJ high pulse width	10	10	10
Tasr	Row addr setup time before RASJ	0	0	0
Trah	Row address hold time after RASJ	10	10	15
Tasc	Column address setup time before CASJ	0	0	0
Tcah	Column address hold time after CASJ	10	15	20
Trad	Column address delay time from RASJ	15 30	15 35	20 40
Twsr	WEJ setup time before RASJ	0	0	0
Trwh	WEJ hold time after RASJ	10	10	15
Tdtrs	OEJ setup time before RASJ	0	0	0
Tdtrh	OEJ hold time after RASJ	10	10	15
Trcs	Read setup time before CASJ low	0	0	0
Trch	Read hold time after CASJ high	0	0	0
Trrh	Read hold time after RASJ high	0	0	0
Tral	Column address to RASJ setup time	30	35	40
Tcloe	OEJ hold time after CASJ low	20	20	25
Toech	CASJ hold time after OEJ low	15	20	20
Twcs	Write setup time before CASJ	0	0	0
Twch	Write hold time after CASJ	10	15	15
Tcwl	CASJ hold time after write	15	20	20
Trwl	RASJ hold time after write	15	20	20
Twp	Write pulse width	10	15	15
Tdsc	Data setup time before CASJ	0	0	0
Tdhc	Data hold time after CASJ	10	15	15
Tdsw	Data setup time before write	0	0	0
Tdhw	Data hold time after write	10	15	15
Toehd	Delay time OEJ high to data	10	15	15
Twoe	OEJ hold time after write	10	15	15
Trasp	RASJ low pulse width	95	115	135

Read Transfer Cycle				
Symbol	Parameter	-60 m M	-70 m M	-80 m M
Trdh	OEJ hold time after RASJ		55	65
Tcdh	OEJ hold time after CASJ		30	30
Tadh	OEJ hold time after address		30	30
Tsdh	SC hold time after OEJ		15	15
Tcsd	Delay time CASJ to SC		30	30
Tscc	SC clock cycle time		30	30
Tsch	SC high pulse width		10	10
Tscl	SC low pulse width		10	10



M3147V PCI v1.0 interface timing specifications

SYMBOL	MEANING	Min	Max	Unit
T0	LCLK High time	4/10	6/10	LCLK
T1	LCLK Low time	4/10	6/10	LCLK
T2	FRAMEJ setup time	8		ns
T3	FRAMEJ hold time	2		
T4	AD[31:0],CBE[3:0]setup time	10		
T5	AD[31:0],CBE[3:0] hold time	0		
T6	read DATA[31:0] setup time	5		
T7	read DATA[31:0] hold time	10		
T8	write DATA{31:0] hold time	0		
T9	DEVSELJ, PARITY, STOPJ after first FRAMEJ	1		LCLK
T10	DEVSELJ float time from LCLK after command finish	3		ns
T11	TRDYJ active delay		16	
T12	PARITY active delay		10	
T13	STOPJ hold time	3		

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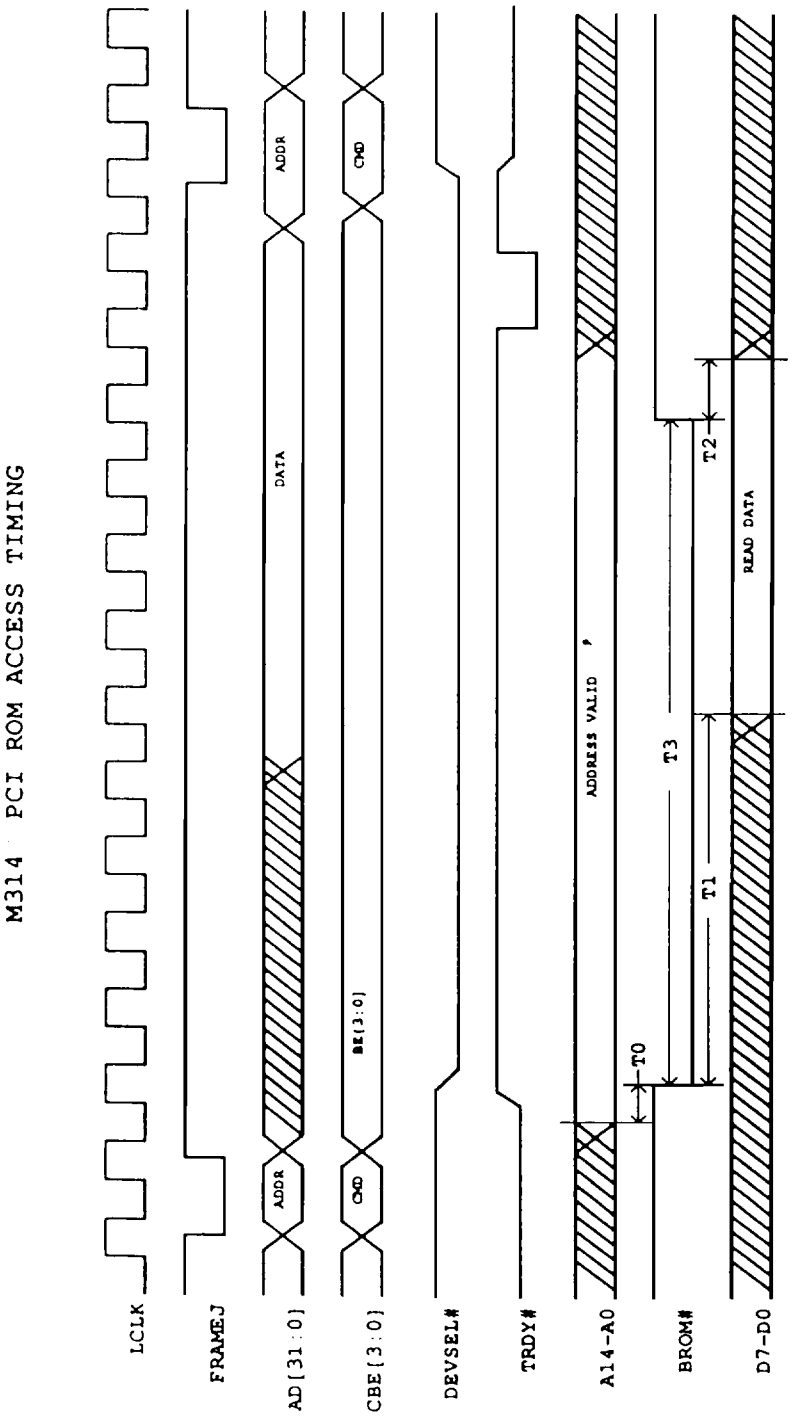
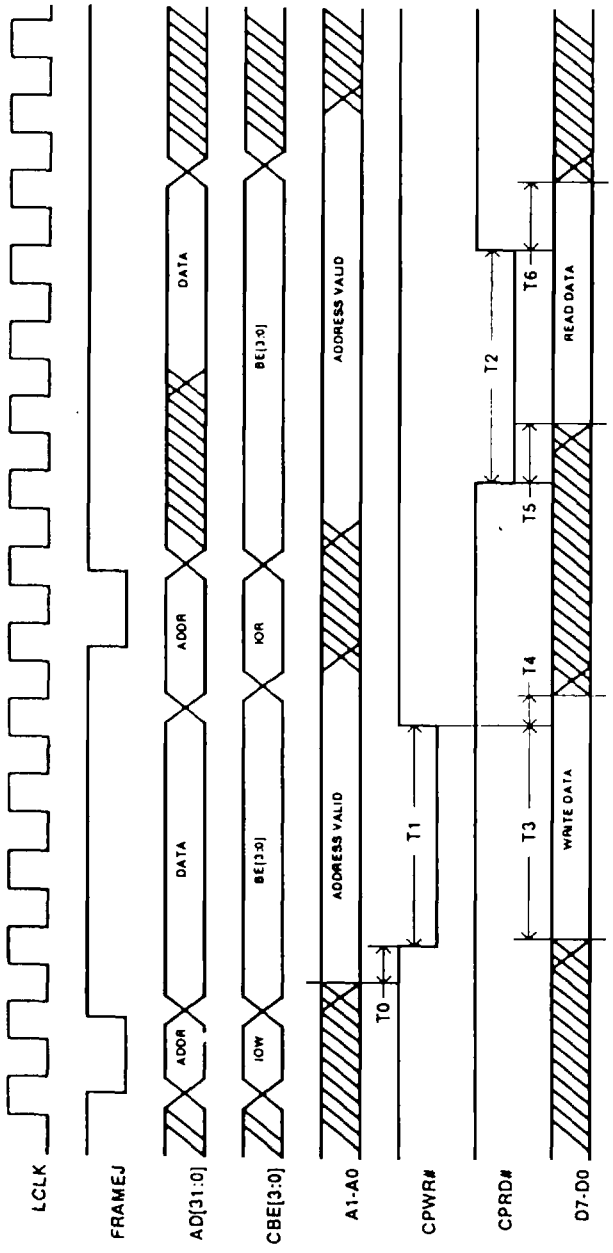
M314 PCI ROM ACCESS TIMING



M3147 PCI RAMDAC ACCESS AC TIMING



M3147V PCI ROM access AC timing specifications

SYMBOL	MEANING	Min	Max	Unit
T0	ADDRESS setup time from BROMJ	15		ns
T1	DATA appear time after BROMJ		50	
T2	DATA hold time from BROMJ	0		
T3	BROMJ low pulse width	140		

M3147V PCI RAMDAC access AC timing specifications

SYMBOL	MEANING	Min	Max	Unit
T0	ADDRESS setup time		15	ns
T1	DAC write command pulse width	55		
T2	DAC read command pulse width	55		
T3	write DATA[31:0] setup time	40		
T4	write DATA{31:0] hold time	5		
T5	CPRDJ asserted to DATA valid		40	
T6	DATA 3-stated from CPRDJ negated	15		

CLKCELL Interface AC Timing