



Integrated Device Technology, Inc.

LOW POWER 3V CMOS SRAM 1 MEG (64K x 16-BIT)

ADVANCE INFORMATION IDT71V016L

FEATURES:

- 64K x 16 Organization
- Wide Operating Voltage Range: 2.7V to 3.6V
- Speed Grades: 70ns, 100ns
- Low Operating Power: 45mA (max)
- Low Standby Power: 5µA (max)
- Low-Voltage Data Retention: 1.5V (min)
- Available in a 44-pin TSOP package

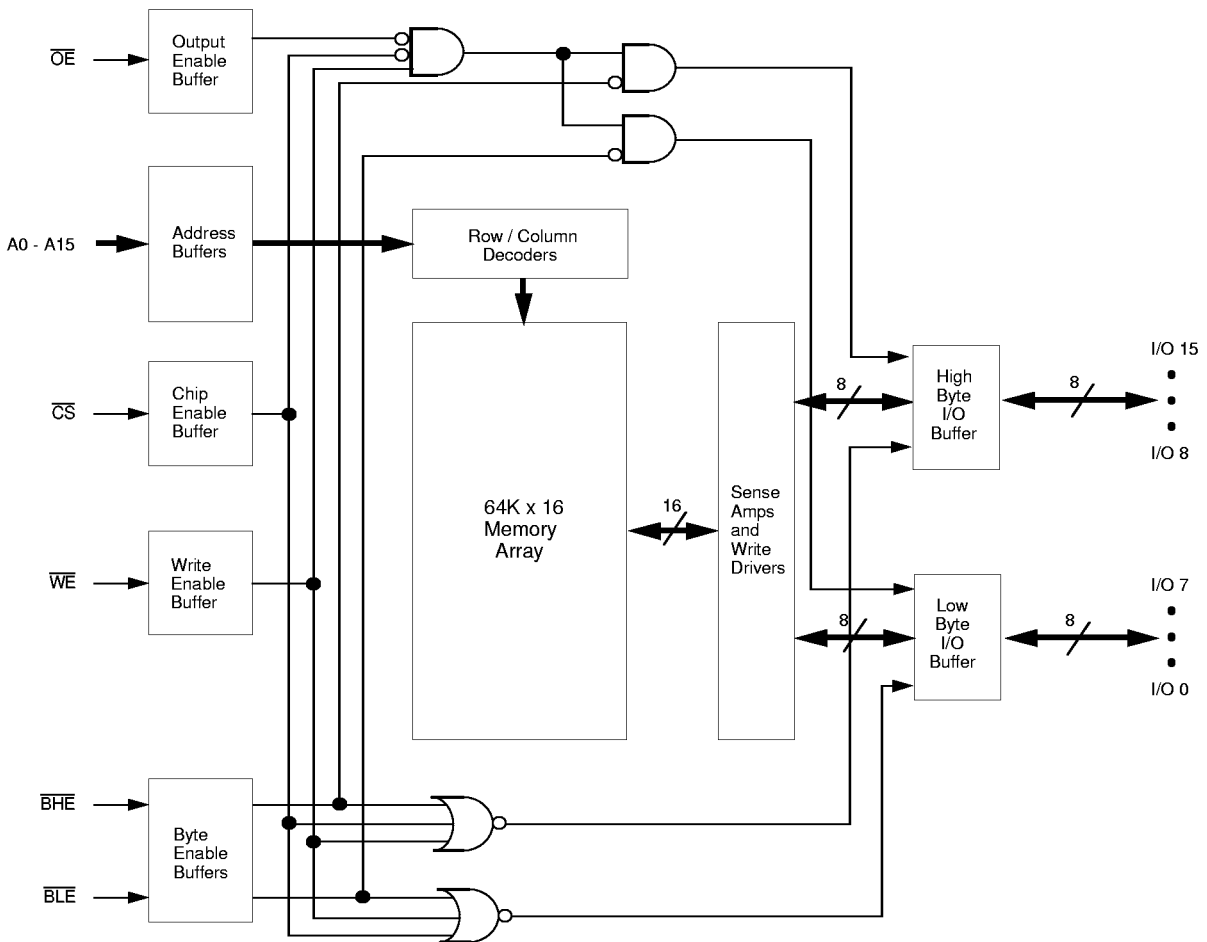
DESCRIPTION:

The IDT71V016L is a 1,048,576-bit very low-power Static RAM organized as 64K x 16. It is fabricated using IDT's high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for low-power memory needs. It uses a 6-transistor memory cell.

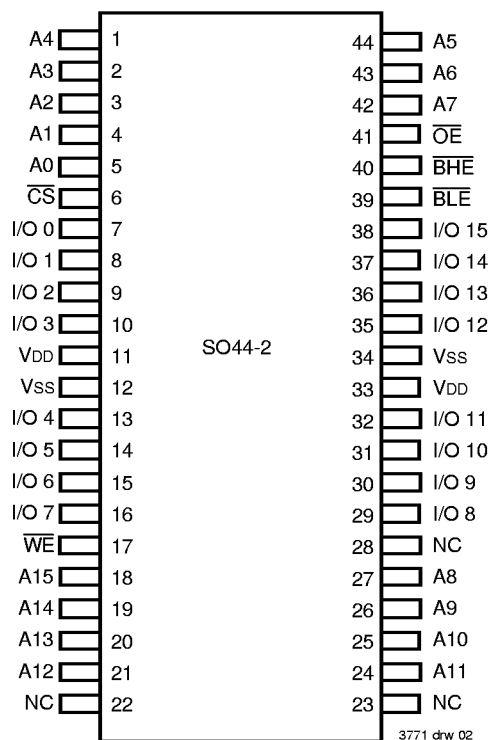
All input and output signals of the IDT71V016L are TTL-compatible and operation is from a single extended-range 3.3V supply. This extended supply range makes the device ideally suited for unregulated battery-powered applications. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71V016L is packaged in a JEDEC standard 44-pin TSOP Type II.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



TSOP
 TOP VIEW

PIN DESCRIPTIONS

A0 – A15	Address Inputs	Input
\overline{CS}	Chip Select	Input
\overline{WE}	Write Enable	Input
\overline{OE}	Output Enable	Input
\overline{BHE}	High Byte Enable	Input
\overline{BLE}	Low Byte Enable	Input
I/O ₀ - I/O ₁₅	Data Input/Output	I/O
VDD	Power	Pwr
VSS	Ground	Gnd

3771 tbl 01

TRUTH TABLE⁽¹⁾

\overline{CS}	\overline{OE}	\overline{WE}	\overline{BLE}	\overline{BHE}	I/O ₀ -I/O ₇	I/O ₈ -I/O ₁₅	Function
H	X	X	X	X	High-Z	High-Z	Deselected - Standby
L	L	H	L	H	DATAOUT	High-Z	Low Byte Read
L	L	H	H	L	High-Z	DATAOUT	High Byte Read
L	L	H	L	L	DATAOUT	DATAOUT	Word Read
L	X	L	L	L	DATAIN	DATAIN	Word Write
L	X	L	L	H	DATAIN	High-Z	Low Byte Write
L	X	L	H	L	High-Z	DATAIN	High Byte Write
L	H	H	X	X	High-Z	High-Z	Outputs Disabled
L	X	X	H	H	High-Z	High-Z	Outputs Disabled

NOTE:

1. H = V_{IH}, L = V_{IL}, X = Don't care.

3771 tbl 02

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Com'l. and Ind'l.	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to V _{SS}	-0.5 to +4.6	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to V _{SS}	-0.5 to V _{DD} +0.5V	V
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-55 to +125	°C
P _T	Power Dissipation	1.0	W
I _{OUT}	DC Output Current	20	mA

NOTES:

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{DD} terminals only.
- Input, Output, and I/O terminals; 4.6V maximum.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	V _{SS}	V _{DD}
Commercial	0°C to +70°C	0V	2.7V to 3.6V
Industrial	-40°C to +85°C	0V	2.7V to 3.6V

3771 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage	2.7	3.0	3.6	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.0	—	V _{DD} +0.3	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.8	V

NOTE:

3771 tbl 05

- V_{IL} (min.) = -1.5V for pulse width less than t_{RC}/2, once per cycle.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	6	pF
C _{I/O}	I/O Capacitance	V _{OUT} = 3dV	7	pF

NOTE:

3771 tbl 06

- This parameter is guaranteed by device characterization, but not production tested.

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 2.7V to 3.6V, Commercial and Industrial Temperature Ranges

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I _{LI}	Input Leakage Current	V _{DD} = Max., V _{IN} = V _{SS} to V _{DD}	—	1	μA
I _{LO}	Output Leakage Current	V _{DD} = Max., \overline{CS} = V _{IH} , V _{OUT} = V _{SS} to V _{DD}	—	1	μA
V _{OH}	Output High Voltage	I _{OH} = -1mA, V _{DD} = Min.	2.4	—	V
V _{OL}	Output Low Voltage	I _{OL} = 2mA, V _{DD} = Min.	—	0.4	V

3771 tbl 07

DC ELECTRICAL CHARACTERISTICS^(1, 2)

V_{DD} = 2.7 to 3.6V, V_{LC} = 0.2V, V_{HC} = V_{DD}-0.2V, Commercial and Industrial Temperature Ranges

Symbol	Parameter	Test Conditions	71V016L70	71V016L100	Unit
I _{CC2}	Dynamic Operating Current	\overline{CS} = V _{LC} , Outputs Open, V _{DD} = 3.6V, f = f _{MAX} ⁽³⁾	45	35	mA
I _{CC}	Static Operating Current	\overline{CS} = V _{LC} , Outputs Open, \overline{WE} = V _{HC} , V _{DD} = 3.6V, f = 0 ⁽⁴⁾	10	10	mA
I _{SB1}	Standby Supply Current	\overline{CS} = V _{HC} , Outputs Open, V _{DD} = 3.6V	5	5	μA

NOTES:

3771 tbl 08

- All values are maximum guaranteed values.
- Input low and high voltage levels are 0.2V and V_{DD}-0.2V respectively for all tests.
- f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}).
- f = 0 means no address input lines are changing.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

($V_{LC} = 0.2V$, $V_{HC} = V_{DD} - 0.2V$)

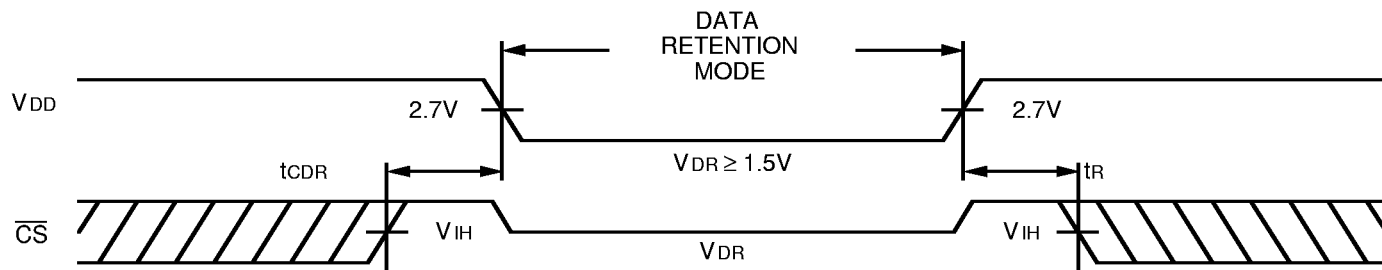
Symbol	Parameter	Test Condition	Min.	Typ. ⁽¹⁾	Max.	Unit
V _{DR}	V _{CC} for Data Retention	—	1.5	—	—	V
I _{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$	—	<1	5	μA
t _{CDR} ⁽³⁾	Chip Deselect to Data Retention Time		0	—	—	ns
t _R ⁽³⁾	Operation Recovery Time		t _{RC} ⁽²⁾	—	—	ns

NOTES:

1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization, but is not production tested.

3771 tbl 09

LOW V_{DD} DATA RETENTION WAVEFORM



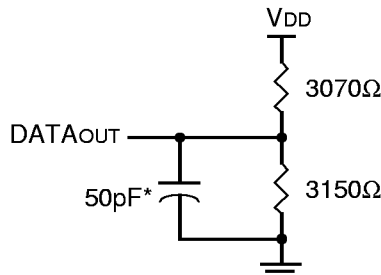
3771 drw 05

AC TEST CONDITIONS

Input Pulse Levels	GND to 2.5V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figure 1

3771 tbl 09

AC TEST LOAD



3771 drw 04

*Including jig and scope capacitance.

Figure 1. AC Test Load

AC ELECTRICAL CHARACTERISTICS (V_{DD} = 2.7 to 3.6V, All Temperature Ranges)

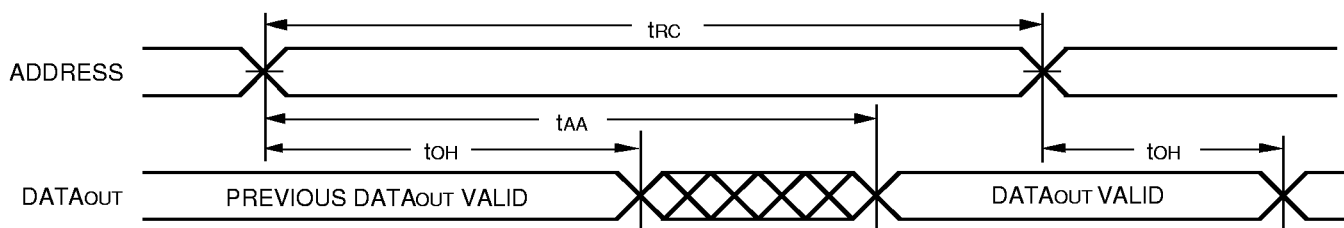
Symbol	Parameter	71V016L70		71V016L100		Units
		Min.	Max.	Min.	Max.	
Read Cycle						
t _{RC}	Read Cycle Time	70	—	100	—	ns
t _{AA}	Address Access Time	—	70	—	100	ns
t _{ACS}	Chip Select Access Time	—	70	—	100	ns
t _{CLZ} ⁽¹⁾	Chip Select Low to Output in Low-Z	10	—	10	—	ns
t _{CHZ} ⁽¹⁾	Chip Select High to Output in High-Z	—	25	—	30	ns
t _{OE}	Output Enable Low to Output Valid	—	35	—	50	ns
t _{OLZ} ⁽¹⁾	Output Enable Low to Output in Low-Z	5	—	5	—	ns
t _{OHZ} ⁽¹⁾	Output Enable High to Output in High-Z	—	25	—	30	ns
t _{OH}	Output Hold from Address Change	10	—	15	—	ns
t _{BE}	Byte Enable Low to Output Valid	—	35	—	50	ns
t _{BLZ} ⁽¹⁾	Byte Enable Low to Output in Low-Z	5	—	5	—	ns
t _{BHZ} ⁽¹⁾	Byte Enable High to Output in High-Z	—	25	—	30	ns
Write Cycle						
t _{WC}	Write Cycle Time	70	—	100	—	ns
t _{AW}	Address Valid to End of Write	65	—	80	—	ns
t _{CW}	Chip Select Low to End of Write	65	—	80	—	ns
t _{BW}	Byte Enable Low to End of Write	65	—	80	—	ns
t _{AS}	Address Set-up Time	0	—	0	—	ns
t _{WR}	Address Hold from End of Write	0	—	0	—	ns
t _{WP}	Write Pulse Width	55	—	70	—	ns
t _{DW}	Data Valid to End of Write	30	—	40	—	ns
t _{DH}	Data Hold Time	0	—	0	—	ns
t _{OW} ⁽¹⁾	Write Enable High to Output in Low-Z	5	—	5	—	ns
t _{WHZ} ⁽¹⁾	Write Enable Low to Output in High-Z	—	25	—	30	ns

NOTE:

1. This parameter is guaranteed by device characterization, but is not production tested.

3771 tbl 10

TIMING WAVEFORM OF READ CYCLE NO. 1^(1,2,3)

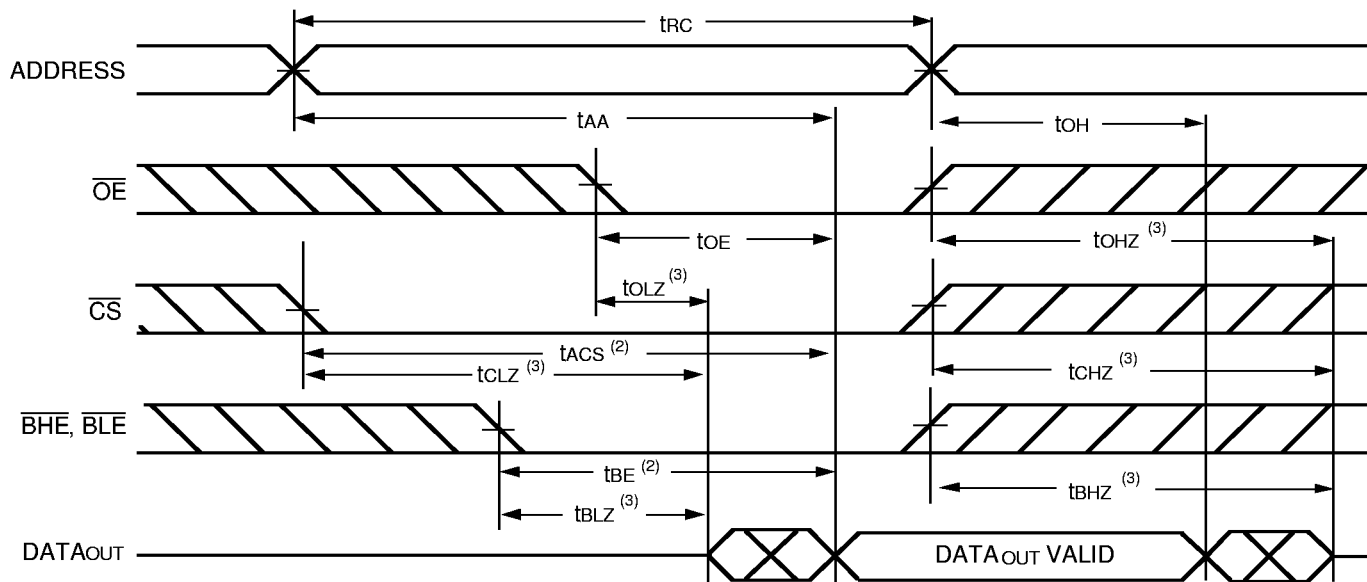


3771 drw 06

NOTES:

1. \overline{WE} is HIGH for Read Cycle.
2. Device is continuously selected, \overline{CS} is LOW.
3. \overline{OE} , \overline{BHE} , and \overline{BLE} are LOW.

TIMING WAVEFORM OF READ CYCLE NO. 2⁽¹⁾

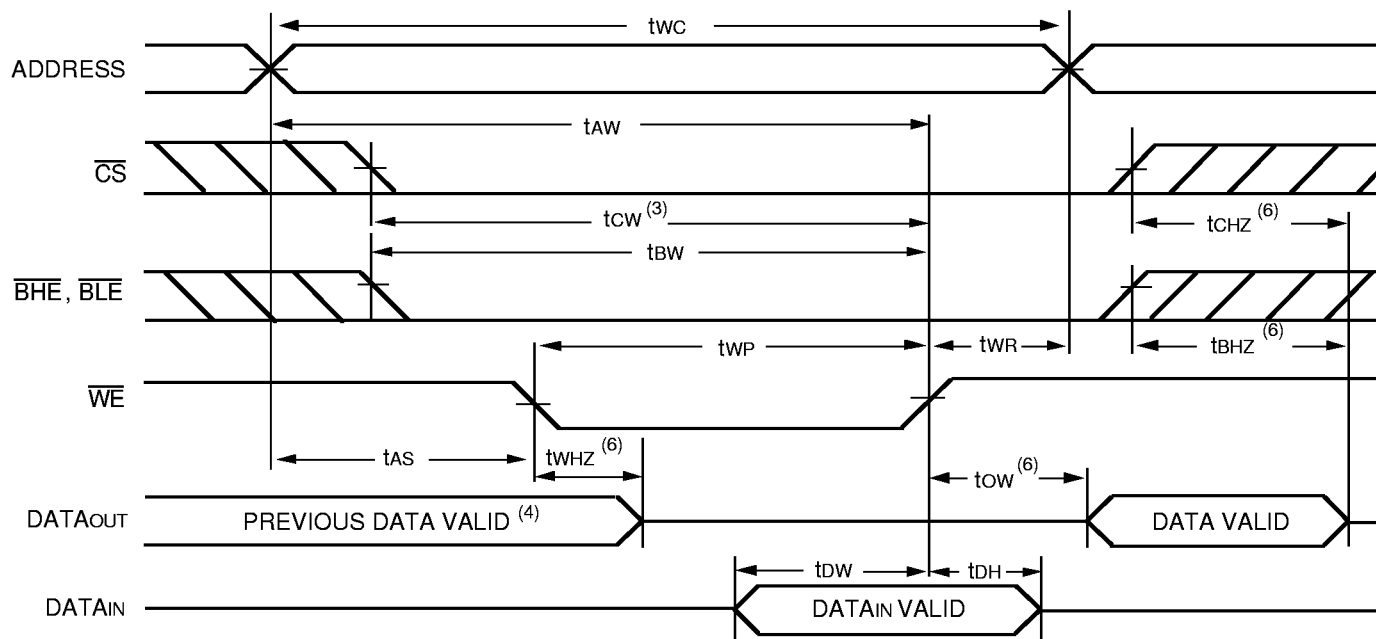


NOTES:

1. \overline{WE} is HIGH for Read Cycle.
2. Address must be valid prior to or coincident with the later of \overline{CS} , \overline{BHE} , or \overline{BLE} transition LOW; otherwise t_{AA} is the limiting parameter.
3. Transition is measured $\pm 200\text{mV}$ from steady state.

3771 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (\overline{WE} CONTROLLED TIMING)^(1,2,3,5)

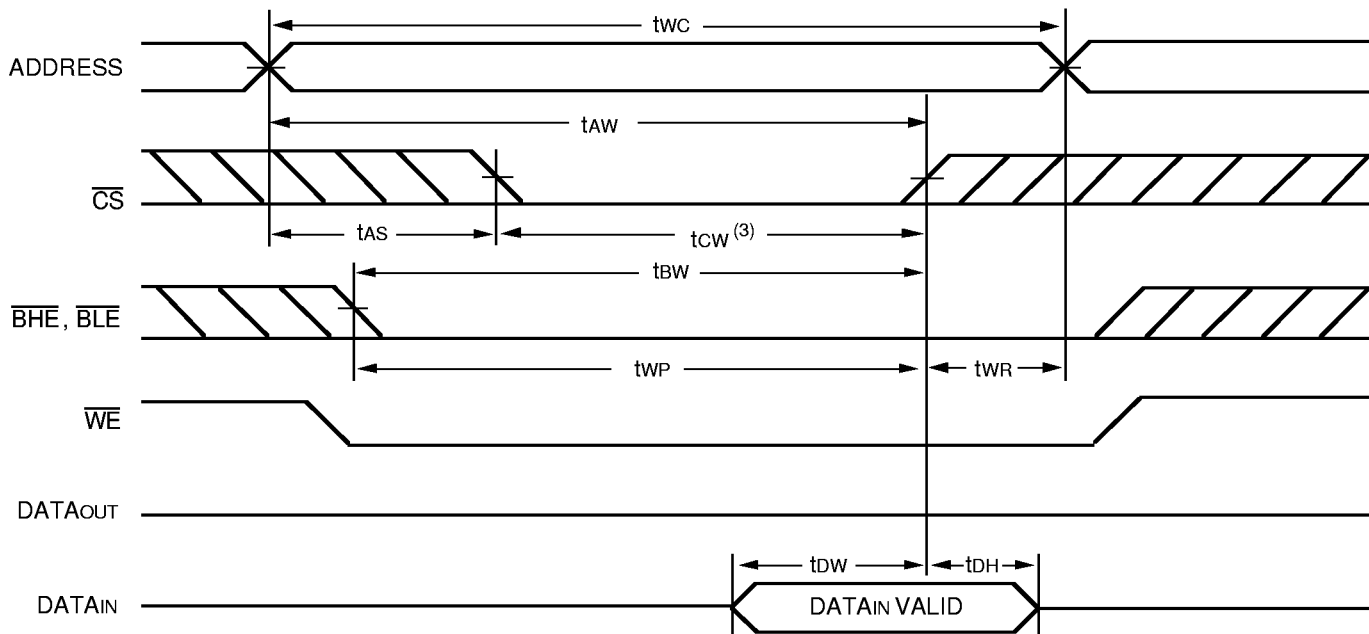


NOTES:

1. \overline{WE} or (\overline{BHE} and \overline{BLE}) or \overline{CS} must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW \overline{CS} , LOW \overline{BHE} or \overline{BLE} , and a LOW \overline{WE} .
3. \overline{OE} is continuously HIGH. If during a \overline{WE} controlled write cycle \overline{OE} is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW} . If \overline{OE} is HIGH during a \overline{WE} controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP} .
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the \overline{CS} LOW or \overline{BHE} and \overline{BLE} LOW transition occurs simultaneously with or after the \overline{WE} LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured $\pm 200\text{mV}$ from steady state.

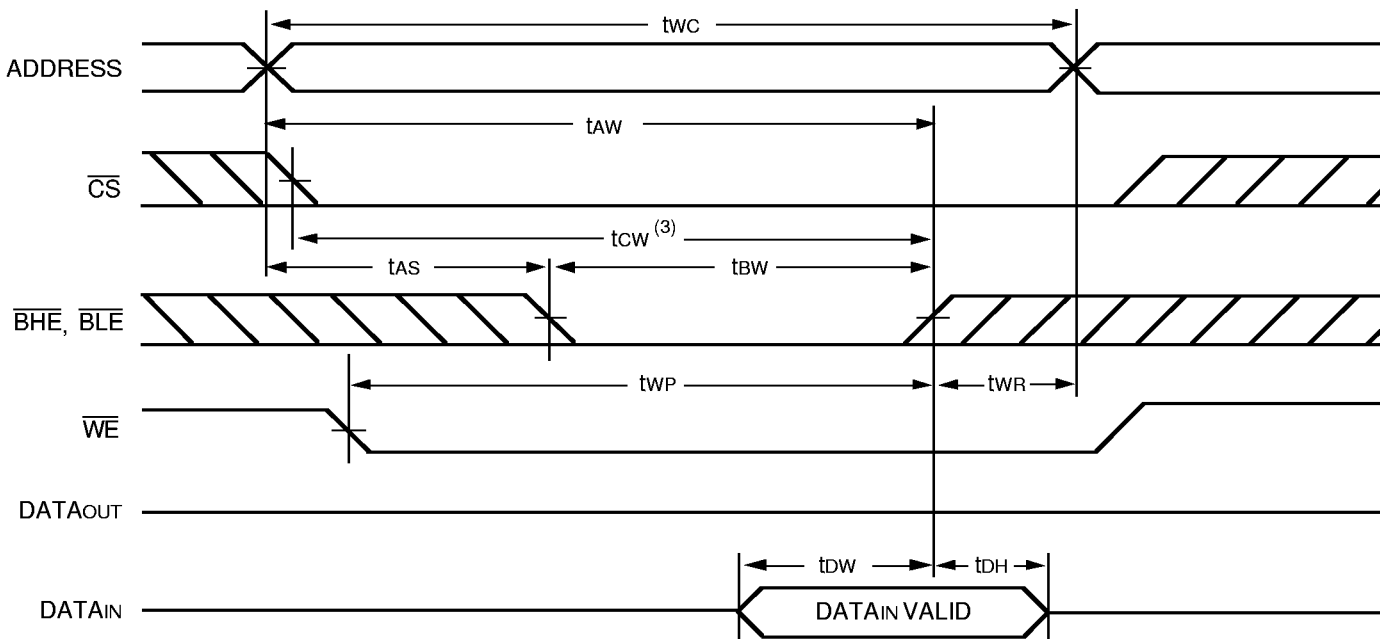
3771 drw 08

TIMING WAVEFORM OF WRITE CYCLE NO. 2 (\overline{CS} CONTROLLED TIMING)^(1,2,5)



3771 drw 09

TIMING WAVEFORM OF WRITE CYCLE NO. 3 (\overline{BHE} , \overline{BLE} CONTROLLED TIMING)^(1,2,5)

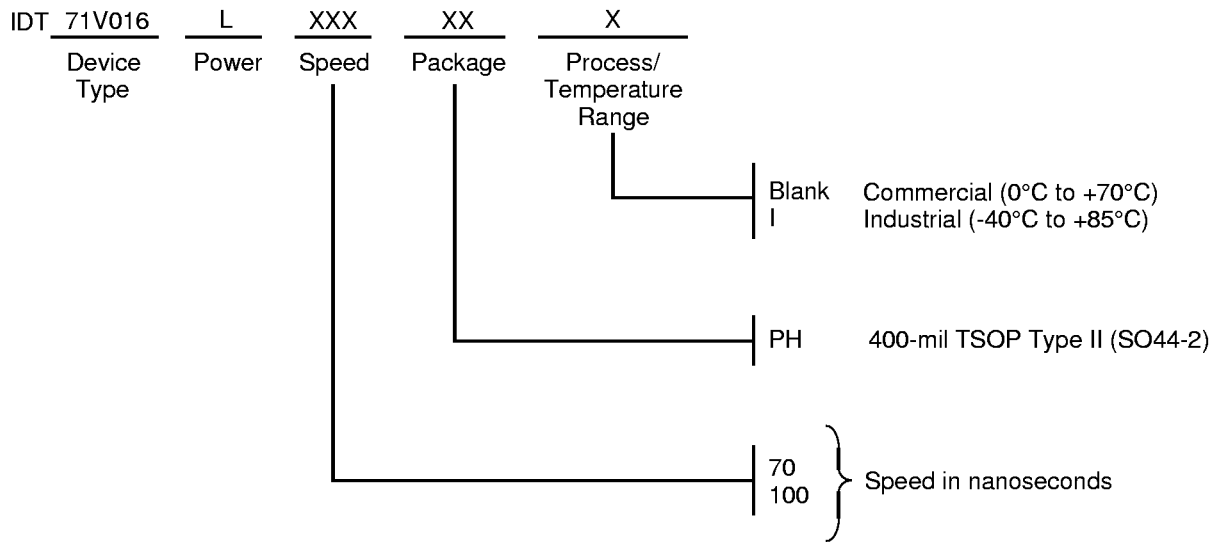


3771 drw 10

NOTES:

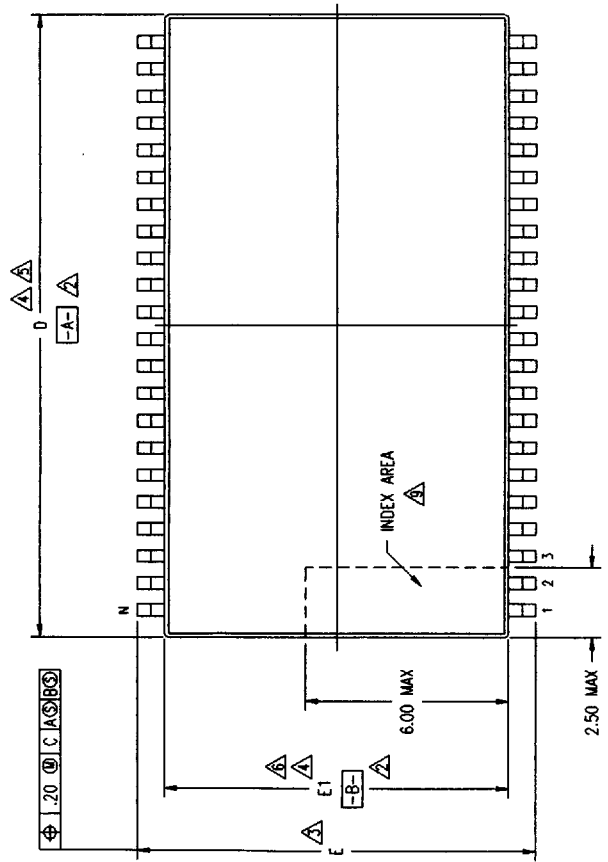
1. \overline{WE} or (\overline{BHE} and \overline{BLE}) or \overline{CS} must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW \overline{CS} , LOW \overline{BHE} or \overline{BLE} , and a LOW \overline{WE} .
3. \overline{OE} is continuously HIGH. If during a \overline{WE} controlled write cycle \overline{OE} is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW} . If \overline{OE} is HIGH during a \overline{WE} controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP} .
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the \overline{CS} LOW or \overline{BHE} and \overline{BLE} LOW transition occurs simultaneously with or after the \overline{WE} LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured $\pm 200\text{mV}$ from steady state.

ORDERING INFORMATION

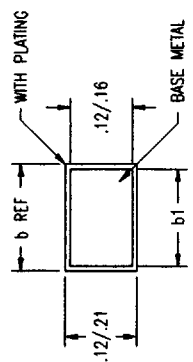
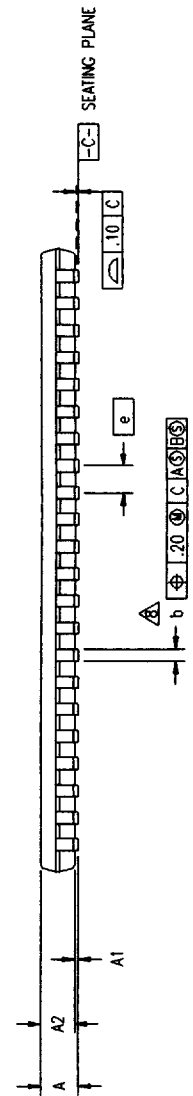
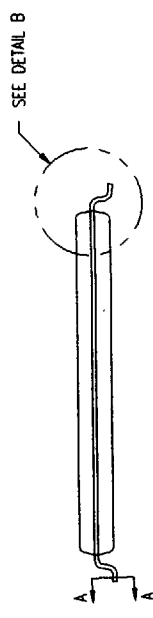
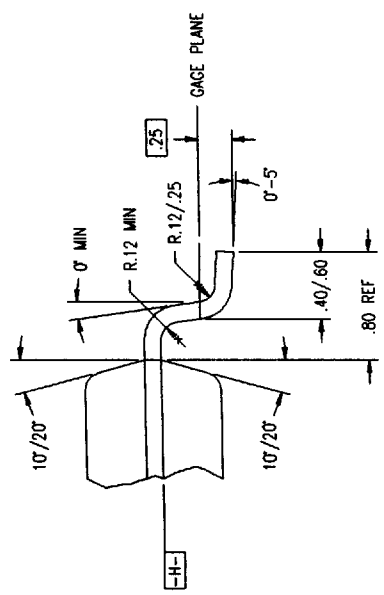


3771 drw 11

REVISIONS		DATE	APPROVED
DCN	REV	DESCRIPTION	
28074	00	INITIAL RELEASE	T. VU
29046	01	ADD 32 LD	



DETAIL B



SECTION A-A

		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-8116 FAX: (408) 492-8674 TWR: 910-336-2070	
TOLERANCES UNLESS SPECIFIED	DECIMAL	ANGULAR	
XXXX	±		
XXXXX			
APPROVALS	DATE	TITLE	
DRAWN	08/20/95	PH PACKAGE OUTLINE	
CHECKED		10.16 mm BODY WIDTH	
		TSOP TYPE II	
		SIZE	DRAWING NO.
		C	PSC-4050
		REV	01
		DO NOT SCALE DRAWING	
		SHEET 1 OF 2	