

TOSHIBA BI-DIRECTIONAL TRIODE THYRISTOR SILICON PLANAR TYPE

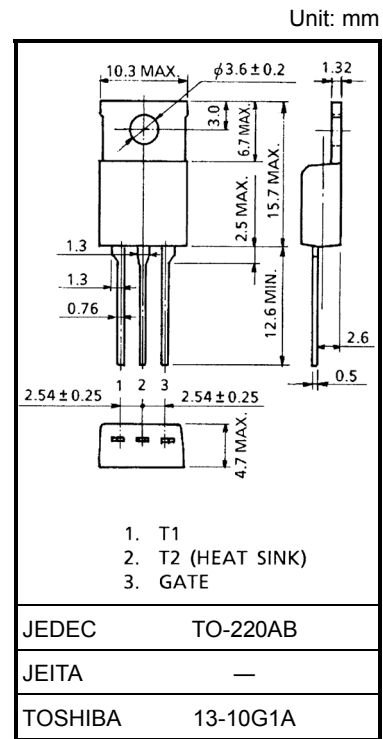
S6903G, S6903J

AC POWER CONTROL APPLICATIONS

- High Rush Current Capability
Optimal for controlling actuators where high rush current may flow
: $I_{TRM} = 120A$ ($n = 100k$ cycle, $T_c = 45^\circ C$)
- R.M.S On-State Current : I_T (RMS) = 20A
- Repetitive Peak Off-State Voltage : $V_{DRM} = 400V, 600V$

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Repetitive Peak Off-State Voltage	S6903G	400	V
	S6903J	600	
R.M.S On-State Current (Full Sine Waveform $T_c = 100^\circ C$)	I_T (RMS)	20	A
Peak One Cycle Surge On-State Current (Non-Repetitive)	I_{TSM}	180 (50Hz)	A
		200 (60Hz)	
Repetitive Surge On-State Current (Note 1)	I_{TRM}	120	A
I^2t Limit Value	I^2t	167	A^2s
Critical Rate of Rise of On-State Current	di / dt	50	A / μs
Peak Gate Power Dissipation	P_{GM}	5	W
Average Gate Power Dissipation	P_G (AV)	0.5	W
Peak Gate Voltage	V_{GM}	10	V
Peak Gate Current	I_{GM}	2	A
Junction Temperature	T_j	-40~125	$^\circ C$
Storage Temperature Range	T_{stg}	-40~125	$^\circ C$

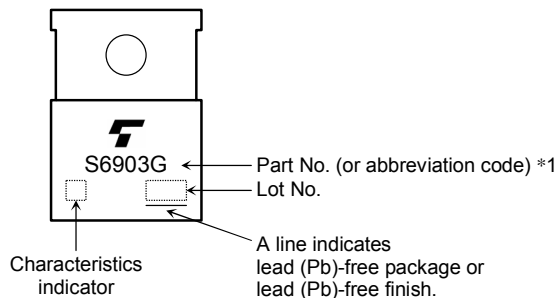


Weight: 2.0 g (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

MARKING

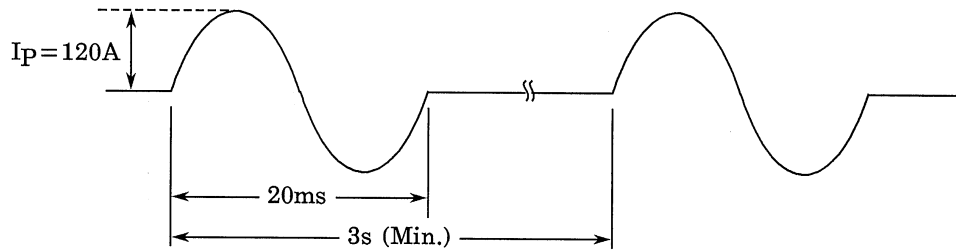


*1	Part No. (or abbreviation code)	Part No.
	S6903G	S6903G
	S6903J	S6903J

ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT		
Repetitive Peak Off-State Current	I_{DRM}	$V_{DRM} = \text{Rated}$	—	—	20	μA		
Gate Trigger Voltage	I	$V_D = 12\text{V}$ $R_L = 20\Omega$		T2 (+), Gate (+)	—	—	1.5	V
	II			T2 (+), Gate (-)	—	—	1.5	
	III			T2 (-), Gate (-)	—	—	1.5	
	IV			T2 (-), Gate (+)	—	—	—	
Gate Trigger Current	I	$V_D = 12\text{V}$ $R_L = 20\Omega$		T2 (+), Gate (+)	—	—	30	mA
	II			T2 (+), Gate (-)	—	—	30	
	III			T2 (-), Gate (-)	—	—	30	
	IV			T2 (-), Gate (+)	—	—	—	
Peak On-State Voltage	V_{TM}	$I_{TM} = 30\text{A}$	—	—	1.6	V		
Gate Non-Trigger Voltage	V_{GD}	$V_D = \text{Rated}, T_c = 125^\circ\text{C}$	0.2	—	—	V		
Holding Current	I_H	$V_D = 12\text{V}, I_{TM} = 2\text{A}$	—	—	50	mA		
Thermal Resistance	$R_{th(j-c)}$	Junction to Case, AC	—	—	1.0	$^\circ\text{C} / \text{W}$		
Critical Rate of Rise of Off-State Voltage at Commutation	$(dv / dt)_c$	$V_{DRM} = 400\text{V}, T_j = 125^\circ\text{C}$ $(di / dt)_c = -8.7\text{A} / \text{ms}$	10	—	—	$\text{V} / \mu\text{s}$		

Note 1: Repetitive Surge On-State Current



$I_P = 120\text{A}$ ($f = 50\text{Hz}$) at $T_c = 45^\circ\text{C}$

Max. Repetitive Number of cycle $n = 100\text{k}$ cycle (Repetitive cycle $T = 3\text{s Min.}$)

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