MN5920/21

8-Bit, 150MHz
Flash A/D Converters

FEATURES

- **8-Bit Resolution**
- **150MHz Sampling Rate**
- **335MHz Input Bandwidth**
- **Low 10pF Input Capacitance**
- **Comparator Input and Clock Buffers**
- **Single -5.2V Supply Operation**
- **ECL-Compatible Digital Inputs/Outputs**
- **0°C to +70°C Operation**
- **42-Pin Ceramic DIP Package**

DESCRIPTION

The MN5920/21 are monolithic 8-bit, 150MHz flash A/D converters. These converters are ECL-compatible and are clocked from a single sampling clock.

They feature a unique comparator design with input and clock buffers. The analog input buffers stabilize the comparators input capacitance over changing input frequencies making these devices easier to drive than typical flash A/D converters.

The devices are packaged in a 42-pin ceramic DIP packages and operate from a single -5.2V supply.

Devices are available for commercial and industrial applications and are specified for 0°C to +70°C applications.

APPLICATIONS

Video Digitizer
RADAR
Pulse Measurement Systems
Communications
Infrared Imaging
IF Digitizer
Imaging
Medical Imaging

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MN5920/21 8-Bit 150MHz Flash A/D Converters

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	0°C to +70°C
Specified Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Power Supplies	-7.0 to +0.5Volts
Digital Inputs	$-V_{EE}$ to +0.5Volts
Analog Input	$-V_{EE}$ to +0.5Volts
Reference Current V_{RTF} to V_{RBF}	25mA
Digital Output Current	0 to -30mA

ORDERING INFORMATION

PART NUMBER **MN5920/21**

Standard model is specified for 0°C to +70°C operation.

SPECIFICATIONS Typical at +25°C, $-V_{EE}$=-5.2V, V_{IN}= 0 to -2V, f_S= 150MSPS, f_{CLK}= 150MHz, V_{RTF}= 0.0V, V_{RBF}= -2.0V, unless otherwise specified.

SPECIFICATIONS	MIN.	TYP.	MAX.	UNITS
ANALOG INPUT				
Input Voltage Range	-2		0	Volts
Input Capacitance		10		pF
Input Resistance		15		kΩ
Input Bandwidth (Vin=500mVp-p)		335		MHz
DIGITAL INPUTS				
Logic Levels: Logic "1"	-1.1		-0.7	Volts
Logic "0"	-2		-1.5	Volts
Logic Currents: Logic "1"		40		uA
Logic "0"		40		uA
DIGITAL OUTPUTS				
Logic Levels: Logic "1" (50Ω to -2V)	-1.1			Volts
Logic "0" (50Ω to -2V)			-1.5	Volts
TRANSFER CHARACTERISTICS				
Integral Nonlinearity Error (@ f_{CLK}=100kHz)	-0.75		+0.75	LSB
Differential Nonlinearity Error (@ f_{CLK}=100kHz)	-0.75		-0.75	LSB
Offset Error			+/-30	mV
Gain Error			+/-30	mV
No Missing Codes	Guaranteed			
DYNAMIC CHARACTERISTICS				
Conversion Rate	125	150		MHz
Clock to Data Delay		2.4		nsec
Acquisition Time		1.5		nsec
Aperture Jitter		5		psec-
Signal-to-Noise Ratio (SNR) (MN5920/5921)				
f_{IN} = 3.58MHz	46/45	48/47		dB
f_{IN} = 50MHz	42/40	46/44		dB
Total Harmonic Distortion (THD) (MN5920/5921)				
f_{IN} = 3.58MHz	-48/-46	-52/-50		dB
f_{IN} = 50MHz	-40/-39	-44/-43		dB
Signal-to-(Noise + Distortion) (SINAD) (MN5920/5921)				
f_{IN} = 3.58MHz	45/43	48/46		dB
f_{IN} = 50MHz	39/37	42/40		dB
REFERENCE INPUT				
Resistance	100	200	300	Ω
Bandwidth		10		MHz

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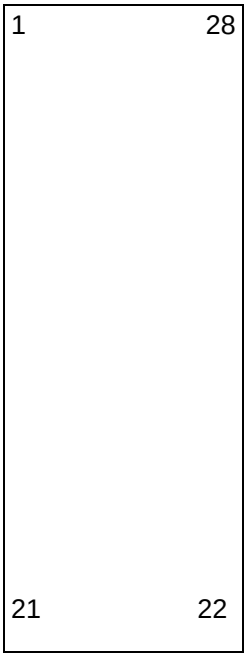
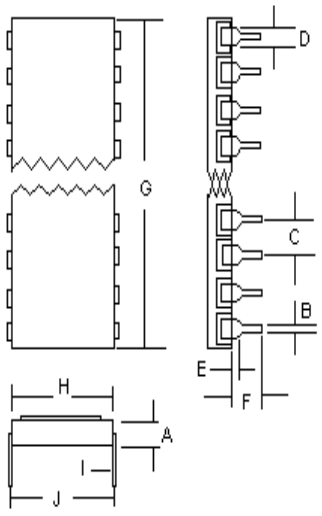
SPECIFICATIONS	MIN.	TYP.	MAX.	UNITS
POWER SUPPLY REQUIREMENTS				
Power Supply		-5.2		Volts
Supply Current		425	550	mA
Power Consumption		2.2	2.9	Watts

PIN DESIGNATIONS



1. Power Supply ($-V_{EE}$)
2. N.C.
3. LINV
4. Power Supply ($-V_{EE}$)
5. AGND
6. DGND
7. D0 (LSB)
8. D1
9. D2
10. D3
11. D4
12. D5
13. D6
14. D7 (MSB)
15. DGND
16. AGND
17. Power Supply ($-V_{EE}$)
18. MINV
19. N.C.
20. CLK
21. CLK
22. N.C.
23. V_{RFB}
24. N.C.
25. Power Supply ($-V_{EE}$)
26. Power Supply ($-V_{EE}$)
27. N.C.
28. N.C.
29. AGND
30. Analog Input
31. AGND
32. $V_{RF/2}$
33. AGND
34. Analog Input
35. AGND
36. N.C.
37. N.C.
38. Power Supply ($-V_{EE}$)
39. Power Supply ($-V_{EE}$)
40. N.C.
41. V_{RTF}
42. N.C.

PACKAGE OUTLINE



	INCHES		MILLIMETERS	
DIM	**MINIMUM**	**MAXIMUM**	**MINIMUM**	**MAXIMUM**
A	0.081	0.099	2.06	2.51
B	0.016	0.020	0.41	0.51
C	0.095	0.105	2.41	2.67
D		0.050 (typ)		1.27
E		0.050 (typ)		1.27
F		0.275		6.99
G	2.080	2.120	52.83	53.85
H	0.585	0.605	14.86	15.37
I	0.008	0.015	0.20	0.38
J	0.600	0.620	15.24	15.75

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APPLICATIONS INFORMATION - The MN5920 and MN5921 are fast monolithic 8-bit parallel flash A/D converters. The nominal conversion rate for these two devices is 150MSPS with an analog input bandwidth in excess of 200MHz.
The devices are designed with input preamplifiers inserted between the reference ladder and input comparators facilitating a reduction in the level of clock transient kickback into the input and reference ladder circuitry. These preamplifiers act as buffers and stabilize the input capacitance so that it remains constant for varying input frequencies and, therefore, making the devices easier to drive than other flash A/D converters. In addition the MN5920 and MN5921 incorporate proprietary decoding scheme that reduces metastable errors (sometimes referred to as sparkle codes or flyers) to a maximum of 1 LSB.

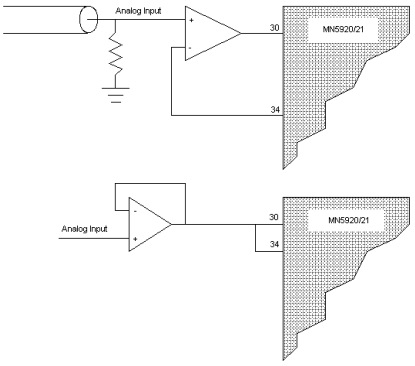
These devices are designed with true differential analog and digital paths from the preamplifiers to the output buffers (Current Mode Logic) for reducing potential missing codes while rejecting common mode noise.

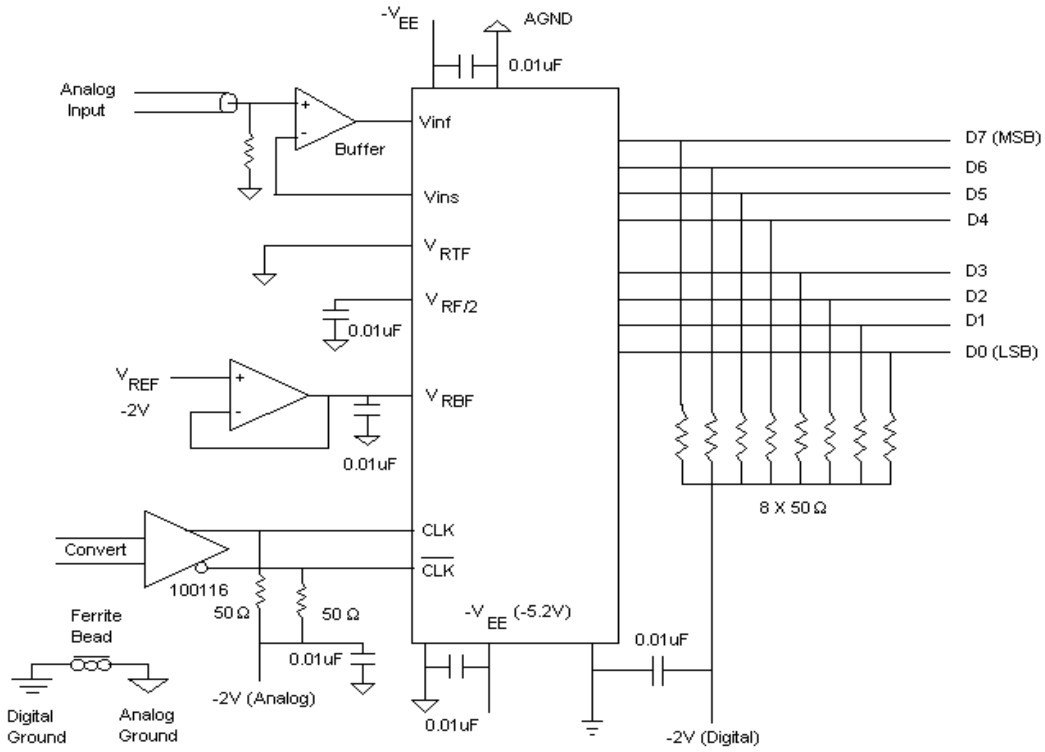
Signature errors are also reduced by careful layout of the analog circuitry. Every comparator also has a clock buffer to reduce differential delays and to improve signal-to-noise ratio. The output drive capability of the device can provide full ECL swings into 50Ω loads.

TYPICAL INTERFACE CIRCUIT - The typical interface circuit is shown below. The MN5920/21 is relatively easy to apply depending on the accuracy needed in the intended application. Wire-wrap may be employed with careful point-to-point ground connections if desired, but to achieve best operation, a double-sided PC board with a ground plane on the component side separated into digital and analog sections will give the best performance. The converter is bonded-out to place the digital pins on the left side of the package with the analog pins located on the right side of the package. Additionally, an RF bead connection through a single point from the analog to digital ground planes will reduce ground noise pickup.

POWER SUPPLIES AND GROUNDING - The $-V_{EE}$ connections are the device's power supply with respect to analog ground and is nominally -5.2V. The power supply pins should be bypassed as close to the device as possible with at least a 0.01uF ceramic capacitor. A 1uF tantalum capacitor should also be employed for low frequency noise suppression. The device's digital ground connection is the reference for the ECL outputs and is to be referenced to the output pulldown voltage appropriately bypassed as shown in the applications diagram.

ANALOG INPUT - There are two analog input pins tied internally to the same point. Either one may be used as an analog input sense and the other one for input force connections. This is convenient for testing the source signal when ensuring sufficient drive capability. The pins can also be tied together and driven single-ended. The





MN5920 and MN5921 offer superior performance compared to similar devices due to their internal comparator design.
Each comparator circuit is preceded with a preamplifier stage making the devices easier to drive because of a constant capacitance presented to the driving source. This constant capacitance results in less slew rate distortion.

CLOCK INPUTS - The clock inputs are designed to be driven differentially with ECL levels. The clock may be driven single-ended since CLK is internally biased to-1.3V. CLK may be left open, however, it is recommended that a 0.01uF capacitor be connected from CLK to analog ground. Please note that overall performance may be degraded due to increased clock noise and or jitter in this configuration.

OUTPUT LOGIC CONTROL (MINV, LINV) - The are ECL-compatible digital control lines designed to accommodate changing the output coding of these devices (straight binary , two's complement, etc.). See the following table for additional information. Both MINV and LINV are in the logic "low" state when left open. The high state can be obtained by tying these inputs to analog ground through a diode or 3.9KΩ resistor.

DIGITAL OUTPUTS - The device's digital outputs can drive ECL levels into 50Ω when pulled down to -2V. When pulled down to -5.2V, the output can drive 150Ω to 1KΩ loads.

REFERENCE INPUTS - The device's have two reference input connections and one external reference tap. The reference bottom force connection is typically connected to a -2V reference source (please see the applications diagram) and a reference top force connection typically tied to analog ground. The reference mid tap should be bypassed to analog ground for further noise suppression.

DIGITAL OUTPUT CODING

MINV LINV	0 0	0 1	1 0	1 1
0V	1111 1111	1000 0000	0111 1111	0000 0000
	1111 1110	1000 0001	0111 1110	0000 0001
	1000 0000	1111 1111	0000 0000	0111 1111
	0111 1111	0000 0000	1111 1111	1000 0000
	0000 0001	0111 1110	1000 0001	1111 1110
-2V	0000 0000	0111 1111	1000 0000	1111 1111

TIMING DIAGRAM