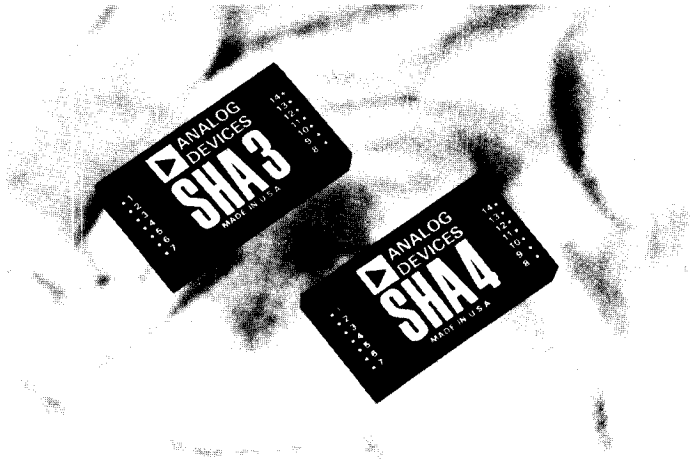
Low Cost, Low Droop, Sample-and-Hold

SHA-3, -4, -5

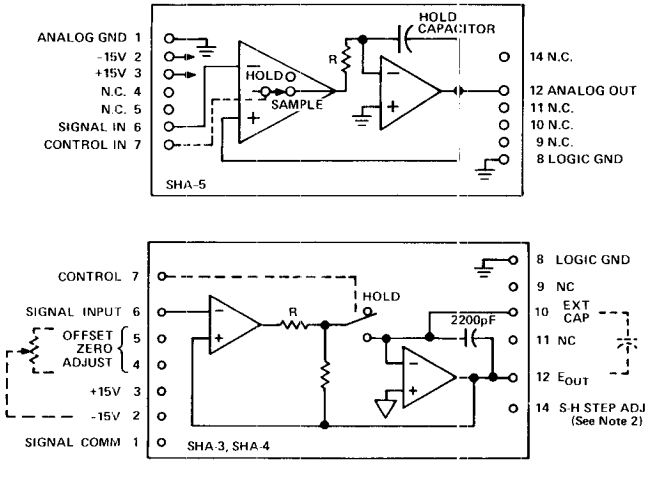
FEATURES
- **Low Tracking Error: 0.01% at Low Frequency**
- **Low Drift: 10μV/°C (SHA-3, 4)**
- **Low Droop Rate: 10μV/ms (SHA-3, 4)**
- **Short Aperture: 40ns**
- **High Input Impedance in Sample Mode: 4×10^9 ohms**
- **DTL/TTL Compatible**
- **Compact Module: 1 1/8" x 2" x 0.4"**

APPLICATIONS
- **Data Acquisition**
- **Data Distribution**
- **Peak and Valley Measurement**
- **Simultaneous Sample and Hold**



GENERAL DESCRIPTION

The SHA-3 to -5 are a family of general purpose sample and hold amplifiers built in a very compact module package. When DTL or TTL Logic "1" is applied at the control input, the operating mode is "Sample", and the output tracks the input at unity gain, without polarity inversion. When Logic "0" is applied, the operating mode is "Hold", and the output remains at the value just prior to the opening of the switch. See Figure 1.



Notes: (SHA-3, -4)
1. Offset zero adjustment: (optional)
   a. Sample mode, signal input grounded, adjust for output zero.
2. Sample-to-Hold offset step trim (optional) 100Ω max; Adjust for minimum offset step when external capacitor is used.

Figure 1. Simplified Block Diagrams

TRACKING LOOP

Charge proportional to the instantaneous value of input signal voltage is stored in the hold capacitor (see Figure 1). Since this capacitor is connected in a high gain feedback loop, its charging current is provided by an amplifier. Thus, the SHA's are relatively easy to apply, since capacitor charging current does not have to be supplied by the signal source.

DYNAMIC PERFORMANCE

Of prime importance in selecting sample and hold amplifiers is the transition characteristic when the module is commanded into "Hold" by the application of a logic "0" to the control input. A finite delay occurs between the application of the hold command and the response of the internal switching circuit. In the SHA-5, this "aperture delay" time is 40ns. The aperture jitter, or the cycle to cycle repeatability of aperture delay, is approximately 4ns. In most systems and for most applications, the jitter specification is the limiting factor on overall system speed for a given accuracy, since the essentially fixed aperture delay can be compensated by adjusting the system timing.

The SHA-5 settles to 0.01% in 15μs or less after a 20 volt step input. When switched to "Hold", the switching transient settles to ±1mV within 2μs. Since aperture jitter is approximately 4ns, an input signal slewing at a rate of 12.5mV/μs will be acquired to appreciably better than one LSB uncertainty for a 12 bit A/D converter.

The SHA-3 and SHA-4 are characterized by low droop rate of 10μV/ms and are ideally suited for most data acquisition and data distribution applications.

APPLICATIONS

In the design of sample and hold amplifiers, the major tradeoff is usually in connection with speed of acquisition and droop in "Hold". As the size of the storage capacitor is increased, the droop rate improves and the acquisition time lengthens. The SHA-5, conceived as a general purpose product, has been designed with droop rate appropriate for use with almost all successive approximation A/D converters; it is also well suited for use in data distribution systems using D/A converters with up to 12 bit resolution, where the data update rate is not slower than approximately 10 per second. The 15μs settling time makes the SHA-5 appropriate for use with all but the fastest A/D converters.

SPECIFICATIONS (typical @ +25°C and nominal supply voltages, unless otherwise specified)

MODEL	SHA-3	SHA-4	SHA-5
ACCURACY			
Gain	+1	*	*
Gain Error	±0.01%	*	*
Gain Tempco	±1ppm/°C max	*	±0.3ppm/°C
SAMPLE MODE DYNAMICS			
Small Signal Frequency Response (-3dB)	50kHz	*	1.4MHz
Full Power Bandwidth	10kHz	*	30kHz
Settling Time to 0.01% (20V input step)	100μs max	20μs	15μs max
Overload Recovery (50% overload)	150μs	*	10μs
SAMPLE TO HOLD SWITCHING			
Aperture Delay Time	50ns	*	40ns
Aperture Jitter	5ns	*	~4ns
Switching Transient Settling Time (to ±1mV)	10μs	*	2μs
Sample-to-Hold Offset	1mV max	*	3mV (10mV max)
HOLDING CHARACTERISTICS			
Droop Rate	10μV/ms max	*	50μV/ms (250μV/ms max)
Feedthrough (20V p-p @ 1kHz in)	2mV p-p		1mV p-p
INPUT CHARACTERISTICS			
Resistance (Sample Mode) min	100MΩ	*	4 x 10^9Ω
Bias Current (Sample Mode)	200nA	*	25nA
Offset, Initial (Adj to 0)	±1.0mV	*	±1mV (±2mV max)
Offset vs Temp, max	±10μV/°C	*	±20μV/°C
Offset vs Supply, max	±0.015mV/%ΔV	*	±10μV/%ΔV
Input Voltage Range min	±10V	*	±10V
OUTPUT CHARACTERISTICS			
Output Voltage	±10V @ 10mA	*	*
Capacitance Load	1000pF	*	*
DIGITAL CONTROL LOGIC LEVELS (DTL/TTL Compatible)			
("1") Sample	+2 to +5.5V @ 15nA	*	*
("0") Hold	-0.5 to +0.8V @ 100μA	*	*
POWER REQUIREMENTS			
Supply Voltage	±15V ±2%	*	*
Quiescent Current	±15mA	±18mA	+30, -25mA
TEMPERATURE RANGE			
Operating	0 to +70°C	*	*
Storage	-55°C to +85°C	*	*
DIMENSIONS	1" x 2" x 0.4"	*	*
	(28.5mm x 50.8mm x 10mm)	*	*

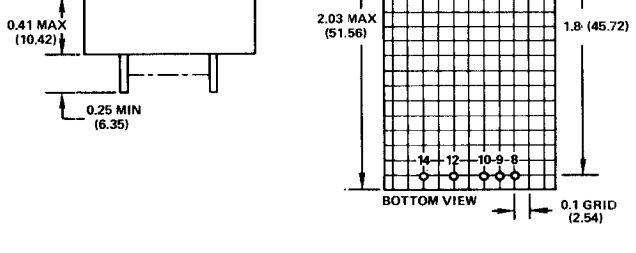
*Specifications same as SHA-3.

Specifications subject to change without notice.

NOTE: Switching the SHA-5 from SAMPLE to HOLD causes a 6mA decrease in the +15V supply current. This rapid change in current can induce voltage transients in certain types of power supplies which will couple directly onto the output terminal. To minimize this effect, a capacitor, such as a 100μF tantalum, should be connected between pins 1 and 3.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTES:

1. Pins: 0.019 ±0.001 (0.48mm ±0.02mm) dia. half-hard brass, gold plated per MIL-G-45204B, Class I, Type II.
2. Grid and markings next to pins are for reference only, and do not appear on unit.
3. Mating socket AC4102 or pin sockets P/N 2-330808-8 (7 required).