

# High-Speed Schottky Priority Encoders

## SN54/74S148 (93S18) SN54/74S348

### Features/Benefits

- Second-generation Schottky designs feature VERY-High-Speed compared to other TTL priority encoders
- Totem-pole outputs on SN54/74S148
- Three-state outputs on SN54/74S348
- SN54/74S148 is speed upgrade for SN54/74148, SN54/74LS148, 9318, 93L18
- SN54/74S348 is speed upgrade for SN54/74LS348
- Encode eight data lines to 3-bit binary (octal) code
- Cascadable in several different ways
- Glitch on  $\overline{GS}$  line in other TTL priority encoders has been designed out
- Applications include:
  - Interrupt/status scanning
  - Resource allocation in processors/peripherals
  - Normalization in floating-point arithmetic units
  - Bus arbitration
- Maximum Logic Delays:
 

• $\overline{D}_i \rightarrow \overline{A}_i$	13ns	}	'S148 and 'S348
• $\overline{D}_i \rightarrow \overline{GS}$	15ns		
• $\overline{D}_i \rightarrow \overline{EO}$	15ns		
• $t_{ZX}(E_i \text{ to } A_i)$	18ns	}	'S348 Only
• $t_{XZ}(E_i \text{ to } A_i)$	15ns		

### Description

The SN54/74S148 and SN54/74S348 high-speed Schottky TTL priority encoders scan 8 data-input lines, and output a 3-bit binary (that is, "octal") code which is the line number of the highest-priority data input being asserted. To allow expansion by cascading, in some cases without external logic, both devices provide three control signals:  $\overline{EI}$  (Enable Input),  $\overline{EO}$  (Enable Output), and  $\overline{GS}$  (Group Select).

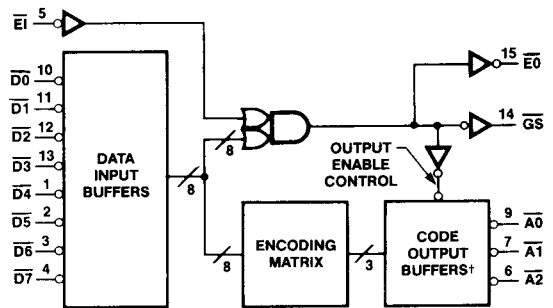
When  $\overline{EI}$  is not being asserted, the code outputs are forced High in the 'S148 and into Hi-Z state in the 'S348. When  $\overline{EI}$  is being asserted, these outputs are forced to the line-number code; see "Function Table." Also, when  $\overline{EI}$  is being asserted,  $\overline{EO}$  and  $\overline{GS}$  are complementary;  $\overline{EO}$  indicates that no data-input line is being asserted, whereas  $\overline{GS}$  indicates that at least one of them is being asserted.

$\overline{EI}$  and  $\overline{EO}$  may be used to link encoders together in a "daisy-chained" configuration. Also, in a two-level cascaded configuration, the  $\overline{GS}$  signals from the first-level encoders are the data inputs for the second-level encoder(s); see "Applications."

### Ordering Information

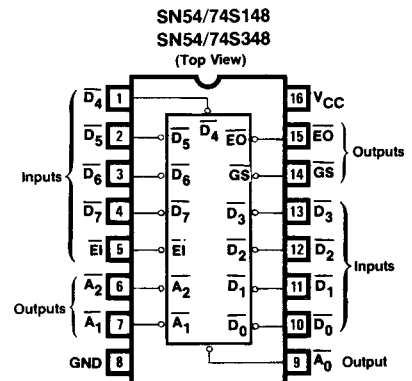
PART NUMBER	PKG	TEMP	OUTPUTS	POWER
SN54S148	J,F,W(20L)	Mil	Totem-pole	S
SN74S148	N,J	Com		
SN54S348	J,F,W(20L)	Mil	Three-state	
SN74S348	N,J	Com		

### Block Diagram



† Disabled outputs are High for 54/74S148 and Hi-Z for 54/74S348.

### Pin Configuration

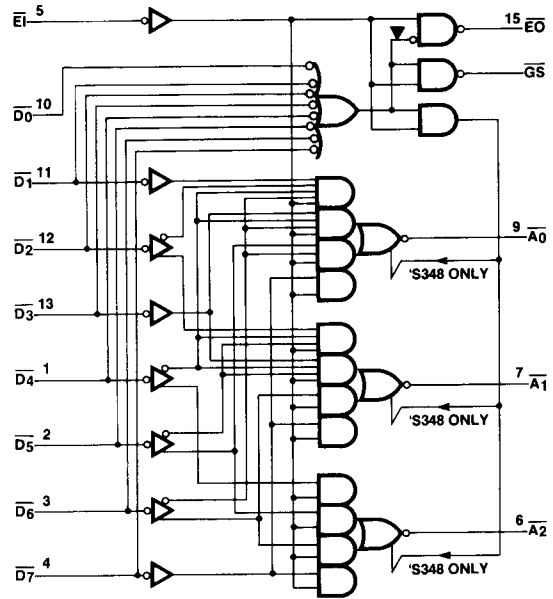


The line-number-code outputs ( $\overline{A_2}$ ,  $\overline{A_1}$ ,  $\overline{A_0}$ ) are totem-pole in the 'S148 and are three-state in the 'S348. All inputs and outputs of both devices are TTL-compatible. Data inputs present two standard 54S/74S normalized loads; EI, however, presents only a half of one such load.

The "Function Table" has been stated in terms of High (H) and Low (L) signal levels rather than in terms of "ones" and "zeroes." The most natural interpretation of the operation of these parts is that *all* signals, outputs as well as inputs, are *assertive-low* — that is, L is identified with "one" and H with "zero." Consequently, the highest-priority data input is named "D<sub>7</sub>" and the output code it produces when asserted is LLL. In like manner, asserting the input D<sub>4</sub> produces the output code LHH if none of the higher-priority data-input lines D<sub>7</sub>, D<sub>6</sub>, or D<sub>5</sub> is being asserted; and so forth.

It is consistent with this interpretation that an 'S148 outputs a code of HHH either when it is disabled, or when it is enabled but none of its data inputs are being asserted. Under the same circumstances, the code outputs of an 'S348 go into Hi-Z state.

**Logic Diagram**



**Function Table**

INPUTS								OUTPUTS				
$\overline{EI}$	$\overline{D_0}$	$\overline{D_1}$	$\overline{D_2}$	$\overline{D_3}$	$\overline{D_4}$	$\overline{D_5}$	$\overline{D_6}$	$\overline{A_2}$	$\overline{A_1}$	$\overline{A_0}$	$\overline{GS}$	$\overline{EO}$
H	X	X	X	X	X	X	X	H/Z*	H/Z*	H/Z*	H	H
L	H	H	H	H	H	H	H	H/Z*	H/Z*	H/Z*	H	L
L	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	L	H	H	H	L	H	L	L	H
L	X	X	L	H	H	H	H	L	L	L	L	H
L	X	L	H	H	H	H	H	L	H	L	L	H
L	L	H	H	H	H	H	H	H	H	L	L	H

\* NOTE: "H" for 'S148, "Z" for 'S348

### Absolute Maximum Ratings

Supply voltage $V_{CC}$ .....	Operating -0.5 V to 7 V
Input voltage .....	-1.5 V to 7 V
Off-state output voltage .....	-0.5 V to 5.5 V
Storage temperature range .....	-65° to +150°C

### Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$I_{OH}$	High level output current			-1			-1	mA
$I_{OL}$	Low level output current			20			20	mA
$T_A$	Operating free air temperature	-55		+125	0		+75	°C

### Electrical Characteristics Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IL}$	Low-level input voltage					0.8			0.8	V
$V_{IH}$	High-level input voltage			2			2			V
$V_{IC}$	Input clamp voltage		$V_{CC} = \text{MIN}$ $I_I = -18\text{mA}$			-1.2			-1.2	V
$I_{IL}$	Low-level input current	$\bar{E}I$ Input	$V_{CC} = \text{MAX}$ $V_I = 0.5\text{V}$			-0.8			-0.8	mA
		Any Input Except $\bar{E}I$				-3.2		-3.2		
$I_{IH}$	High-level input current		$V_{CC} = \text{MAX}$ $V_I = 2.7\text{V}$			50			50	$\mu\text{A}$
$I_I$	Input current		$V_{CC} = \text{MAX}$ $V_I = 5.5\text{V}$			1			1	mA
$V_{OL}$	Low-level output voltage		$V_{CC} = \text{MIN}$ $V_{IH} = 2\text{V}$ $V_{IL} = 0.8\text{V}$ $I_{OL} = 20\text{mA}$			.5			.5	V
$V_{OH}$	High-level output voltage		$V_{CC} = \text{MIN}$ $V_{IH} = 2\text{V}$ $V_{IL} = 0.8\text{V}$ $I_{OH} = -1.0\text{mA}$	2.5	3.4		2.7	3.4		V
$I_{OZL}$	Off-state output current Low-level voltage applied	(S348 Only)	$V_{CC} = \text{MAX}$ $V_{IL} = 0.8\text{V}$ $V_{IH} = 2\text{V}$ $V_O = 0.4\text{V}$			-50			-50	$\mu\text{A}$
$I_{OZH}$	Off-state output current High-level voltage applied	(S348 Only)	$V_{CC} = \text{MAX}$ $V_{IL} = 0.8\text{V}$ $V_{IH} = 2\text{V}$ $V_O = 2.7\text{V}$			50			50	$\mu\text{A}$
$I_{OS}$	Short-circuit output current †		$V_{CC} = \text{MAX}$	-40		-100	-40		-100	mA
$I_{CC}$	Supply current See note 1	'S148	$V_{CC} = \text{MAX}$			115			110	mA
		'S348				125		120		

NOTE 1:  $I_{CC}$  is measured with inputs  $\bar{D}_7$  and  $\bar{E}I$  Low, other inputs High, and outputs open.

† Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

**Switching Characteristics**  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

SYMBOL	PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay	Low to High	$\overline{D}_1$ thru $\overline{D}_7$	$\overline{A}_0, \overline{A}_1, \text{ or } \overline{A}_2$	$C_L = 15\text{ pf}$ $R_L = 280\Omega$	9	13	ns	
$t_{PHL}$		High to Low				9	13	ns	
$t_{PLH}$		Low to High	$\overline{D}_0$ thru $\overline{D}_7$	$\overline{GS}$		11	15	ns	
$t_{PHL}$		High to Low				11	15	ns	
$t_{PLH}$		Low to High				$\overline{EO}$	12	15	ns
$t_{PHL}$		High to Low					12	15	ns
$t_{PLH}$		Low to High	$\overline{EI}$	$\overline{GS}$		6	9	ns	
$t_{PHL}$		High to Low				6	9	ns	
<b>SN54/74S148 ONLY</b>									
$t_{PLH}$	Propagation delay	Low to High	$\overline{EI}$	$\overline{EO}$	$C_L = 15\text{ pf}$ $R_L = 280\Omega$	8	12	ns	
$t_{PHL}$		High to Low				8	12	ns	
$t_{PLH}$		Low to High		$\overline{A}_0, \overline{A}_1, \text{ or } \overline{A}_2$		10	13	ns	
$t_{PHL}$		High to Low				10	13	ns	
<b>SN54/74S348 ONLY</b>									
$t_{PLH}$	Propagation delay	Low to High	$\overline{EI}$	$\overline{EO}$	$C_L = 15\text{ pf}$ $R_L = 280\Omega$	11	14	ns	
$t_{PHL}$		High to Low				11	14	ns	
$t_{PZH}$		Three-state to High		$\overline{A}_0, \overline{A}_1, \text{ or } \overline{A}_2$	$C_L = 50\text{ pf}$	12	18	ns	
$t_{PZL}$		Three-state to Low				$R_L = 280\Omega$	12	18	ns
$t_{PHZ}$		High to Three-state		$\overline{A}_0, \overline{A}_1, \text{ or } \overline{A}_2$	$C_L = 5\text{ pf}$ $R_L = 280\Omega$	8	15	ns	
$t_{PLZ}$		Low to Three-state				8	15	ns	
$t_{PZH}$		Three-state to High		$\overline{D}_0$ thru $\overline{D}_7^*$	$\overline{A}_0, \overline{A}_1, \text{ or } \overline{A}_2$	N/A†	13		ns
$t_{PZL}$		Three-state to Low					13		ns
$t_{PHZ}$		High to Three-state					20		ns
$t_{PLZ}$		Low to Three-state					26		ns

\* NOTE: Refer to second line of "Function Table".

† NOTE: These values are furnished for the purpose of estimating the logic delays of a combination such as shown in Fig. 1 and 2. They are design guidelines only and are not tested and therefore not guaranteed.

### Applications

The basic logic function performed by these priority encoders is to scan a parallel word of any length for the most-significant Low signal in a field of Highs. Although a single part has only 8 data inputs and hence can only scan a one-byte field, the architecture of these parts supports several different cascading schemes.

The Enable Input ( $\bar{E}1$ ), when *not* being asserted, forces the code outputs ( $\bar{A}2, \bar{A}1, \bar{A}0$ ) High in an 'S148 or into Hi-Z (high-impedance) state in an 'S348. Since all input signals and all output signals for these parts are conventionally considered as assertive-low, the effect is to disable the code outputs in the manner appropriate for a totem-pole part ('S148) or a three-state part ('S348). When  $\bar{E}1$  is asserted, the code outputs are forced to the code of the highest-priority data inputs being asserted; if no data input is being asserted, the code outputs remain as if the part were not enabled.

Also, when  $\bar{E}1$  is being asserted, the  $\bar{E}0$  and  $\bar{G}S$  signals operate as complementary "presence" signals. When the encoder asserts  $\bar{E}0$ , this condition means that none of the data inputs for that encoder are being asserted, and that a lower-priority encoder should therefore be enabled to examine its data inputs. Thus, several encoders may be daisy-chained as in Figures 1 and 2, with  $\bar{E}0$  from the highest-priority encoder controlling  $\bar{E}1$  for the next-highest-priority encoder, and so forth. The highest-priority-encoder is always enabled. In such daisy-chain arrangements, code outputs may simply be bussed together if three-state encoders are being used, or combined using external assertive-low "OR" logic. Figure 1 illustrates a three-encoder daisy chain to scan 24 lines; a two-encoder daisy-chain may likewise be used to scan 16 lines. In each of these cases, no other components besides encoders are needed.

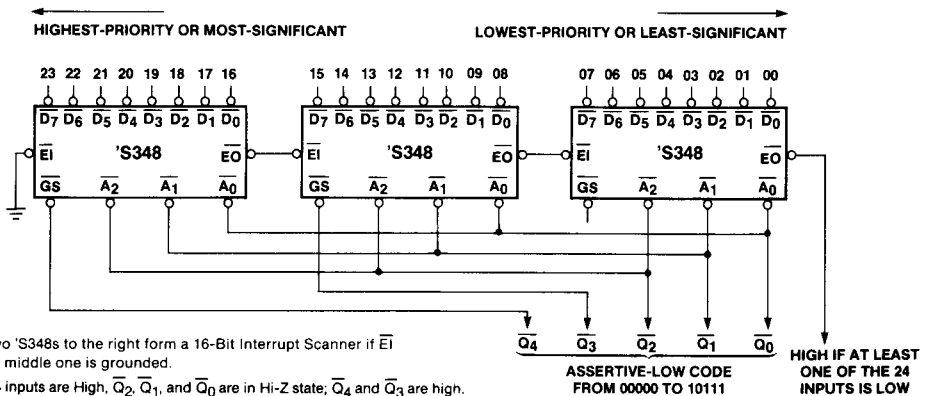
A slightly different approach is needed to scan more than 24 lines. Figure 2 shows a 64-line scanner which uses 9 'S348s and no other components. These encoders are on two "levels"; the  $\bar{G}S$  outputs from the first-level encoders are the inputs for the second-level encoder, and indicate when asserted that the corresponding first-level encoders do indeed have inputs being asserted. The bussed first-level-encoder outputs form the least-significant octal digit of the 6-bit line-number code for the highest-priority data-input line being asserted; the outputs of the second-level encoder form the most-significant octal digit

of this result. Figure 3 shows the highest-speed "totally-parallel" approach, which eliminates the potential delay due to daisy-chaining the enable signal through the first-level parts. The  $\bar{E}1$  signals for all of the encoders are grounded, and an 8-way 3-bit multiplexer comprised of three 'S151s or three 'S251s is used to select the code outputs of the highest-priority first-level encoder which has any data-input lines being asserted. The address lines of these multiplexers are controlled by the code outputs of the second-level encoder.

Yet another cascading scheme, not shown, uses a single decoder such as an 'S138 instead of three multiplexers. The decoder's address-input lines are controlled by the second-level-encoder outputs as in Figure 3. Its outputs go to the  $\bar{E}1$  inputs of the first-level encoders, so that *only* the highest-priority first-level encoder which has any data-input lines being asserted gets enabled. The first-level-encoder code outputs are bussed together as in Figure 2. This scheme is not quite as fast as that of Figure 3, but is faster than that of Figure 2 since the daisy-chaining delay is still eliminated.

The scheme of Figure 3 can be implemented with either totem-pole or three-state parts; the others require three-state parts. Additional schemes are possible. If more than 64 lines must be scanned, more than two levels of encoders can be used. Obviously, also, if only 48 or 56 lines must be scanned, a partially-populated version of one of the 64-bit schemes can do the job.

Although the original system purpose of priority encoders was to scan interrupt lines, they are also ideally suited for high-speed normalization scanning of the result of a floating-point adder/subtractor, in order to determine how many leading zeroes the result contains in order that the normalization shift may be performed in one operation by a "barrel shifter" or "matrix shifter." This result must be in "Negative Absolute Value" form because of the assertive-low behavior of the encoder. (See Monolithic Memories Application note AN-111, "Big, Fast, and Simple — Algorithms, Architecture, and Components for High-End-Superminis," by Ehud Gordon and Chuck Hastings, pages 7-8.) Another important application is "resource control" in computer systems having several semi-autonomous active units; for instance, a single encoder followed by a decoder can arbitrate requests on 8 bus-request lines and return a single bus-grant signal on one of 8 bus-grant lines.



- NOTES: 1. The two 'S348s to the right form a 16-Bit Interrupt Scanner if  $\bar{E}1$  for the middle one is grounded.  
 2. If all 24 inputs are High,  $\bar{Q}2, \bar{Q}1,$  and  $\bar{Q}0$  are in Hi-Z state;  $\bar{Q}4$  and  $\bar{Q}3$  are high.

Figure 1. 24-Bit Leading-Zeros Detector or Interrupt Scanner Using 'S348s and No External Components

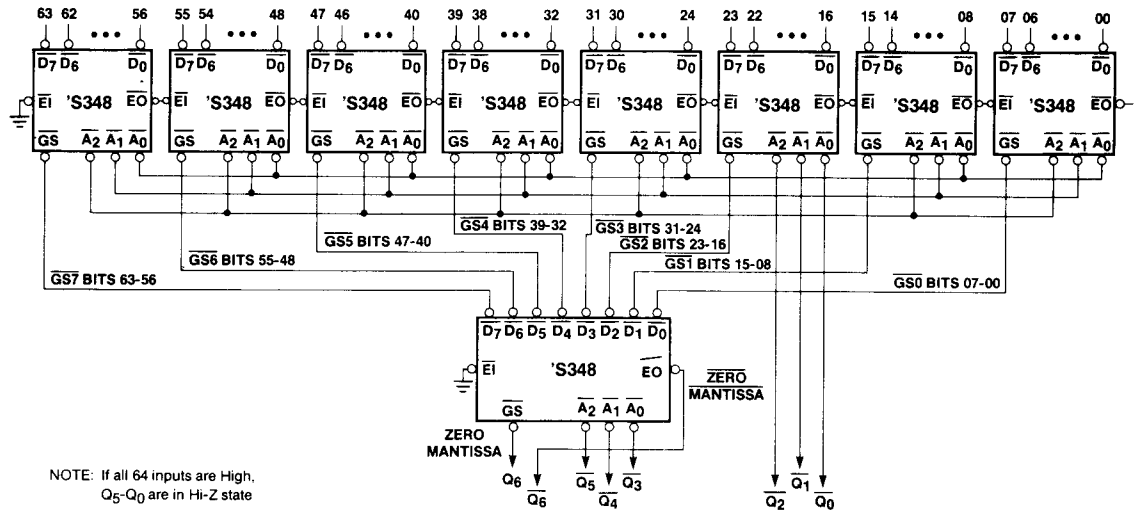


Figure 2. 64-Bit Leading-Zeros Detector or Interrupt Scanner Using 'S348s and No External Components

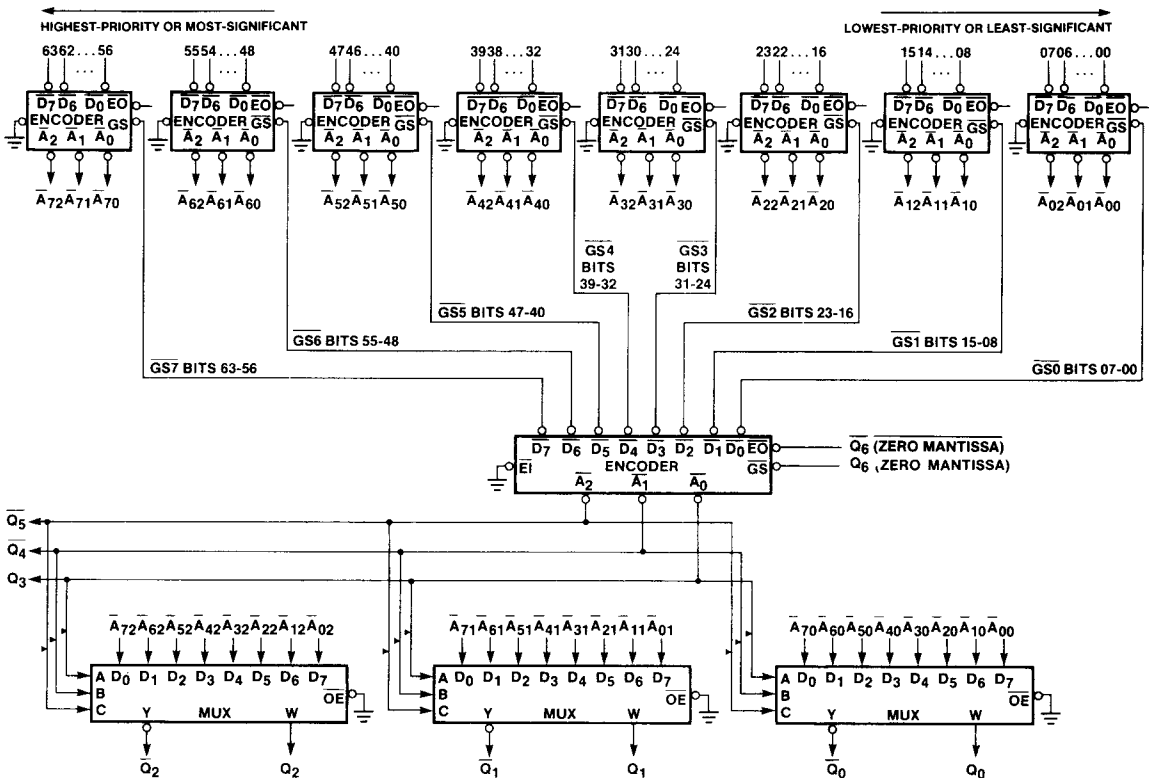
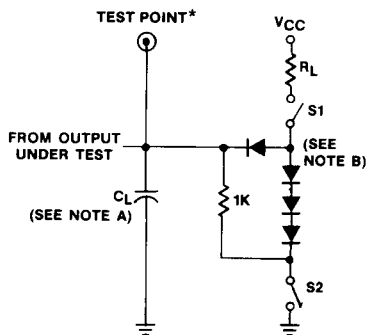
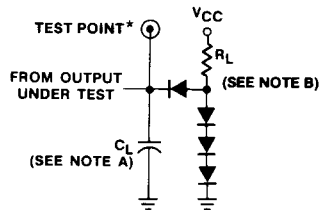


Figure 3. Totally-Parallel 64-Bit Leading-Zeros Detector or Interrupt Scanner

## Test Loads



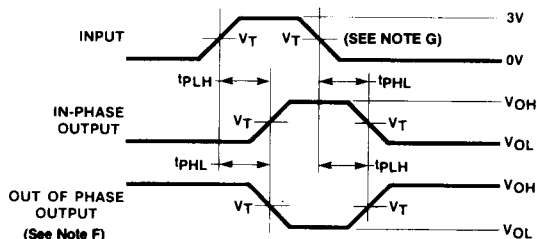
LOAD CIRCUIT FOR  
THREE-STATE OUTPUTS



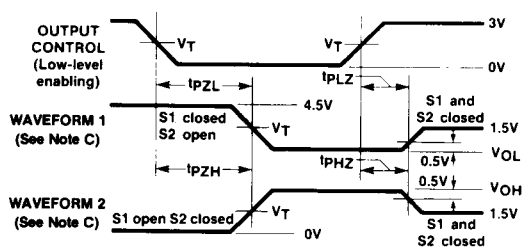
LOAD CIRCUIT FOR  
BI-STATE  
TOTEM-POLE OUTPUTS

\* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

## Test Waveforms



PROPAGATION DELAY



ENABLE AND DISABLE

NOTES: A.  $C_L$  includes probe and jig capacitance.

B. All diodes are 1N916 or 1N3064

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

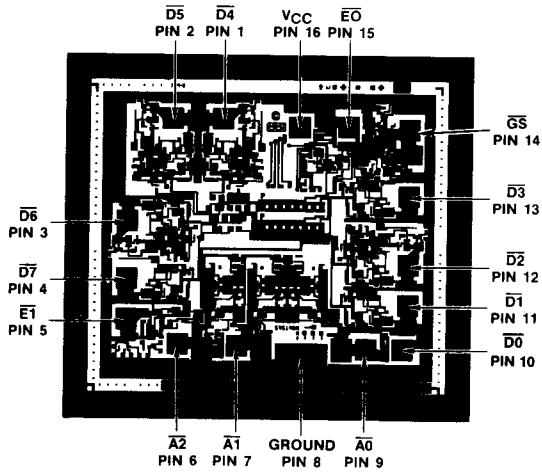
E. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1$  MHz,  $Z_{out} = 50\Omega$  and:

F. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

G.  $V_T = 1.5V$

Die Configurations

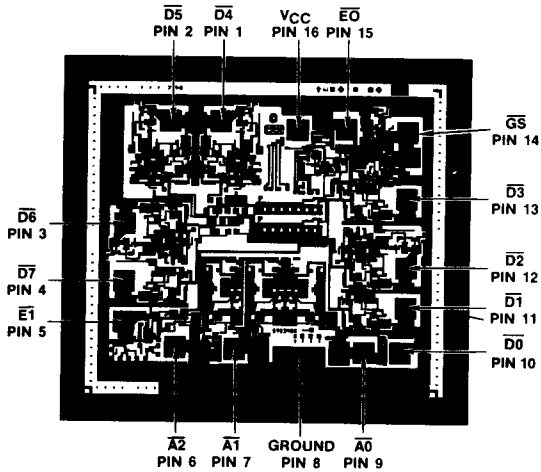
SN54/74S148



Die Size: 81x70 mil<sup>2</sup>

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SN54/74S348



Die Size: 81x70 mil<sup>2</sup>