To all our customers

Information regarding change of names mentioned within this document, to Renesas Technology Corp.

On April 1st 2003 the following semiconductor operations were transferred to Renesas Technology Corporation: operations covering microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.).
Accordingly, although Hitachi, Hitachi, Ltd., Hitachi Semiconductors, and other Hitachi brand names are mentioned in the document, these names have all been changed to Renesas Technology Corporation.
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Renesas Technology Corp.
April 1, 2003

RENESAS

Renesas Technology Corp.

Preliminary

HD66761

(128 x 80-dot Graphics LCD Controller/Driver for 256 Colors)

HITACHI

Rev 0.5
July 4, 2000

Description

The HD66761, color-graphics LCD controller and driver LSI, displays 128-by-80-dot graphics for 256 STN colors. It consists of upper and lower screens and drives maximum 128-by-160-dot STN color LCDs. The HD66761's bit-operation functions and a 16-bit high-speed bus interface enable efficient data transfer and high-speed rewriting of data to the graphics RAM.

The HD66761 has various functions for reducing the power consumption of an LCD system, such as low-voltage operation of 2.2 V/min., a step-up circuit to generate a maximum of seven-times the LCD drive voltage from the supplied voltage, and voltage-followers to decrease the direct current flow in the LCD drive bleeder-resistors. Combining these hardware functions with software functions, such as a partial display with low-duty drive and standby and sleep modes, allows precise power control. The HD66761 is suitable for any mid-sized or small portable battery-driven product requiring long-term driving capabilities, such as digital cellular phones supporting a WWW browser, bidirectional pagers, and small PDAs.

Features

- 128 × 80-dot graphics display LCD controller/driver for 256 STN colors
- Display mode change between 256 colors (8 bits per pixel) and four colors (2-bit per pixel)
- 16-/8-bit high-speed bus interface
- Bit-operation functions for graphics processing:
  - Write-data mask function in bit units
  - Swap function of upper and lower bytes
  - Logical operation in pixel unit and conditional write function
- Various color-display control functions:
  - 256 of the 4,096 possible colors can be displayed at the same time (grayscale palette incorporated)
  - Vertical scroll display function in raster-row units
  - Horizontal scroll display function in four-pixel units
  - Color window cursor display supported by hardware
- Low-power operation supports:
  - Vcc = 2.2 to 3.6 V (low voltage)
  - V_{LCD} (= V_{LPS} – GND) = 5 to 15.5 V (liquid crystal drive voltage)

  - — Four-, five-, six-, or seven-times step-up circuit for liquid crystal drive voltage
  - — 128-step contrast adjuster and voltage followers to decrease direct current flow in the LCD drive bleeder-resistors
  - — Power-save functions such as the standby mode and sleep mode
  - — Partial LCD drive of two screens in any position
  - — Programmable drive duty ratios (1/16–1/80) and bias values (1/5–1/10) displayed on LCD
- Parallel operation for two vertical screens (up to maximum 128-by-160-dot display)
- Internal RAM capacity: 10,240 bytes
- 384-segment × 80-common liquid crystal display driver
- n-raster-row AC liquid-crystal drive (C-pattern waveform drive)
- Internal oscillation and hardware reset
- Shift change of segment and common drivers

<Target values>

Total Current Consumption Characteristics (Vcc = 2.5 V, TYP Conditions, LCD Drive Power Current Included)

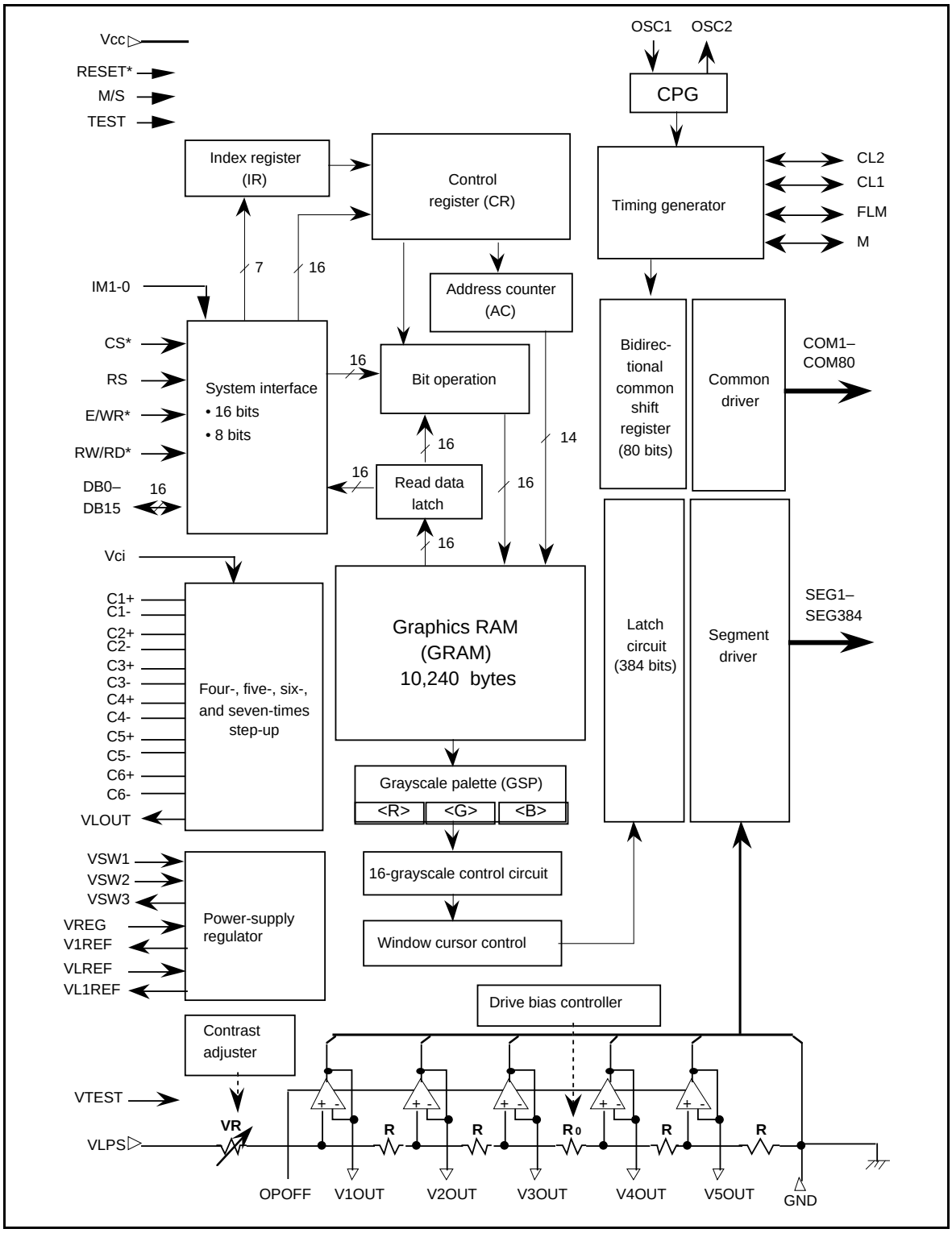
				Total Power Consumption				
				Normal Display Operation				
Character Display Dot Size	Duty Ratio	R-C Oscillation Frequency	Frame Frequency	Internal Logic	LCD Power	Total*	Sleep Mode	Standby Mode
128 x 16 dots	1/16	180 kHz	70 Hz	(35 µA)	(25 µA)	Four-times (135 µA)	(15 µA)	0.1 µA
128 x 24 dots	1/24	180 kHz	70 Hz	(40 µA)	(25 µA)	Four-times (140 µA)	(15 µA)	
128 x 56 dots	1/56	180 kHz	70 Hz	(85 µA)	(25 µA)	Five-times (210 µA)	(15 µA)	
128 x 64 dots	1/64	180 kHz	70 Hz	(90 µA)	(25 µA)	Five-times (220 µA)	(15 µA)	
128 x 72 dots	1/72	180 kHz	70 Hz	(95 µA)	(25 µA)	Six-times (245 µA)	(15 µA)	
128 x 80 dots	1/80	180 kHz	70 Hz	(100 µA)	(25 µA)	Six-times (250 µA)	(15 µA)	

Note: When a four-, five-, six-, or seven-times step-up is used:
the total power consumption = internal logic current + LCD power current x 4 (four-times step-up),
the total power consumption = internal logic current + LCD power current x 5 (five-times step-up),
the total power consumption = internal logic current + LCD power current x 6 (six-times step-up), and
the total power consumption = internal logic current + LCD power current x 7 (seven-times step-up)

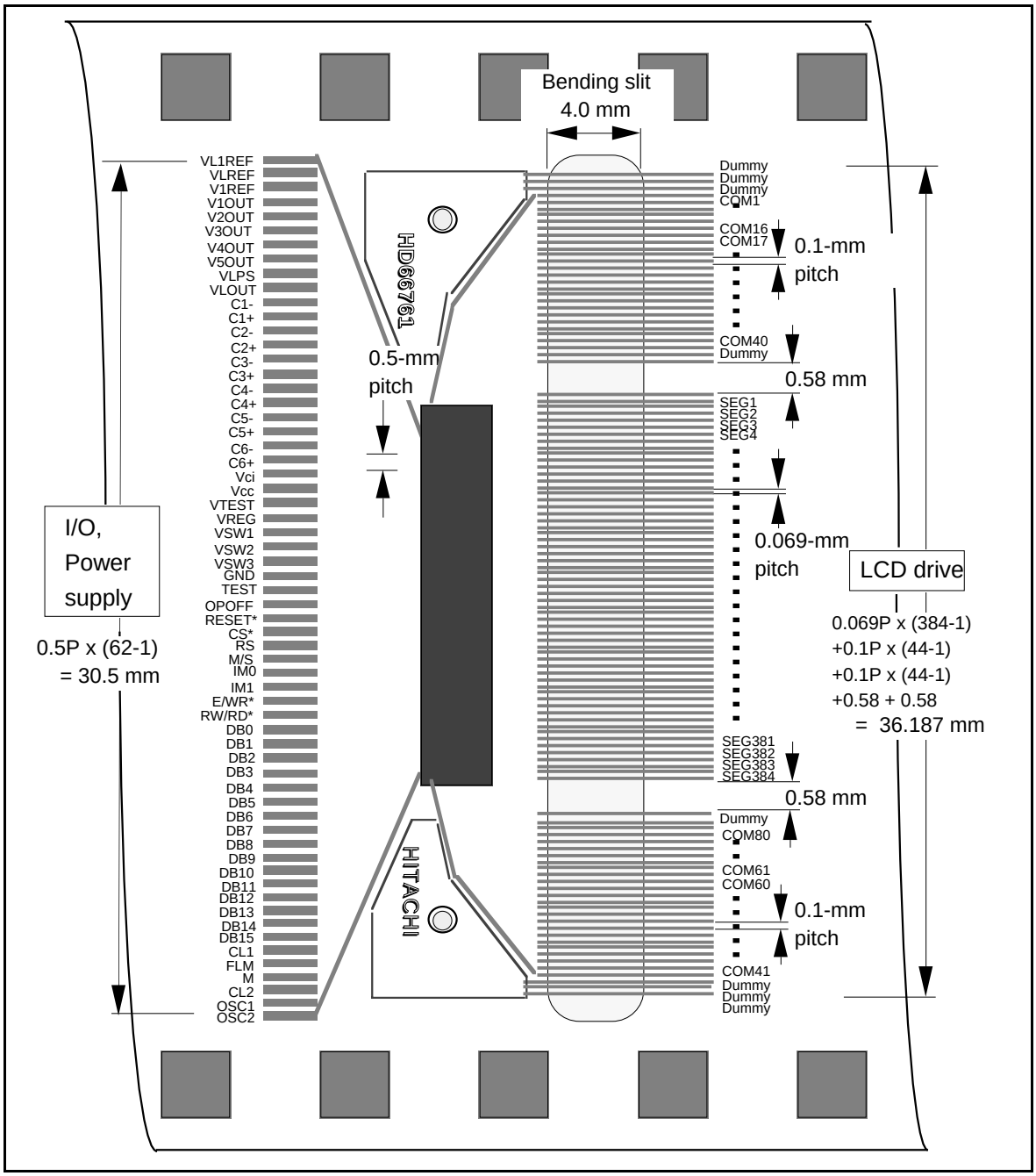
Type Name

Types	External Dimensions	COM Driver Arrangement	Display
HD66761TB0	Bending TCP	Both sides of COM (Output from both sides of the chip)	256 RGB colors
HCD66761BP	Au-bump chip		

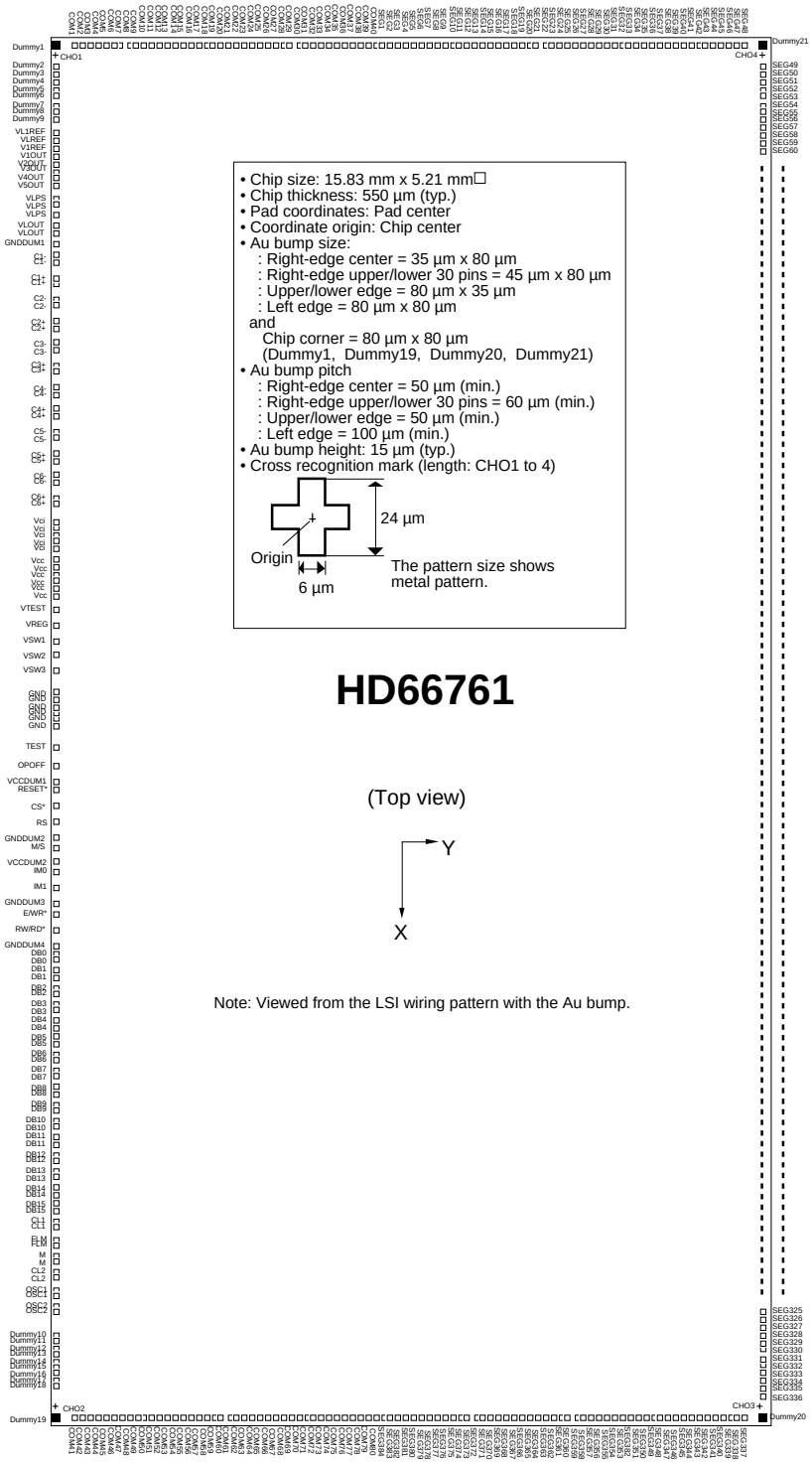
HD66761 Block Diagram



TCP Dimensions (HD66761TB0)



Pad Arrangement



HD66761 Pad Coordinate

No.	Pad Name	X (㎛)	Y (㎛)
1	DUMMY1	-7721	-2411
2	DUMMY2	-7520	-2411
3	DUMMY3	-7420	-2411
4	DUMMY4	-7320	-2411
5	DUMMY5	-7220	-2411
6	DUMMY6	-7120	-2411
7	DUMMY7	-7020	-2411
8	DUMMY8	-6920	-2411
9	DUMMY9	-6820	-2411
10	VL1REF	-6620	-2411
11	VLREF	-6520	-2411
12	V1REF	-6420	-2411
13	V1OUT	-6320	-2411
14	V2OUT	-6219	-2411
15	V3OUT	-6119	-2411
16	V4OUT	-6019	-2411
17	V5OUT	-5919	-2411
18	VLPS	-5769	-2411
19	VLPS	-5669	-2411
20	VLPS	-5569	-2411
21	VLOUT	-5419	-2411
22	VLOUT	-5319	-2411
23	GNDDUM1	-5169	-2411
24	CAP1-	-5069	-2411
25	CAP1-	-4968	-2411
26	CAP1+	-4868	-2411
27	CAP1+	-4768	-2411
28	CAP2-	-4668	-2411
29	CAP2-	-4568	-2411
30	CAP2+	-4468	-2411
31	CAP2+	-4368	-2411
32	CAP3-	-4268	-2411
33	CAP3-	-4168	-2411
34	CAP3+	-4068	-2411
35	CAP3+	-3968	-2411
36	CAP4-	-3868	-2411
37	CAP4-	-3767	-2411
38	CAP4+	-3667	-2411
39	CAP4+	-3567	-2411
40	CAP5-	-3467	-2411
41	CAP5-	-3367	-2411
42	CAP5+	-3267	-2411
43	CAP5+	-3167	-2411
44	CAP6-	-3067	-2411
45	CAP6-	-2967	-2411
46	CAP6+	-2867	-2411
47	CAP6+	-2767	-2411
48	Vci	-2617	-2411
49	Vci	-2516	-2411
50	Vci	-2416	-2411
51	Vci	-2316	-2411
52	Vci	-2216	-2411
53	Vcc	-2027	-2411
54	Vcc	-1927	-2411
55	Vcc	-1827	-2411
56	Vcc	-1727	-2411
57	Vcc	-1627	-2411
58	Vcc	-1527	-2411
59	VTEST	-1327	-2411
60	VREG	-1127	-2411
61	VSW1	-926	-2411
62	VSW2	-726	-2411
63	VSW3	-526	-2411
64	GND	-395	-2411
65	GND	-295	-2411
66	GND	-195	-2411
67	GND	-95	-2411
68	GND	5	-2411
69	GND	105	-2411
70	TEST	236	-2411
71	OPOFF	433	-2411
72	VCCDUM1	536	-2411
73	RESET	636	-2411
74	CS	836	-2411
75	RS	1036	-2411
76	GNDDUM2	1136	-2411
77	M/S	1237	-2411
78	VCCDUM2	1337	-2411
79	IM0	1437	-2411
80	IM1	1637	-2411
81	GNDDUM3	1737	-2411
82	EWR	1837	-2411
83	RW/RD	2037	-2411
84	GNDDUM4	2137	-2411
85	DB0	2237	-2411
86	DB0	2337	-2411
87	DB1	2437	-2411
88	DB1	2538	-2411
89	DB2	2638	-2411
90	DB2	2738	-2411
91	DB3	2838	-2411
92	DB3	2938	-2411
93	DB4	3038	-2411
94	DB4	3138	-2411
95	DB5	3238	-2411
96	DB5	3338	-2411
97	DB6	3438	-2411
98	DB6	3538	-2411
99	DB7	3638	-2411
100	DB7	3739	-2411
101	DB8	3839	-2411
102	DB8	3939	-2411
103	DB9	4039	-2411
104	DB9	4139	-2411
105	DB10	4239	-2411
106	DB10	4339	-2411
107	DB11	4439	-2411
108	DB11	4539	-2411
109	DB12	4639	-2411
110	DB12	4739	-2411
111	DB13	4839	-2411
112	DB13	4939	-2411
113	DB14	5040	-2411
114	DB14	5140	-2411
115	DB15	5240	-2411
116	DB15	5340	-2411
117	CL1	5440	-2411
118	CL1	5540	-2411
119	FLM	5640	-2411
120	FLM	5740	-2411
121	M	5840	-2411
122	M	5940	-2411
123	CL2	6040	-2411
124	CL2	6140	-2411
125	OSC1	6241	-2411
126	OSC1	6341	-2411
127	OSC2	6441	-2411
128	OSC2	6541	-2411
129	DUMMY10	6641	-2411
130	DUMMY11	6780	-2411
131	DUMMY12	6920	-2411
132	DUMMY13	7020	-2411
133	DUMMY14	7120	-2411
134	DUMMY15	7220	-2411
135	DUMMY16	7320	-2411
136	DUMMY17	7420	-2411
137	DUMMY18	7520	-2411
138	DUMMY19	7721	-2411
139	COM41	7721	-2231
140	COM42	7721	-2181
141	COM43	7721	-2131
142	COM44	7721	-2081
143	COM45	7721	-2030
144	COM46	7721	-1980
145	COM47	7721	-1930
146	COM48	7721	-1880
147	COM49	7721	-1830
148	COM50	7721	-1780
149	COM51	7721	-1730
150	COM52	7721	-1680
151	COM53	7721	-1630
152	COM54	7721	-1580
153	COM55	7721	-1530
154	COM56	7721	-1480
155	COM57	7721	-1430
156	COM58	7721	-1380
157	COM59	7721	-1330
158	COM60	7721	-1280
159	COM61	7721	-1230
160	COM62	7721	-1180
161	COM63	7721	-1130
162	COM64	7721	-1080
163	COM65	7721	-1030
164	COM66	7721	-980
165	COM67	7721	-930
166	COM68	7721	-880
167	COM69	7721	-830
168	COM70	7721	-779
169	COM71	7721	-729
170	COM72	7721	-679
171	COM73	7721	-629
172	COM74	7721	-579
173	COM75	7721	-529
174	COM76	7721	-479
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176	COM78	7721	-379
177	COM79	7721	-329
178	COM80	7721	-279
179	SEG384	7721	-229
180	SEG383	7721	-179
181	SEG382	7721	-129
182	SEG381	7721	-79
183	SEG380	7721	-29
184	SEG379	7721	21
185	SEG378	7721	71
186	SEG377	7721	121
187	SEG376	7721	171
188	SEG375	7721	221
189	SEG374	7721	271
190	SEG373	7721	321
191	SEG372	7721	371
192	SEG371	7721	421
193	SEG370	7721	472
194	SEG369	7721	522
195	SEG368	7721	572
196	SEG367	7721	622
197	SEG366	7721	672
198	SEG365	7721	722
199	SEG364	7721	772
200	SEG363	7721	822
201	SEG362	7721	872
202	SEG361	7721	922
203	SEG360	7721	972
204	SEG359	7721	1022
205	SEG358	7721	1072
206	SEG357	7721	1122
207	SEG356	7721	1172
208	SEG355	7721	1222
209	SEG354	7721	1272
210	SEG353	7721	1322
211	SEG352	7721	1372
212	SEG351	7721	1422
213	SEG350	7721	1472
214	SEG349	7721	1522
215	SEG348	7721	1572
216	SEG347	7721	1622
217	SEG346	7721	1672
218	SEG345	7721	1723
219	SEG344	7721	1773
220	SEG343	7721	1823
221	SEG342	7721	1873
222	SEG341	7721	1923
223	SEG340	7721	1973
224	SEG339	7721	2023
225	SEG338	7721	2073
226	SEG337	7721	2123
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237	SEG327	6937	2411
238	SEG326	6877	2411
239	SEG325	6817	2411
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241	SEG323	6697	2411
242	SEG322	6636	2411
243	SEG321	6576	2411
244	SEG320	6516	2411
245	SEG319	6456	2411
246	SEG318	6396	2411
247	SEG317	6336	2411
248	SEG316	6276	2411
249	SEG315	6216	2411
250	SEG314	6155	2411
251	SEG313	6095	2411
252	SEG312	6035	2411
253	SEG311	5975	2411
254	SEG310	5915	2411
255	SEG309	5855	2411
256	SEG308	5795	2411
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260	SEG304	5579	2411
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262	SEG302	5479	2411
263	SEG301	5429	2411
264	SEG300	5379	2411
265	SEG299	5329	2411
266	SEG298	5279	2411
267	SEG297	5229	2411
268	SEG296	5179	2411
269	SEG295	5129	2411
270	SEG294	5079	2411
271	SEG293	5029	2411
272	SEG292	4979	2411
273	SEG291	4929	2411
274	SEG290	4879	2411
275	SEG289	4829	2411
276	SEG288	4779	2411
277	SEG287	4729	2411
278	SEG286	4679	2411
279	SEG285	4629	2411
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283	SEG281	4429	2411
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304	SEG260	3378	2411
305	SEG259	3328	2411
306	SEG258	3278	2411
307	SEG257	3228	2411
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324	SEG240	2377	2411
325	SEG239	2327	2411
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328	SEG236	2177	2411
329	SEG235	2127	2411
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336	SEG228	1776	2411
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372	SEG192	-25	2411
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381	SEG183	-475	2411
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383	SEG181	-575	2411
384	SEG180	-626	2411
385	SEG179	-676	2411
386	SEG178	-726	2411
387	SEG177	-776	2411
388	SEG176	-826	2411
389	SEG175	-876	2411
390	SEG174	-926	2411
391	SEG173	-976	2411
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393	SEG171	-1076	2411
394	SEG170	-1126	2411
395	SEG169	-1176	2411
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405	SEG159	-1676	2411
406	SEG158	-1726	2411
407	SEG157	-1776	2411
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409	SEG155	-1877	2411
410	SEG154	-1927	2411
411	SEG153	-1977	2411
412	SEG152	-2027	2411
413	SEG151	-2077	2411
414	SEG150	-2127	2411
415	SEG149	-2177	2411
416	SEG148	-2227	2411
417	SEG147	-2277	2411
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423	SEG141	-2577	2411
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444	SEG120	-3628	2411
445	SEG119	-3678	2411
446	SEG118	-3728	2411
447	SEG117	-3778	2411
448	SEG116	-3828	2411
449	SEG115	-3878	2411
450	SEG114	-3928	2411
451	SEG113	-3978	2411
452	SEG112	-4028	2411
453	SEG111	-4078	2411
454	SEG110	-4128	2411
455	SEG109	-4178	2411
456	SEG108	-4228	2411
457	SEG107	-4278	2411
458	SEG106	-4328	2411
459	SEG105	-4379	2411
460	SEG104	-4429	2411
461	SEG103	-4479	2411
462	SEG102	-4529	2411
463	SEG101	-4579	2411
464	SEG100	-4629	2411
465	SEG99	-4679	2411
466	SEG98	-4729	2411
467	SEG97	-4779	2411
468	SEG96	-4829	2411
469	SEG95	-4879	2411
470	SEG94	-4929	2411
471	SEG93	-4979	2411
472	SEG92	-5029	2411
473	SEG91	-5079	2411
474	SEG90	-5129	2411
475	SEG89	-5179	2411
476	SEG88	-5229	2411
477	SEG87	-5279	2411
478	SEG86	-5329	2411
479	SEG85	-5379	2411
480	SEG84	-5429	2411
481	SEG83	-5479	2411
482	SEG82	-5529	2411
483	SEG81	-5579	2411
484	SEG80	-5630	2411
485	SEG79	-5680	2411
486	SEG78	-5735	2411
487	SEG77	-5795	2411
488	SEG76	-5855	2411
489	SEG75	-5915	2411
490	SEG74	-5975	2411
491	SEG73	-6035	2411
492	SEG72	-6095	2411
493	SEG71	-6155	2411
494	SEG70	-6216	2411
495	SEG69	-6276	2411
496	SEG68	-6336	2411
497	SEG67	-6396	2411
498	SEG66	-6456	2411
499	SEG65	-6516	2411
500	SEG64	-6576	2411
501	SEG63	-6636	2411
502	SEG62	-6697	2411
503	SEG61	-6757	2411
504	SEG60	-6817	2411
505	SEG59	-6877	2411
506	SEG58	-6937	2411
507	SEG57	-6997	2411
508	SEG56	-7057	2411
509	SEG55	-7117	2411
510	SEG54	-7178	2411
511	SEG53	-7238	2411
512	SEG52	-7298	2411
513	SEG51	-7358	2411
514	SEG50	-7418	2411
515	SEG49	-7478	2411
516	DUMMY21	-7721	2411
517	SEG48	-7721	2123
518	SEG47	-7721	2073
519	SEG46	-7721	2023
520	SEG45	-7721	1973
521	SEG44	-7721	1923
522	SEG43	-7721	1873
523	SEG42	-7721	1823
524	SEG41	-7721	1773
525	SEG40	-7721	1723
526	SEG39	-7721	1672
527	SEG38	-7721	1622
528	SEG37	-7721	1572
529	SEG36	-7721	1522
530	SEG35	-7721	1472
531	SEG34	-7721	1422
532	SEG33	-7721	1372
533	SEG32	-7721	1322
534	SEG31	-7721	1272
535	SEG30	-7721	1222
536	SEG29	-7721	1172
537	SEG28	-7721	1122
538	SEG27	-7721	1072
539	SEG26	-7721	1022
540	SEG25	-7721	972
541	SEG24	-7721	922
542	SEG23	-7721	872
543	SEG22	-7721	822
544	SEG21	-7721	772
545	SEG20	-7721	722
546	SEG19	-7721	672
547	SEG18	-7721	622
548	SEG17	-7721	572
549	SEG16	-7721	522
550	SEG15	-7721	472
551	SEG14	-7721	421
552	SEG13	-7721	371
553	SEG12	-7721	321
554	SEG11	-7721	271
555	SEG10	-7721	221
556	SEG9	-7721	171
557	SEG8	-7721	121
558	SEG7	-7721	71
559	SEG6	-7721	21
560	SEG5	-7721	-29
561	SEG4	-7721	-79
562	SEG3	-7721	-129
563	SEG2	-7721	-179
564	SEG1	-7721	-229
565	COM40	-7721	-279
566	COM39	-7721	-329
567	COM38	-7721	-379
568	COM37	-7721	-429
569	COM36	-7721	-479
570	COM35	-7721	-529
571	COM34	-7721	-579
572	COM33	-7721	-629
573	COM32	-7721	-679
574	COM31	-7721	-729
575	COM30	-7721	-779
576	COM29	-7721	-830
577	COM28	-7721	-880
578	COM27	-7721	-930
579	COM26	-7721	-980
580	COM25	-7721	-1030
581	COM24	-7721	-1080
582	COM23	-7721	-1130
583	COM22	-7721	-1180
584	COM21	-7721	-1230
585	COM20	-7721	-1280
586	COM19	-7721	-1330
587	COM18	-7721	-1380
588	COM17	-7721	-1430
589	COM16	-7721	-1480
590	COM15	-7721	-1530
591	COM14	-7721	-1580
592	COM13	-7721	-1630
593	COM12	-7721	-1680
594	COM11	-7721	-1730
595	COM10	-7721	-1780
596	COM9	-7721	-1830
597	COM8	-7721	-1880
598	COM7	-7721	-1930
599	COM6	-7721	-1980
600	COM5	-7721	-2030
601	COM4	-7721	-2081
602	COM3	-7721	-2131
603	COM2	-7721	-2181
604	COM1	-7721	-2231
Length 1 (CHO1)		-7619	-2411
Length 2 (CHO2)		7619	-2411
Length 3 (CHO3)		7619	2411
Length 4 (CHO4)		-7619	2411

Pin Functions

Table 1 Pin Functional Description

Signals	Number of Pins	I/O	Connected to	Functions
IM1, IM0	2	I	GND or V_{CC}	Selects the MPU interface mode: IM1 / IM0 / MPU interface mode GND / GND / 68-system 16-bit bus interface GND / Vcc / 68-system 8-bit bus interface Vcc / GND / 80-system 16-bit bus interface Vcc / Vcc / 80-system 8-bit bus interface
CS*	1	I	MPU	Selects the HD66761: Low: HD66761 is selected and can be accessed High: HD66761 is not selected and cannot be accessed Must be fixed at GND level when not in use.
RS	1	I	MPU	Selects the register. Low: Index/status High: Control
E/WR*	1	I	MPU	For a 68-system bus interface, serves as an enable signal to activate data read/write operation. For an 80-system bus interface, serves as a write strobe signal and writes data at the low level.
RW/RD*	1	I	MPU	For a 68-system bus interface, serves as a signal to select data read/write operation. Low: Write High: Read For an 80-system bus interface, serves as a read strobe signal and reads data at the low level.
DB0–DB15	16	I/O	MPU	Serves as a 16-bit bidirectional data bus. For an 8-bit bus interface, data transfer uses DB15-DB8; fix unused DB7-DB0 to the Vcc or GND level.
COM1–COM80	80	O	LCD	Output signals for common drive: All the unused pins output unselected waveforms. In the display-off period (D1–0 = 00, 01), sleep mode (SLP = 1), or standby mode (STB = 1), all pins output GND level. The CMS bit can change the shift direction of the common signal. For example, if CMS = 0, COM1 shifts to COM80. If CMS = 1, COM80 shifts to COM1. Note that the start position of the common output is shifted by screen-division driving.
SEG1–SEG384	384	O	LCD	Output signals for segment drive. In the display-off period (D1–0 = 00, 01), sleep mode (SLP = 1), or standby mode (STB = 1), all pins output GND level. The SGS bit can change the shift direction of the segment signal. For example, if SGS = 0, RAM address 0000 is output from SEG1. If SGS = 1, it is output from SEG384. SEG1, SEG4, SEG7, ... display red (R), SEG2, SEG5, SEG8, ... display green (G), and SEG3, SEG6, SEG9, ... display blue (B) (SGS = 0).

Table 1 Pin Functional Description (cont)

Signals	Number of Pins	I/O	Connected to	Functions
V1OUT–V5 OUT	5	I/O	Capacitor or master/slave	Used for output from the internal operational amplifiers when they are used (OPOFF = GND); attach a capacitor to stabilize the output. When the amplifiers are not used (OPOFF = V_{CC}), V1 to V5 voltages can be supplied to these pins from the master side. Adjust the contrast for V1OUT ≥ V_{CC}, V_{Ci}.
V_{LPS}	1	—	Power supply	Power supply for LCD drive. V_{LCD} (= V_{LPS} – GND) = 15.5 V max.
V_{CC}, GND	2	—	Power supply	V_{CC}: +2.2 V to + 3.6 V; GND (logic): 0 V
OSC1, OSC2	2	I or O	Oscillation-resistor (master)	In the master mode, connect an external resistor for R-C oscillation. In the slave mode, fix OSC1 to GND and open OSC2.
Vci	1	I	Power supply	Inputs a reference voltage and supplies power to the step-up circuit; generates the liquid crystal display drive voltage from the operating voltage. The step-up output voltage must not be larger than the absolute maximum ratings. Must be left disconnected when the step-up circuit is not used.
VLOUT	1	O	V_{LPS} pin/step-up capacitance	Potential difference between Vci and GND is four- to seven-times-stepped up and then output. Magnitude of step-up is selected by instruction.
C1+, C1–	2	—	Step-up capacitance	External capacitance should be connected here for step-up.
C2+, C2–	2	—	Step-up capacitance	External capacitance should be connected here for step-up.
C3+, C3–	2	—	Step-up capacitance	External capacitance should be connected here for step-up.
C4+, C4–	2	—	Step-up capacitance	External capacitance should be connected here for step-up.
C5+, C5–	2	—	Step-up capacitance	External capacitance should be connected here for step-up.
C6+, C6–	2	—	Step-up capacitance	External capacitance should be connected here for step-up.
CL2	1	I/O	Master/slave	In the master mode, the operating clock for slave is output. In the slave mode, the operating clock is input.
CL1	1	I/O	Master/slave	In the master mode, the one-raster-row-cycle pulse is output. In the slave mode, the one-raster-row-cycle pulse is input.
M	1	I/O	Master/slave	In the master mode, the AC-cycle signal is output. In the slave mode, the AC-cycle signal is input.
FLM	1	I/O	Master/slave	In the master mode, the frame-start pulse is output. In the slave mode, the frame-start pulse is input.

Table 1 Pin Functional Description (cont)

Signals	Number of Pins	I/O	Connected to	Functions
M/S	1	I	Vcc or GND	Enters the master mode in V_{cc} level, and the slave mode in GND level. When one M/S is used, be sure to set the master mode.
RESET*	1	I	MPU or external R-C circuit	Reset pin. Initializes the LSI when low. Must be reset after power-on.
OPOFF	1	I	V_{CC} or GND	Turns the internal operational amplifier off when OPOFF = V_{CC}, and turns it on when OPOFF = GND. In the slave mode, turn off the amplifier and supply V1 to V5 on the master side to the V1OUT to V5OUT pins.
VSW1, VSW2	2	I	GND	Test pins. Must be VSW1, VSW2 = GND, and VSW3 = open.
VSW3	1	O	—	
VREG	1	I	Input pin	This pin is used when the reference voltage of the internal power-supply regulator is externally supplied. When the internal reference voltage (1/2 Vci) is used, VREG must be opened since the 1/2-Vci level is output.
VLREF	1	I	Input pin	Use this pin when the LCD drive voltage is externally supplied. When the internal power-supply regulator is used, short VLREF with the V1REF pin.
V1REF	1	O	Output pin	Outputs the LCD drive voltage generated in the internal power-supply regulator. Insert this pin when the external temperature-compensation circuit is used between V1REF and VLREF. If the circuit is not used, short V1REF and VLREF.
VccDUM	2	O	Input pins	Outputs the internal V_{CC} level; shorting this pin sets the adjacent input pin to the V_{CC} level.
GNDDUM	4	O	Input pins	Outputs the internal GND level; shorting this pin sets the adjacent input pin to the GND level.
Dummy	4	—	—	Dummy pad. Must be left disconnected.
TEST	1	I	GND	Test pin. Must be fixed at GND level.
VTEST	1	—	—	Test pin. Must be left disconnected.
VL1REF	1	O	—	Test pin. Must be left disconnected.

Block Function Description

System Interface

The HD66761 has four high-speed system interfaces: an 80-system 16-bit/8-bit bus and a 68-system 16-bit/8-bit bus. The interface mode is selected by the IM1-0 pins.

The HD66761 has three 16-bit registers: an index register (IR), a write data register (WDR), and a read data register (RDR). The IR stores index information from the control registers and the GRAM. The WDR temporarily stores data to be written into control registers and the GRAM, and the RDR temporarily stores data read from the GRAM. Data written into the GRAM from the MPU is first written into the WDR and then is automatically written into the GRAM by internal operation. Data is read through the RDR when reading from the GRAM, and the first read data is invalid and the second and the following data are normal. When a logic operation is performed inside of the HD66761 by using the display data set in the GRAM and the data written from the MPU, the data read through the RDR is used. Accordingly, the MPU does not need to read data twice nor to fetch the read data into the MPU. This enables high-speed processing.

Execution time for instruction excluding oscillation start is 0 clock cycle and instructions can be written in succession.

Table 2 Register Selection

80-series Bus		68-series Bus		
WR Bits	**RD Bits**	**R/W Bits**	**RS Bits**	**Operations**
0	1	0	0	Writes indexes into IR
1	0	1	0	Reads internal status
0	1	0	1	Writes into control registers and GRAM through WDR
1	0	1	1	Reads from GRAM through RDR

Bit Operation

The HD66761 supports the following functions: a swap function that writes the data written from the MPU into the GRAM by reversing the display position vertically in byte units, a write data mask function that selects and writes data into the GRAM in bit units, and a logic operation function that performs logic operations or conditional determination on the display data set in the GRAM and writes into the GRAM. With the 16-bit bus interface, these functions can greatly reduce the processing loads of the MPU graphics software and can rewrite the display data in the GRAM at high speed. For details, see the Graphics Operation Function section.

Address Counter (AC)

The address counter (AC) assigns addresses to the GRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC.

After writing into the GRAM, the AC is automatically incremented by 1 (or decremented by 1). After reading from the data, the AC is not updated.

Graphics RAM (GRAM)

The graphics RAM (GRAM) has eight bits/pixel and stores the bit-pattern data of 128 x 80 bytes.

Grayscale Palette (GSP)

The grayscale palette (GSP) is a palette table that converts the information (three bits for each color: two bits for B) read from the GRAM to 4-bit grayscale data. Any 256 of the 4,096 possible colors can be displayed at the same time. For details, see the Grayscale Palette section.

Grayscale Control Circuit

The grayscale control circuit performs 16-grayscale control with the frame rate control (FRC) method for grayscale display for each color. For details, see the Grayscale Palette section.

Timing Generator

The timing generator generates timing signals for the operation of internal circuits such as the GRAM. The RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interference with one another. The timing generator generates the master-slave interface signals (M, FLM, CL1, and CL2) at master/slave operation.

Oscillation Circuit (OSC)

The HD66761 can provide R-C oscillation simply through the addition of an external oscillation-resistor between the OSC1 and OSC2 pins. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the external-resistor value. Clock pulses can also be supplied externally. Since R-C oscillation stops during the standby mode, current consumption can be reduced. For details, see the Oscillation Circuit section.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 80 common signal drivers (COM1 to COM80) and 384 segment signal drivers (SEG1 to SEG384). When the number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output unselected waveforms.

Display pattern data is latched when 384-bit data has arrived. The latched data then enables the segment signal drivers to generate drive waveform outputs. The shift direction of 384-bit data can be changed by the SGS bit. The shift direction for the common driver can also be changed by the CMS bit by selecting an appropriate direction for the device mounting configuration.

When multiplexing drive is not used, or during the standby or sleep mode, all the above common and segment signal drivers output the GND level, halting the display.

Step-up Circuit (DC-DC Converter)

The step-up generates four-, five-, six-, or seven-times voltage input to the Vci pin. With this, both the internal logic units and LCD drivers can be controlled with a single power supply. Step-up output level from four-times to seven-times step-up can be selected by software. For details, see the Power Supply for Liquid Crystal Display Drive section.

V-Pin Voltage Follower

A voltage follower for each voltage level (V1 to V5) reduces current consumption by the LCD drive power supply circuit. No external resistors are required because of the internal bleeder-resistor, which generates different levels of LCD drive voltage. This internal bleeder-resistor can be software-specified from 1/5 bias to 1/10 bias, according to the liquid crystal display drive duty value. For details, see the Power Supply for Liquid Crystal Display Drive section.

Contrast Adjuster

The contrast adjuster can be used to adjust LCD contrast in 128 steps by varying the LCD drive voltage by software. This can be used to select an appropriate LCD brightness or to compensate for temperature.

Power-supply Regulator

The power-supply regulator generates the LCD drive voltage from the reference voltage, which does not depend on the LCD load current. The fluctuating LCD drive voltage can be controlled for the fluctuating LCD load current. For details, see the Liquid Crystal Display Voltage Generator section.

GRAM Address Map (HD66761)

Table 3 Relationship between Display Position and GRAM Address (GS = 0, SGS = 0)

SEG/COM Pin		SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	.....	SEG373	SEG374	SEG375	SEG376	SEG377	SEG378	SEG379	SEG380	SEG381	SEG382	SEG383	SEG384
CMS=0	CMS=1	DB 15		DB 8	DB 7		DB 0	DB 15		DB 8	DB 7		DB 0		DB 15		DB 8	DB 7		DB 0	DB 15		DB 8	DB 7		DB 0
COM1	COM80	"0000"H						"0001"H						.....	"003E"H						"003F"H					
COM2	COM79	"0100"H						"0101"H						.....	"013E"H						"013F"H					
COM3	COM78	"0200"H						"0201"H						.....	"023E"H						"023F"H					
COM4	COM77	"0300"H						"0301"H						.....	"033E"H						"033F"H					
COM5	COM76	"0400"H						"0401"H						.....	"043E"H						"043F"H					
COM6	COM75	"0500"H						"0501H						.....	"053E"H						"053F"H					
COM7	COM74	"0600"H						"0601"H						.....	"063E"H						"063F"H					
COM8	COM73	"0700"H						"0701"H						.....	"073E"H						"073F"H					
COM9	COM72	"0800"H						"0801"H						.....	"083E"H						"083F"H					
COM10	COM71	"0900"H						"0901"H						.....	"093E"H						"093F"H					
COM11	COM70	"0A00"H						"0A01"H						.....	"0A3E"H						"0A3F"H					
COM12	COM69	"0B00"H						"0B01"H						.....	"0B3E"H						"0B3F"H					
COM13	COM68	"0C00"H						"0C01"H						.....	"0C3E"H						"0C3F"H					
COM14	COM67	"0D00"H						"0D01"H						.....	"0D3E"H						"0D3F"H					
COM15	COM66	"0E00"H						"0E01"H						.....	"0E3E"H						"0E3F"H					
COM16	COM65	"0F00"H						"0F01"H						.....	"0F3E"H						"0F3F"H					
COM17	COM64	"1000"H						"1001"H						.....	"103E"H						"103F"H					
COM18	COM63	"1100"H						"1101"H						.....	"113E"H						"113F"H					
COM19	COM62	"1200"H						"1201"H						.....	"123E"H						"123F"H					
COM20	COM61	"1300"H						"1301"H						.....	"133E"H						"133F"H					
⋮	⋮	⋮						⋮							⋮						⋮					
COM73	COM8	"4800"H						"4801"H						.....	"483E"H						"483F"H					
COM74	COM7	"4900"H						"4901"H						.....	"493E"H						"493F"H					
COM75	COM6	"4A00"H						"4A01"H						.....	"4A3E"H						"4A3F"H					
COM76	COM5	"4B00"H						"4B01"H						.....	"4B3E"H						"4B3F"H					
COM77	COM4	"4C00"H						"4C01"H						.....	"4C3E"H						"4C3F"H					
COM78	COM3	"4D00"H						"4D01"H						.....	"4D3E"H						"4D3F"H					
COM79	COM2	"4E00"H						"4E01"H						.....	"4E3E"H						"4E3F"H					
COM80	COM1	"4F00"H						"4F01"H						.....	"4F3E"H						"4F3F"H					

Table 4 Relationship between GRAM Data and Display Contents

GRAM Data	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Selection Palette	RK palette			GK palette			BK palette		RK palette			GK palette			BK palette	
Output Pin	SEG (6n+1)			SEG (6n+2)			SEG (6n+3)		SEG (6n+4)			SEG (6n+5)			SEG (6n+6)	

Note: n = Lower 7-bit address (0 to 63)

Table 5 Relationship between Display Position and GRAM Address (GS = 0, SGS = 1)

SEG/COM Pin		SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	.....	SEG373	SEG374	SEG375	SEG376	SEG377	SEG378	SEG379	SEG380	SEG381	SEG382	SEG383	SEG384
CMS=0	CMS=1	DB 0		DB 7	DB 8		DB 15	DB 0		DB 7	DB 8		DB 15		DB 0		DB 7	DB 8		DB 15	DB 0		DB 7	DB 8		DB 15
COM1	COM80	"003F"H						"003E"H						.....	"0001"H						"0000"H					
COM2	COM79	"013F"H						"013E"H						.....	"0101"H						"0100"H					
COM3	COM78	"023F"H						"023E"H						.....	"0201"H						"0200"H					
COM4	COM77	"033F"H						"033E"H						.....	"0301"H						"0300"H					
COM5	COM76	"043F"H						"043E"H						.....	"0401"H						"0400"H					
COM6	COM75	"053F"H						"053E"H						.....	"0501H						"0500"H					
COM7	COM74	"063F"H						"063E"H						.....	"0601"H						"0600"H					
COM8	COM73	"073F"H						"073E"H						.....	"0701"H						"0700"H					
COM9	COM72	"083F"H						"083E"H						.....	"0801"H						"0800"H					
COM10	COM71	"093F"H						"093E"H						.....	"0901"H						"0900"H					
COM11	COM70	"0A3F"H						"0A3E"H						.....	"0A01"H						"0A00"H					
COM12	COM69	"0B3F"H						"0B3E"H						.....	"0B01"H						"0B00"H					
COM13	COM68	"0C3F"H						"0C3E"H						.....	"0C01"H						"0C00"H					
COM14	COM67	"0D3F"H						"0D3E"H						.....	"0D01"H						"0D00"H					
COM15	COM66	"0E3F"H						"0E3E"H						.....	"0E01"H						"0E00"H					
COM16	COM65	"0F3F"H						"0F3E"H						.....	"0F01"H						"0F00"H					
COM17	COM64	"103F"H						"103E"H						.....	"1001"H						"1000"H					
COM18	COM63	"113F"H						"113E"H						.....	"1101"H						"1100"H					
COM19	COM62	"123F"H						"123E"H						.....	"1201"H						"1200"H					
COM20	COM61	"133F"H						"133E"H						.....	"1301"H						"1300"H					
⋮	⋮	⋮						⋮							⋮						⋮					
COM73	COM8	"483F"H						"483E"H						.....	"4801"H						"4800"H					
COM74	COM7	"493F"H						"493E"H						.....	"4901"H						"4900"H					
COM75	COM6	"4A3F"H						"4A3E"H						.....	"4A01"H						"4A00"H					
COM76	COM5	"4B3F"H						"4B3E"H						.....	"4B01"H						"4B00"H					
COM77	COM4	"4C3F"H						"4C3E"H						.....	"4C01"H						"4C00"H					
COM78	COM3	"4D3F"H						"4D3E"H						.....	"4D01"H						"4D00"H					
COM79	COM2	"4E3F"H						"4E3E"H						.....	"4E01"H						"4E00"H					
COM80	COM1	"4F3F"H						"4F3E"H						.....	"4F01"H						"4F00"H					

Table 6 Relationship between GRAM Data and Display Contents

GRAM Data	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Selection Palette	RK palette			GK palette			BK palette		RK palette			GK palette			BK palette	
Output Pin	SEG (384-6n)			SEG (383-6n)			SEG (382-6n)		SEG (381-6n)			SEG (380-6n)			SEG (379-6n)	

Note: n = Lower 7-bit address (0 to 63)

Table 7 Relationship between Display Position and GRAM Address (GS = 1, SGS = 0)

SEG/COM Pin		SEG1 ... SEG12	SEG13 ... SEG24	SEG25 ... SEG36	SEG37 ... SEG48	.....	SEG337 ... SEG348	SEG349 ... SEG360	SEG361 ... SEG372	SEG373 ... SEG384
CMS=0	CMS=1	DB15 ... DB8	DB7 ... DB0	DB15 ... DB8	DB7 ... DB0		DB15 ... DB8	DB7 ... DB0	DB15 ... DB8	DB7 ... DB0
COM1	COM80	"0000"H		"0001"H		.....	"000E"H		"000F"H	
COM2	COM79	"0100"H		"0101"H		.....	"010E"H		"010F"H	
COM3	COM78	"0200"H		"0201"H		.....	"020E"H		"020F"H	
COM4	COM77	"0300"H		"0301"H		.....	"030E"H		"030F"H	
COM5	COM76	"0400"H		"0401"H		.....	"040E"H		"040F"H	
COM6	COM75	"0500"H		"0501H		.....	"050E"H		"050F"H	
COM7	COM74	"0600"H		"0601"H		.....	"060E"H		"060F"H	
COM8	COM73	"0700"H		"0701"H		.....	"070E"H		"070F"H	
COM9	COM72	"0800"H		"0801"H		.....	"080E"H		"080F"H	
COM10	COM71	"0900"H		"0901"H		.....	"090E"H		"090F"H	
COM11	COM70	"0A00"H		"0A01"H		.....	"0A0E"H		"0A0F"H	
COM12	COM69	"0B00"H		"0B01"H		.....	"0B0E"H		"0B0F"H	
COM13	COM68	"0C00"H		"0C01"H		.....	"0C0E"H		"0C0F"H	
COM14	COM67	"0D00"H		"0D01"H		.....	"0D0E"H		"0D0F"H	
COM15	COM66	"0E00"H		"0E01"H		.....	"0E0E"H		"0E0F"H	
COM16	COM65	"0F00"H		"0F01"H		.....	"0F0E"H		"0F0F"H	
COM17	COM64	"1000"H		"1001"H		.....	"100E"H		"100F"H	
COM18	COM63	"1100"H		"1101"H		.....	"110E"H		"110F"H	
COM19	COM62	"1200"H		"1201"H		.....	"120E"H		"120F"H	
COM20	COM61	"1300"H		"1301"H		.....	"130E"H		"130F"H	
⋮	⋮	⋮		⋮			⋮		⋮	
COM73	COM8	"4800"H		"4801"H		.....	"480E"H		"480F"H	
COM74	COM7	"4900"H		"4901"H		.....	"490E"H		"490F"H	
COM75	COM6	"4A00"H		"4A01"H		.....	"4A0E"H		"4A0F"H	
COM76	COM5	"4B00"H		"4B01"H		.....	"4B0E"H		"4B0F"H	
COM77	COM4	"4C00"H		"4C01"H		.....	"4C0E"H		"4C0F"H	
COM78	COM3	"4D00"H		"4D01"H		.....	"4D0E"H		"4D0F"H	
COM79	COM2	"4E00"H		"4E01"H		.....	"4E0E"H		"4E0F"H	
COM80	COM1	"4F00"H		"4F01"H		.....	"4F0E"H		"4F0F"H	

Notes: 1. When GS = 1, the address is automatically updated in 0000H to 4F0FH.
2. When the GS bit is updated, the RAM data must be rewritten.

Table 8 Relationship between GRAM Data and Display Contents

GRAM Data	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Selection Palette	RK, GK, BK		RK, GK, BK		RK, GK, BK		RK, GK, BK		RK, GK, BK		RK, GK, BK		RK, GK, BK		RK, GK, BK	
Output Pin	SEG (24n+1) ⋮ SEG (24n+3)		SEG (24n+4) ⋮ SEG (24n+6)		SEG (24n+7) ⋮ SEG (24n+9)		SEG (24n+10) ⋮ SEG (24n+12)		SEG (24n+13) ⋮ SEG (24n+15)		SEG (24n+16) ⋮ SEG (24n+18)		SEG (24n+19) ⋮ SEG (24n+21)		SEG (24n+22) ⋮ SEG (24n+24)	

Note: n = Lower 4-bit address (0 to 15)

Table 9 Relationship between Display Position and GRAM Address (GS = 1, SGS = 1)

SEG/COM Pin		SEG1 ..... SEG12	SEG13 ..... SEG24	SEG25 ..... SEG36	SEG37 ..... SEG48	.....	SEG337 ..... SEG348	SEG349 ..... SEG360	SEG361 ..... SEG372	SEG373 ..... SEG384
CMS=0	CMS=1	DB 0 ..... DB 7	DB 8 ..... DB 15	DB 0 ..... DB 7	DB 8 ..... DB 15		DB 0 ..... DB 7	DB 8 ..... DB 15	DB 0 ..... DB 7	DB 8 ..... DB 15
COM1	COM80	"000F"H		"000E"H		.....	"0001"H		"0000"H	
COM2	COM79	"010F"H		"010E"H		.....	"0101"H		"0100"H	
COM3	COM78	"020F"H		"020E"H		.....	"0201"H		"0200"H	
COM4	COM77	"030F"H		"030E"H		.....	"0301"H		"0300"H	
COM5	COM76	"040F"H		"040E"H		.....	"0401"H		"0400"H	
COM6	COM75	"050F"H		"050E"H		.....	"0501H		"0500"H	
COM7	COM74	"060F"H		"060E"H		.....	"0601"H		"0600"H	
COM8	COM73	"070F"H		"070E"H		.....	"0701"H		"0700"H	
COM9	COM72	"080F"H		"080E"H		.....	"0801"H		"0800"H	
COM10	COM71	"090F"H		"090E"H		.....	"0901"H		"0900"H	
COM11	COM70	"0A0F"H		"0A0E"H		.....	"0A01"H		"0A00"H	
COM12	COM69	"0B0F"H		"0B0E"H		.....	"0B01"H		"0B00"H	
COM13	COM68	"0C0F"H		"0C0E"H		.....	"0C01"H		"0C00"H	
COM14	COM67	"0D0F"H		"0D0E"H		.....	"0D01"H		"0D00"H	
COM15	COM66	"0E0F"H		"0E0E"H		.....	"0E01"H		"0E00"H	
COM16	COM65	"0F0F"H		"0F0E"H		.....	"0F01"H		"0F00"H	
COM17	COM64	"100F"H		"100E"H		.....	"1001"H		"1000"H	
COM18	COM63	"110F"H		"110E"H		.....	"1101"H		"1100"H	
COM19	COM62	"120F"H		"120E"H		.....	"1201"H		"1200"H	
COM20	COM61	"130F"H		"130E"H		.....	"1301"H		"1300"H	
⋮	⋮	⋮		⋮			⋮		⋮	
COM73	COM8	"480F"H		"480E"H		.....	"4801"H		"4800"H	
COM74	COM7	"490F"H		"490E"H		.....	"4901"H		"4900"H	
COM75	COM6	"4A0F"H		"4A0E"H		.....	"4A01"H		"4A00"H	
COM76	COM5	"4B0F"H		"4B0E"H		.....	"4B01"H		"4B00"H	
COM77	COM4	"4C0F"H		"4C0E"H		.....	"4C01"H		"4C00"H	
COM78	COM3	"4D0F"H		"4D0E"H		.....	"4D01"H		"4D00"H	
COM79	COM2	"4E0F"H		"4E0E"H		.....	"4E01"H		"4E00"H	
COM80	COM1	"4F0F"H		"4F0E"H		.....	"4F01"H		"4F00"H	

Notes: 1. When GS = 1, the address is automatically updated in 0000H to 4F0FH.
2. When the GS bit is updated, the RAM data must be rewritten.

Table 10 Relationship between GRAM Data and Display Contents

GRAM Data	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Selection Palette	RK, GK, BK		RK, GK, BK		RK, GK, BK		RK, GK, BK		RK, GK, BK		RK, GK, BK		RK, GK, BK		RK, GK, BK	
Output Pin	SEG (384-24n) ⋮ SEG (382-24n)		SEG (381-24n) ⋮ SEG (379-24n)		SEG (378-24n) ⋮ SEG (376-24n)		SEG (375-24n) ⋮ SEG (373-24n)		SEG (372-24n) ⋮ SEG (370-24n)		SEG (369-24n) ⋮ SEG (367-24n)		SEG (366-24n) ⋮ SEG (364-24n)		SEG (363-24n) ⋮ SEG (361-24n)	

Note: n = Lower 4-bit address (0 to 15)

Instructions

Outline

The HD66761 uses the 16-bit bus architecture. Before the internal operation of the HD66761 starts, control information is temporarily stored in the registers described below to allow high-speed interfacing with a high-performance microcomputer. The internal operation of the HD66761 is determined by signals sent from the microcomputer. These signals, which include the register selection signal (RS), the read/write signal (R/W), and the data bus signals (DB15 to DB0), make up the HD66761 instructions. There are eight categories of instructions that:

- Specify the index
- Read the status
- Control the display
- Control power management
- Process the graphics data
- Set internal GRAM addresses
- Transfer data to and from the internal GRAM
- Set grayscale level for the internal grayscale palette table

Normally, instructions that write data are used the most. However, an auto-update of internal GRAM addresses after each data write can lighten the microcomputer program load.

Because instructions are executed in 0 cycles, they can be written in succession.

Instruction Descriptions

Index

The index instruction specifies the RAM control indexes (R00h to R39h). It sets the register number in the range of 000000 to 111001 in binary form. However, R40h to R44h are disabled since they are test registers.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Figure 1 Index Instruction

Status Read

The status read instruction reads the internal status of the HD66761.

L6–0: Indicate the driving raster-row position where the liquid crystal display is being driven.

C6–0: Read the contrast setting values (CT6–0).

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R	0	0	L6	L5	L4	L3	L2	L1	L0	0	C6	C5	C4	C3	C2	C1	C0

Figure 2 Status Read Instruction

Start Oscillation (R00h)

The start oscillation instruction restarts the oscillator from the halt state in the standby mode. After issuing this instruction, wait at least 10 ms for oscillation to stabilize before issuing the next instruction. (See the Standby Mode section.)

If this register is read forcibly, *761H is read. Since the MSB reads the maser/slave setting, 8761H is read when M/S pin = Vcc (master mode), and 0761H is read when M/S pin = GND (slave mode).

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	M/S	0	0	0	0	1	1	1	0	1	1	0	0	0	0	1

Figure 3 Start Oscillation Instruction

Driver Output Control (R01h)

CMS: Selects the output shift direction of a common driver. When CMS = 0, COM1 shifts to COM80. When CMS = 1, COM80 shifts to COM1.

SGS: Selects the output shift direction of a segment driver. When SGS = 0, SEG1 shifts to SEG384. When SGS = 1, SEG384 shifts to SEG1. When SGS = 0, the SEG1 pin assigns the color display to R, G, or B. When SGS = 1, the SEG384 pin assigns R, G, or B to the color display.

NL3–0: Specify the LCD drive duty ratio. The duty ratio can be adjusted for every eight raster-rows. GRAM address mapping does not depend on the setting value of the drive duty ratio.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**CMS**	**SGS**	**0**	**0**	**0**	**0**	**NL3**	**NL2**	**NL1**	**NL0**

Figure 4 Driver Output Control Instruction

Table 11 NL Bits and Drive Duty

NL3	NL2	NL1	NL0	Display Size	LCD Drive Duty	Common Driver Used
0	0	0	0	Setting disabled	Setting disabled	Setting disabled
0	0	0	1	384 x 16 dots	1/16 Duty	COM1–COM16
0	0	1	0	384 x 24 dots	1/24 Duty	COM1–COM24
0	0	1	1	384 x 32 dots	1/32 Duty	COM1–COM32
0	1	0	0	384 x 40 dots	1/40 Duty	COM1–COM40
0	1	0	1	384 x 48 dots	1/48 Duty	COM1–COM48
0	1	1	0	384 x 56 dots	1/56 Duty	COM1–COM56
0	1	1	1	384 x 64 dots	1/64 Duty	COM1–COM64
1	0	0	0	384 x 72 dots	1/72 Duty	COM1–COM72
1	0	0	1	384 x 80 dots	1/80 Duty	COM1–COM80

LCD-Driving-Waveform Control (R02h)

B/C: When B/C = 0, a B-pattern waveform is generated and alternates in every frame for LCD drive. When B/C = 1, a C-pattern waveform is generated and alternates in each raster-row specified by bits EOR and NW4–NW0 in the LCD-driving-waveform control register. For details, see the n-raster-row Reversed AC Drive section.

EOR: When the C-pattern waveform is set (B/C = 1) and EOR = 1, the odd/even frame-select signals and the n-raster-row reversed signals are EORed for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the LCD drive duty ratio and the n raster-row. For details, see the n-raster-row Reversed AC Drive section.

NW4–0: Specify the number of raster-rows n that will alternate at the C-pattern waveform setting (B/C = 1). NW4–NW0 alternate for every set value + 1 raster-row, and the first to the 32nd raster-rows can be selected.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	0	0	0	0	B/C	EOR	NW4	NW3	NW2	NW1	NW0

Figure 5 LCD-Driving-Waveform Control Instruction

Power Control (R03h)

BS2–0: The LCD drive bias value is set within the range of a 1/5 to 1/10 bias. The LCD drive bias value can be selected according to its drive duty ratio and voltage. For details, see the Liquid-crystal-display Drive-bias Selector section.

BT1–0: The output factor of VLOUT between four-times, five-times, six-times, and seven-times step-up is switched. The LCD drive voltage level can be selected according to its drive duty ratio and bias. Lower amplification of the step-up circuit consumes less current.

PS1–0: The internal or external power supply is selected as the reference power supply for the LCD drive-voltage generator.

DC1–0: The operating frequency in the step-up circuit is selected. When the step-up operating frequency is high, the driving ability of the step-up circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.

AP1–0: The amount of fixed current from the fixed current source in the operational amplifier for V pins (V1 to V5) is adjusted. When the amount of fixed current is large, the LCD driving ability and the display quality become high, but the current consumption is increased. Adjust the fixed current considering the display quality and the current consumption.

During no display, when AP1–0 = 00, the current consumption can be reduced by ending the operational amplifier and step-up circuit operation.

SLP: When SLP = 1, the HD66761 enters the sleep mode, where the internal display operations are halted except for the R-C oscillator, thus reducing current consumption. For details, see the Sleep Mode section. Only the following instructions can be executed during the sleep mode.

Power control (BS2–0, BT1–0, DC1–0, AP1–0, SLP, and STB bits)

During the sleep mode, the other GRAM data and instructions cannot be updated although they are retained.

STB: When STB = 1, the HD66761 enters the standby mode, where display operation completely stops, halting all the internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied. For details, see the Standby Mode section.

Only the following instructions can be executed during the standby mode.

a. Standby mode cancel (STB = 0)
b. Start oscillation
c. Power control (BS2–0, BT1–0, DC1–0, AP1–0, SLP, and STB bits)

During the standby mode, the GRAM data and instructions may be lost. To prevent this, they must be set again after the standby mode is canceled.

Table 12 BS Bits and LCD Drive Bias Value

BS2	BS1	BS0	LCD Drive Bias Value
0	0	0	Setting disabled
0	0	1	1/10 bias drive
0	1	0	1/9 bias drive
0	1	1	1/8 bias drive
1	0	0	1/7 bias drive
1	0	1	1/6 bias drive
1	1	0	1/5 bias drive
1	1	1	Setting disabled

Table 13 BT Bits and Output Level

BT1	BT0	VLOUT Output Level
0	0	Four-times step-up
0	1	Five-times step-up
1	0	Six-times step-up
1	1	Seven-times step-up

Table 14 DC Bits and Operating Clock Frequency

DC1	DC0	Operating Clock Frequency in the Step-up Circuit
0	0	32-divided clock
0	1	16-divided clock
1	0	128-divided clock
1	1	64-divided clock

Table 15 AP Bits and Amount of Fixed Current

AP1	AP0	Amount of Fixed Current in the Operational Amplifier
0	0	Operational amplifier and booster do not operate.
0	1	Small
1	0	Middle
1	1	Large

Table 16 Switching Reference Power Supply

PS1	PS0	VREG Pin	V1REF Pin	VLREF Pin
0	0	Output (1/2Vci)	Output (1/2Vci x N-times)	Input (from V1REF pin)
0	1	Input (Vreg)	Output (Vreg x N-times)	Input (from V1REF) Vreg: Voltage input from the VREG pin
1	0	Open (High-Z)	Open (High-Z)	Input (Vlcd: LCD voltage) Vlcd: Voltage input from the VLREF pin
1	1	Setting disabled		

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	**1**	**0**	**0**	**0**	**BS2**	**BS1**	**BS0**	**BT1**	**BT0**	**PS1**	**PS0**	**DC1**	**DC0**	**AP1**	**AP0**	**SLP**	**STB**

Figure 6 Power Control Instruction

Contrast Control (R04h)

CT6–0: These bits control the LCD drive voltage (potential difference between V1 and GND) to adjust 128-step contrast. For details, see the Contrast Adjuster section.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	**1**	**0**	**0**	**0**	**0**	**0**	**VR2**	**VR1**	**VR0**	**0**	**CT6**	**CT5**	**CT4**	**CT3**	**CT2**	**CT1**	**CT0**

Figure 7 Contrast Control Instruction

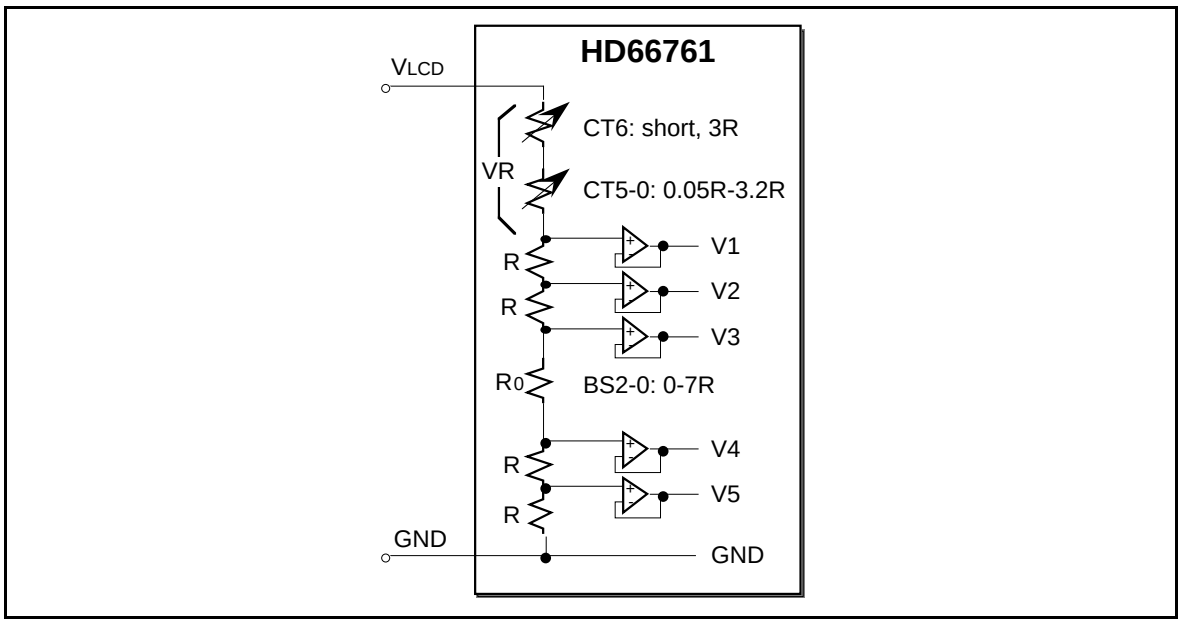


Figure 8 Contrast Adjuster

Table 17 CT Bits and Variable Resistor Value of Contrast Adjuster

CT Set Value						Variable Resistor (VR)	
CT5	**CT4**	**CT3**	**CT2**	**CT1**	**CT0**	**CT6 = 0**	**CT6 = 1**
0	0	0	0	0	0	6.20 x R	3.20 x R
0	0	0	0	0	1	6.15 x R	3.15 x R
0	0	0	0	1	0	6.10 x R	3.10 x R
0	0	0	0	1	1	6.05 x R	3.05 x R
0	0	0	1	0	0	6.00 x R	3.00 x R
			•			•	•
			•			•	•
1	1	1	1	0	1	3.15 x R	0.15 x R
1	1	1	1	1	0	3.10 x R	0.10 x R
1	1	1	1	1	1	3.05 x R	0.05 x R

VR2–0: These bits adjust the output voltage (V1REF) in the LCD drive reference generator in the range of six- to 13-times of Vreg (1/2Vci or VREG pin input voltage).

Table 18 VR Bits and V1REF Voltage

VR2	VR1	VR0	V1REF Voltage Setting
0	0	0	Vreg x six-times
0	0	1	Vreg x seven-times
0	1	0	Vreg x eight-times
0	1	1	Vreg x nine-times
1	0	0	Vreg x ten-times
1	0	1	Vreg x 11-times
1	1	0	Vreg x 12-times
1	1	1	Vreg x 13-times

Entry Mode (R05h)

Compare Register (R06h)

The write data sent from the microcomputer is modified in the HD66761 and written to the GRAM. The display data in the GRAM can be quickly rewritten to reduce the load of the microcomputer software processing. For details, see the Graphics Operation Function section.

SWP: When SWP = 1, the upper and lower bytes in the two-byte data sent from the microcomputer are swapped and written to the GRAM. When SWP = 0, this bit directly writes the two-byte data sent from the microcomputer to the GRAM. This swap processing is performed only for the data sent from the microcomputer before logical operation. When SWP = 1, the upper and lower bytes in the write data mask (WM15–0) are swapped to be executed with the write data.

I/D: When I/D = 1, the address counter (AC) is automatically incremented by 1 after the data is written to the GRAM. When I/D = 0, the AC is automatically decremented by 1 after the data is written to the GRAM.

AM: Set the automatic update method of the AC after the data is written to the GRAM. When AM = 0, the data is continuously written in parallel. When AM = 1, the data is continuously written vertically.

LG2–0: Compare the data read from the GRAM by the microcomputer with the compare registers (CP7–0) by a compare/logical operation and write the results to GRAM. For details, see the Logical/Compare Operation Function.

CP7–0: Set the compare register for the compare operation with the data read from the GRAM or written by the microcomputer.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	0	0	SWP	0	0	0	I/D	AM	LG2	LG1	LG0
W	1	0	0	0	0	0	0	0	0	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0

Figure 9 Entry Mode and Compare Register

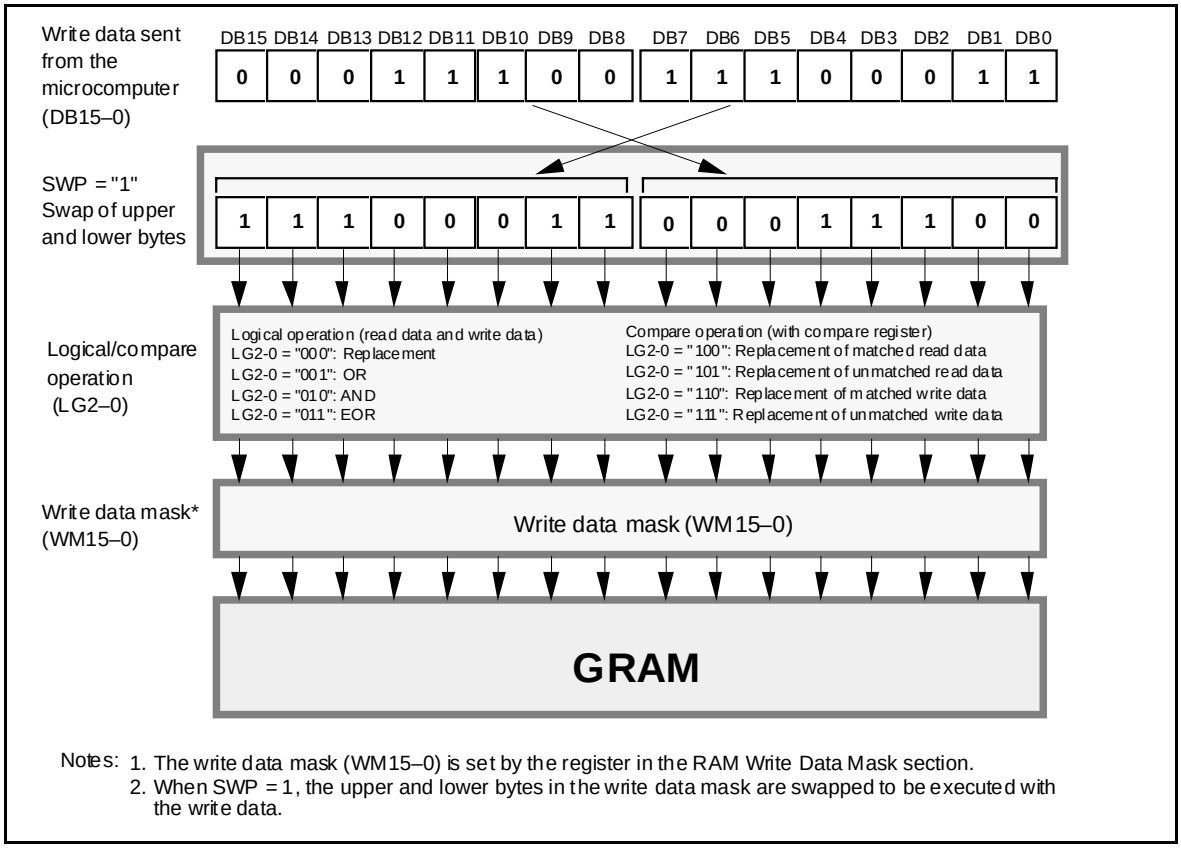


Figure 10 Logical/Compare Operation and Swapping for the GRAM

Display Control (R07h)

VLE2–1: When VLE1 = 1, a vertical scroll is performed in the 1st screen. When VLE2 = 1, a vertical scroll is performed in the 2nd screen. Vertical scrolling on the two screens can be independently controlled.

SPT: When SPT = 1, the 2-division LCD drive is performed. For details, see the Screen-division Driving Function section.

GS: When GS = 0, the display is in eight grayscale mode and displays 256 colors by selecting eight grayscales from 16 grayscale levels. When GS = 1, the display is in four grayscales and displays 256 colors by selecting four grayscales from 16 grayscale levels. In four-grayscale mode, four colors can be displayed with two bits per pixel (RGB). GRAM data must be rewritten when the GS bit is swapped.

When GS = 1, the GRAM address increments or decrements addresses from 0000H to 4F0FH. For details, see the Grayscale Palette and Four-color Display Mode sections.

REV: Displays all character and graphics display sections with reversal when REV = 1. For details, see the Reversed Display Function section. Since the grayscale level can be reversed, display of the same data is enabled on normally-white and normally-black panels.

D1–0: Display is on when D1 = 1 and off when D1 = 0. When off, the display data remains in the GRAM, and can be displayed instantly by setting D1 = 1. When D1 is 0, the display is off with the SEG1 to SEG384 outputs and COM1 to COM80 outputs set to the GND level. Because of this, the HD66761

can control the charging current for the LCD with AC driving.

When D1–0 = 01, the internal display of the HD66761 is performed although the display is off. When D1-0 = 00, the internal display operation halts and the display is off.

Table 19 D Bits and Operation

D1	D0	SEG/COM Output	HD66761 Internal Display Operation	Master/Slave Signal (OSC, CL1, FLM, and M)
0	0	GND	Halt	Halt
0	1	GND	Operate	Operate
1	0	Unlit display	Operate	Operate
1	1	Display	Operate	Operate

Notes: 1. The internal power supply can operate independently from D1–0.
2. Writing from the microcomputer to the GRAM is independent from D1–0.
3. In the sleep and standby modes, D1–0 = 00. However, the register contents of D1–0 are not modified.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	VLE2	VLE1	SPT	0	0	0	0	GS	REV	D1	D0

Figure 11 Display Control Instruction

Cursor Control (R08h)

C: When C = 1, the window cursor display is started. The display mode is selected by the CM1–0 bits, and the display area is specified in a pixel unit by the horizontal cursor position register (HS6–0 and HE6–0 bits) and vertical cursor position register (VS6–0 and VE6–0 bits). The cursor color (CR, CG, or CB) can be set to any of eight colors in the window cursor. However, the cursor color cannot be controlled by the grayscale. For details, see the Color Window Cursor Control section.

CM1–0: The display mode of the window cursor is selected. These bits can display a eight-color cursor, reversed cursor, eight-color blink cursor, and reversed blink cursor.

CR/CB/CG: The window cursor color can be specified. Red, blue, green, white, black, or any combination color can be displayed. However, the cursor color cannot be controlled by the grayscale. For details, see the Color Window Cursor Control section.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	CR	CG	CB	0	0	0	C	0	0	CM1	CM0

Figure 12 Cursor Control Instruction

Table 20 CM Bits and Window Cursor Display Mode

CM1	CM0	Window Cursor Display Mode
0	0	Eight-color cursor (displaying the window cursor with the color specified by CR, CG, or CB)
0	1	Reversed cursor (displaying reversed grayscale data in the window cursor)
1	0	Eight-color blink cursor (alternately blinking normal and eight-color display of CR, CG, or CB in the window cursor)
1	1	Reversed blink cursor (alternately blinking normal and reversed display of the grayscale data in the window cursor)

Grayscale and Blink Synchronization (R09h)

Initializes the blink and frame counters, which control the blink cycle and grayscale generation, respectively. During master/slave operation, blinking between master and slave and synchronization of the grayscale generation cycle are needed. Synchronize the cycle after reading the status and determining the display-read raster-row.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Figure 13 Grayscale and Blink Synchronization Instructions

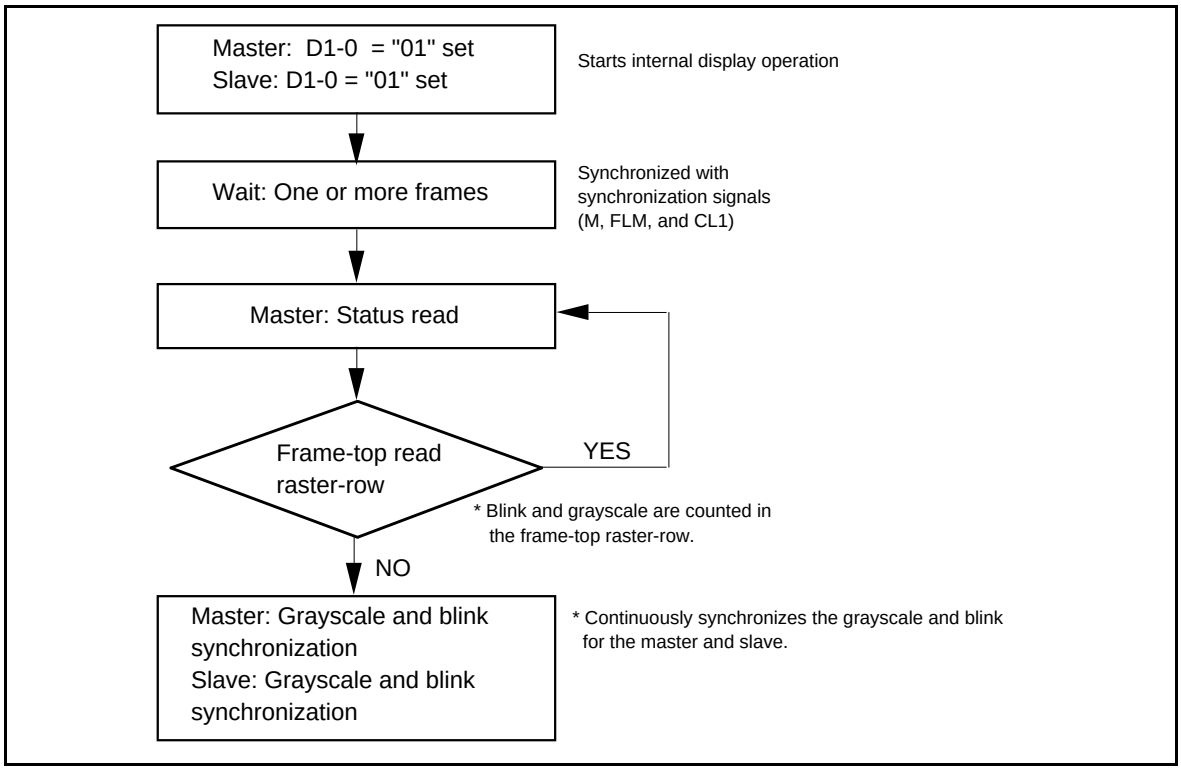


Figure 14 Grayscale and Blink Synchronization

Horizontal Scroll Control (R10h)

HL4–0: Specify the amount of horizontal scroll. The horizontal scroll is performed to the left in four-pixel (RGB) units. After the 128th pixel is displayed, one pixel is displayed. On a divided-screen display, both screens are scrolled.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**HL4**	**HL3**	**HL2**	**HL1**	**HL0**

Figure 15 Horizontal Scroll Control Instructions

Table 21 HL Bits and Horizontal Scroll

HL4	HL3	HL2	HL1	HL0	Amount of Horizontal Scroll
0	0	0	0	0	Display from 1st pixel (no scroll)
0	0	0	0	1	Display from 5th pixel
0	0	0	1	0	Display from 9th pixel
0	0	0	1	1	Display from 13th pixel
0	0	1	0	0	Display from 17th pixel
		:			:
0	0	1	1	0	Display from 121st pixel
1	1	1	1	1	Display from 125th pixel

Vertical Scroll Control (R11h)

VL16–10: Specify the display-start raster-row at the 1st screen display for vertical smooth scrolling. Any raster-row from the first to 80th can be selected. After the 80th raster-row is displayed, the display restarts from the first raster-row. The display-start raster-row (VL16–10) is valid only when VLE1 = 1. The raster-row display is fixed when VLE1 = 0. (VLE1 is the 1st-screen vertical-scroll enable bit.)

VL26–20: Specify the display-start raster-row at the 2nd screen display. The display-start raster-row (VL26–20) is valid only when VLE2 = 1. The raster-row display is fixed when VLE2 = 0. (VLE2 is the 2nd-screen vertical-scroll enable bit.) The vertical scroll for the 1st and 2nd screens can be independently set.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	**1**	**0**	**VL 26**	**VL 25**	**VL 24**	**VL 23**	**VL 22**	**VL 21**	**VL 20**	**0**	**VL 16**	**VL 15**	**VL 14**	**VL 13**	**VL 12**	**VL 11**	**VL 10**

Figure 16 Vertical Scroll Control Instruction

Table 22 VL Bits and Display-start Raster-row

VL26 VL16	VL25 VL15	VL24 VL14	VL23 VL13	VL22 VL12	VL21 VL11	VL20 VL10	Display-start Raster-row
0	0	0	0	0	0	0	1st raster-row
0	0	0	0	0	0	1	2nd raster-row
0	0	0	0	0	1	0	3rd raster-row
0	0	0	0	0	1	1	4th raster-row
0	0	0	0	1	0	0	5th raster-row
:	:	:	:	:	:	:	:
1	0	0	1	1	1	0	79th raster-row
1	0	0	1	1	1	1	80th raster-row

Note: Do not set over the 80th (4FH) raster-row.

Horizontal Cursor Position (R12h)

Vertical Cursor Position (R13h)

HS6–0: Specify the start position for horizontally displaying the window cursor in a pixel unit. The cursor is displayed from the 'set value + 1' pixel. Ensure that HS6–0 ≤ HE6–0.

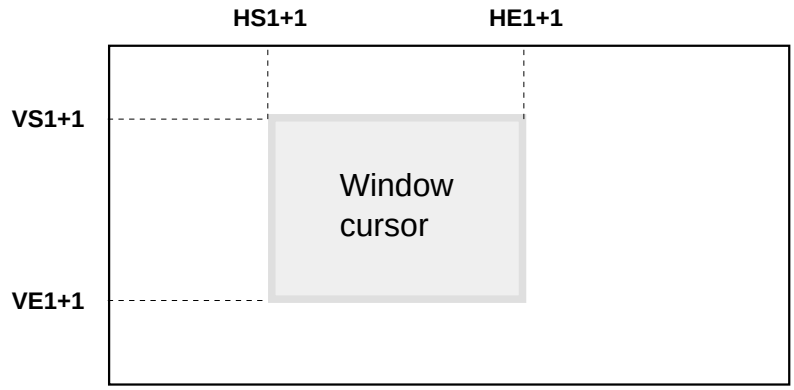
HE6–0: Specify the end position for horizontally displaying the window cursor in a pixel unit. The cursor is displayed to the 'set value + 1' pixel. Ensure that HS6–0 ≤ HE6–0.

VS6–0: Specify the start position for vertically displaying the window cursor in a raster-row unit. The cursor is displayed from the 'set value + 1' raster-row. Ensure that VS6–0 ≤ VE6–0.

VE6–0: Specify the end position for vertically displaying the window cursor in a raster-row unit. The cursor is displayed to the 'set value + 1' raster-row. Ensure that VS6–0 ≤ VE6–0.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	**1**	**0**	**HE6**	**HE5**	**HE4**	**HE3**	**HE2**	**HE1**	**HE0**	**0**	**HS6**	**HS5**	**HS4**	**HS3**	**HS2**	**HS1**	**HS0**
W	**1**	**0**	**VE6**	**VE5**	**VE4**	**VE3**	**VE2**	**VE1**	**VE0**	**0**	**VS6**	**VS5**	**VS4**	**VS3**	**VS2**	**VS1**	**VS0**

Figure 17 Horizontal Cursor Position and Vertical Cursor Position Instructions



Note: The cursor position must be included in the display area.

Figure 18 Window Cursor Position

1st Screen Driving Position (R14h)

2nd Screen Driving Position (R15h)

SS16–0: Specify the driving start position for the first screen in a line unit. The LCD driving starts from the 'set value + 1' common driver.

SE16–0: Specify the driving end position for the first screen in a line unit. The LCD driving is performed to the 'set value + 1' common driver. For instance, when SS16–10 = 07H and SE16–10 = 10H are set, the LCD driving is performed from COM8 to COM17, and non-selection driving is performed for COM1 to COM7, COM18, and others. Ensure that SS16–10 ≤ SE16–10 ≤ 4FH. For details, see the Screen-division Driving Function section.

SS26–0: Specify the driving start position for the second screen in a line unit. The LCD driving starts from the 'set value + 1' common driver. The second screen is driven when SPT = 1.

SE26–0: Specify the driving end position for the second screen in a line unit. The LCD driving is performed to the 'set value + 1' common driver. For instance, when SPT = 1, SS26–20 = 20H, and SE26–20 = 4FH are set, the LCD driving is performed from COM33 to COM80. Ensure that SS16–10 ≤ SE16–10 < SS26–20 ≤ SE26–20 ≤ 4FH. For details, see the Screen-division Driving Function section.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	SE16	SE15	SE14	SE13	SE12	SE11	SE10	0	SS16	SS15	SS14	SS13	SS12	SS11	SS10
W	1	0	SE26	SE25	SE24	SE23	SE22	SE21	SE20	0	SS26	SS25	SS24	SS23	SS22	SS21	SS20

Figure 19 1st Screen Driving Position and 2nd Screen Driving Position

RAM Write Data Mask (R20h)

WM15–0: In writing to the GRAM, these bits mask writing in a bit unit. When WM15 = 1, this bit masks the write data of DB15 and does not write to the GRAM. Similarly, the WM14–0 bits mask the write data of DB14–0 in a bit unit. When SWP = 1, the upper and lower bytes in the write data mask are swapped. For details, see the Graphics Operation Function section.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0

Figure 20 RAM Write Data Mask Instruction

RAM Address Set (R21h)

AD14–0: Initially set GRAM addresses to the address counter (AC). Once the GRAM data is written, the AC is automatically updated according to the AM and I/D bit settings. This allows consecutive accesses without resetting addresses. Once the GRAM data is read, the AC is not automatically updated. In four-color mode (GS = 1), the address for GRAM write is automatically updated from 0000H to 4F0FH. GRAM address setting is not allowed in the sleep mode or standby mode.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	AD14	AD13	AD12	AD11	AD10	AD9	AD8	0	0	AD5	AD4	AD3	AD2	AD1	AD0

Figure 21 RAM Address Set Instruction

Table 23 GRAM Address Range in Eight-grayscale Mode (GS = 0)

AD14–AD0	GRAM Setting
"0000"H–"003F"H	Bitmap data for COM1
"0100"H–"013F"H	Bitmap data for COM2
"0200"H–"023F"H	Bitmap data for COM3
"0300"H–"033F"H	Bitmap data for COM4
:	:
"4C00"H–"4C3F"H	Bitmap data for COM77
"4D00"H–"4D3F"H	Bitmap data for COM78
"4E00"H–"4E3F"H	Bitmap data for COM79
"4F00"H–"4F3F"H	Bitmap data for COM80

Table 24 GRAM Address Range in Four-grayscale Mode (GS = 1)

AD14–AD0	GRAM Setting
"0000"H–"000F"H	Bitmap data for COM1
"0100"H–"010F"H	Bitmap data for COM2
"0200"H–"020F"H	Bitmap data for COM3
"0300"H–"030F"H	Bitmap data for COM4
:	:
"4C00"H–"4C0F"H	Bitmap data for COM77
"4D00"H–"4D0F"H	Bitmap data for COM78
"4E00"H–"4E0F"H	Bitmap data for COM79
"4F00"H–"4F0F"H	Bitmap data for COM80

Write Data to GRAM (R22h)

WD15–0 : Write 16-bit data to the GRAM. This data calls each grayscale palette. After a write, the address is automatically updated according to the AM and I/D bit settings. During the sleep and standby modes, the GRAM cannot be accessed.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	WD 15	WD 14	WD 13	WD 12	WD 11	WD 10	WD 9	WD 8	WD 7	WD 6	WD 5	WD 4	WD 3	WD 2	WD 1	WD 0

Figure 22 Write Data to GRAM Instruction

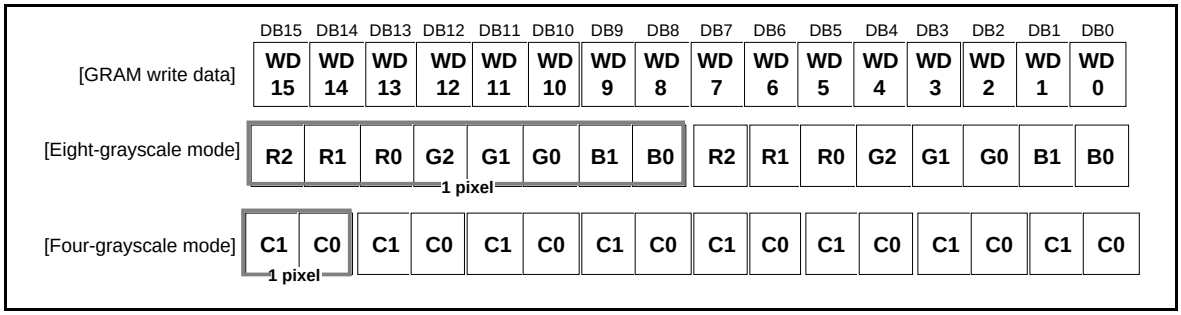


Figure 23 GRAM Write Data

Table 25 GRAM Data and R Grayscale Palette in the Eight-grayscale Mode (GS = 0)

GRAM Data Setting						
R2	**R1**	**R0**	**<R> Grayscale Palette**			
0	0	0	RK03	RK02	RK01	RK00
0	0	1	RK13	RK12	RK11	RK10
0	1	0	RK23	RK22	RK21	RK20
0	1	1	RK33	RK32	RK31	RK30
1	0	0	RK43	RK42	RK41	RK40
1	0	1	RK53	RK52	RK51	RK50
1	1	0	RK63	RK62	RK61	RK60
1	1	1	RK73	RK72	RK71	RK70

Table 26 GRAM Data and G Grayscale Palette in the Eight-grayscale Mode (GS = 0)

GRAM Data Setting						
G2	**G1**	**G0**	**<G> Grayscale Palette**			
0	0	0	GK03	GK02	GK01	GK00
0	0	1	GK13	GK12	GK11	GK10
0	1	0	GK23	GK22	GK21	GK20
0	1	1	GK33	GK32	GK31	GK30
1	0	0	GK43	GK42	GK41	GK40
1	0	1	GK53	GK52	GK51	GK50
1	1	0	GK63	GK62	GK61	GK60
1	1	1	GK73	GK72	GK71	GK70

Table 27 GRAM Data and B Grayscale Palette in the Eight-grayscale Mode (GS = 0)

GRAM Data Setting					
B1	**B0**	**<B> Grayscale Palette**			
0	0	BK03	BK02	BK01	BK00
0	1	BK13	BK12	BK11	BK10
1	0	BK23	BK22	BK21	BK20
1	1	BK33	BK32	BK31	BK30

Table 28 GRAM Data and Grayscale Palette in the Four-grayscale Mode (GS = 1)

GRAM Data Setting													
C1	**C0**	**<R> Grayscale Palette**				**<G> Grayscale Palette**				**<B> Grayscale Palette**			
0	0	RK03	RK02	RK01	RK00	GK03	GK02	GK01	GK00	BK03	BK02	BK01	BK00
0	1	RK13	RK12	RK11	RK10	GK13	GK12	GK11	GK10	BK13	BK12	BK11	BK10
1	0	RK23	RK22	RK21	RK20	GK23	GK22	GK21	GK20	BK23	BK22	BK21	BK20
1	1	RK33	RK32	RK31	RK30	GK33	GK32	GK31	GK30	BK33	BK32	BK31	BK30

Read Data from GRAM (R22h)

RD15–0 : Read 16-bit data from the GRAM. When the data is read to the microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (DB15–0) becomes invalid and the second-word read is normal.

When bit processing, such as a logical operation, is performed within the HD66761, only one read can be processed since the latched data in the first word is used.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R	**1**	**RD 15**	**RD 14**	**RD 13**	**RD 12**	**RD 11**	**RD 10**	**RD 9**	**RD 8**	**RD 7**	**RD 6**	**RD 5**	**RD 4**	**RD 3**	**RD 2**	**RD 1**	**RD 0**

Figure 24 Read Data from GRAM Instruction

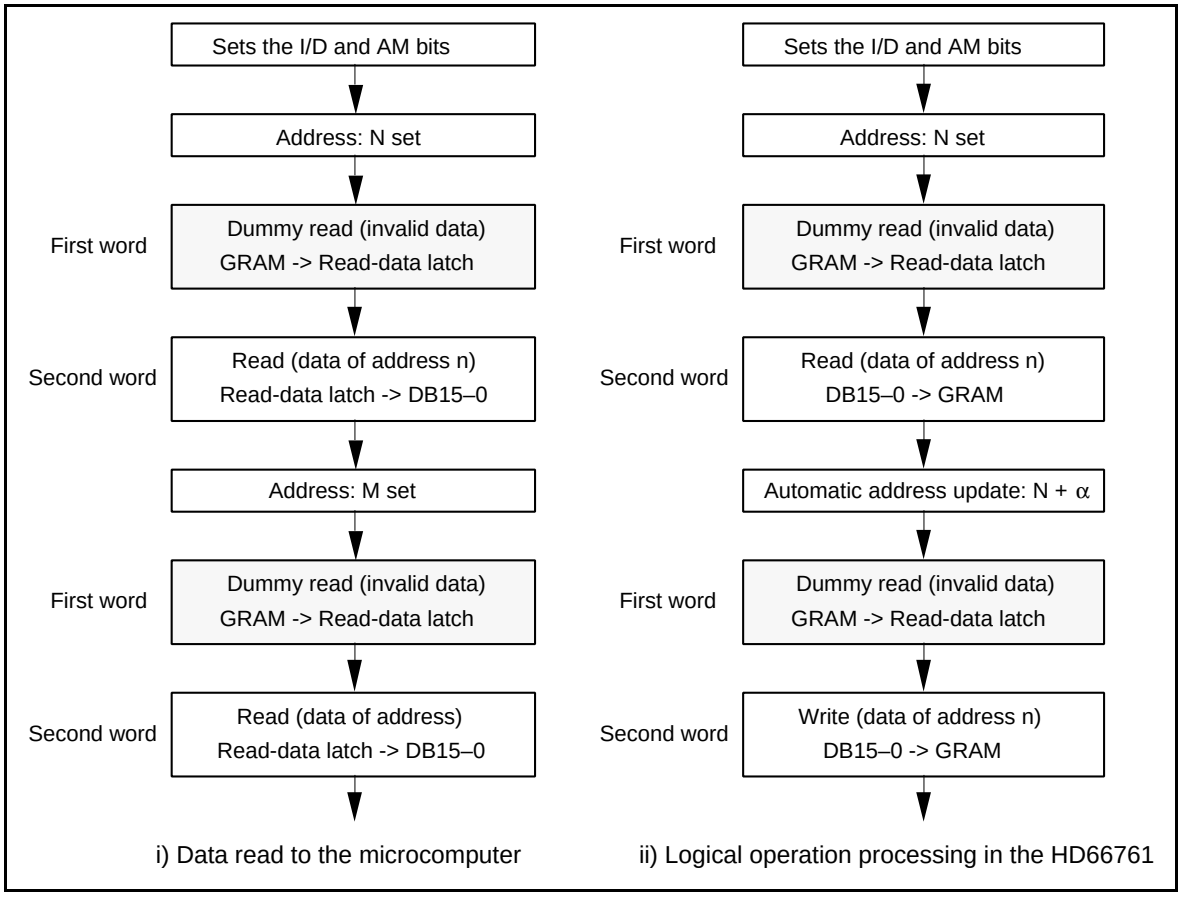


Figure 25 GRAM Read Sequence

Grayscale Palette Control (R30h to R39h)

RK73–00 : Specify the R-grayscale level for eight palettes from the 16-grayscale level. For details, see the Grayscale Palette and Grayscale Palette Table sections.

In four-grayscale display mode, the number of palettes to be used is four. For details, see the Four-grayscale Display Mode section.

GK73–00 : Specify the G-grayscale level for eight palettes from the 16-grayscale level. For details, see the Grayscale Palette and Grayscale Palette Table sections.

In four-grayscale display mode, the number of palettes to be used is four. For details, see the Four-grayscale Display Mode section.

BK33–00 : Specify the B-grayscale level for four palettes from the 16-grayscale level. For details, see the Grayscale Palette and Grayscale Palette Table sections.

In four-grayscale display mode, the number of palettes to be used is four. For details, see the Four-grayscale Display Mode section.

	R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R30	W	1	0	0	0	0	RK 13	RK 12	RK 11	RK 10	0	0	0	0	RK 03	RK 02	RK 01	RK 00
R31	W	1	0	0	0	0	RK 33	RK 32	RK 31	RK 30	0	0	0	0	RK 23	RK 22	RK 21	RK 20
R32	W	1	0	0	0	0	RK 53	RK 52	RK 51	RK 50	0	0	0	0	RK 43	RK 42	RK 41	RK 40
R33	W	1	0	0	0	0	RK 73	RK 72	RK 71	RK 70	0	0	0	0	RK 63	RK 62	RK 61	RK 60
R34	W	1	0	0	0	0	GK 13	GK 12	GK 11	GK 10	0	0	0	0	GK 03	GK 02	GK 01	GK 00
R35	W	1	0	0	0	0	GK 33	GK 32	GK 31	GK 30	0	0	0	0	GK 23	GK 22	GK 21	GK 20
R36	W	1	0	0	0	0	GK 53	GK 52	GK 51	GK 50	0	0	0	0	GK 43	GK 42	GK 41	GK 40
R37	W	1	0	0	0	0	GK 73	GK 72	GK 71	GK 70	0	0	0	0	GK 63	GK 62	GK 61	GK 60
R38	W	1	0	0	0	0	BK 13	BK 12	BK 11	BK 10	0	0	0	0	BK 03	BK 02	BK 01	BK 00
R39	W	1	0	0	0	0	BK 33	BK 32	BK 31	BK 30	0	0	0	0	BK 23	BK 22	BK 21	BK 20

Figure 26 Grayscale Palette Control Instruction

Test Register (R40h to R44h)

Index registers R40h–R44h cannot be used or set since they are test registers. Do not change the contents of the instruction bits in these registers.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	Test register															

Figure 27 Test Register Instruction

Table 29 Instruction List

Reg. No.	Register Name	R/W	RS	Upper Code DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	Lower Code DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Cycle
IR	Index	0	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0	Sets the index register value.	0
SR	Status read	1	0	0	L6	L5	L4	L3	L2	L1	L0	0	C6	C5	C4	C3	C2	C1	C0	Reads the driving raster-row position (L7-0) and contrast setting (C6-0).	0
R00h	Start oscillation	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	Starts the oscillation mode.	10 ms
	Device code read	1	1	M/S	0	0	0	0	1	1	1	0	1	1	0	0	0	0	1	Reads *761H and master/slave setting (M/S).	0
R01h	Driver output control	0	1	0	0	0	0	0	0	CMS	SGS	0	0	0	0	NL3	NL2	NL1	NL0	Sets the common driver shift direction (CMS), segment driver shift direction (SGS), and driving duty ratio (NL3-0).	0
R02h	LCD-driving-waveform control	0	1	0	0	0	0	0	0	0	0	0	B/C	EOR	NW4	NW3	NW2	NW1	NW0	Sets the LCD drive AC waveform (B/C), EOR output (EOR), and the number of n-raster-rows (NW4-0) at C-pattern AC drive.	0
R03h	Power control	0	1	0	0	0	BS2	BS1	BS0	BT1	BT0	PS1	PS0	DC1	DC0	AP1	AP0	SLP	STB	Sets the sleep mode (SLP), standby mode (STB), LCD power on (AP1-0), boosting cycle (DC1-0), reference power-supply setting (PS1-0), boosting ouput multiplying factor (BT1-0), and LCD drive bias value (BS2-0).	0
R04h	Contrast control	0	1	0	0	0	0	0	VR2	VR1	VR0	0	CT6	CT5	CT4	CT3	CT2	CT1	CT0	Sets the contrast adjustment (CT6-0) and regulator adjustment (VR2-0).	0
R05h	Entry mode	0	1	0	0	0	0	0	0	0	SWP	0	0	0	I/D	AM	LG2	LG1	LG0	Specifies the logical operation (LG2-0), AC counter mode (AM), increment/decrement mode (I/D), and swap (SWP).	0
R06h	Compare register	0	1	0	0	0	0	0	0	0	0	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0	Sets the compare register (CP7-0).	0
R07h	Display control	0	1	0	0	0	0	0	VLE2	VLE1	SPT	0	0	0	0	GS	REV	D1	D0	Specifies display on (D1-0), reversed display (REV), 4-/16-grayscale mode (GS), 4-grayscale display page (PG1-0), screen division driving (SPT), and vertical scroll (VLE2-1).	0
R08h	Cursor control	0	1	0	0	0	0	0	CR	CG	CB	0	0	0	C	0	0	CM1	CM0	Specifies cursor display on (C), cursor display mode (CM1-0), and cursor color (CR, CG, or CB).	
R09h	Grayscale and blink synchronization	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Synchronizes the grayscale with the blink cycle.	0
R10h	Horizontal scroll control	0	1	0	0	0	0	0	0	0	0	0	0	0	HL4	HL3	HL2	HL1	HL0	Specifies the amount of horizontal scrolling (HL4-0).	0
R11h	Vertical scroll control	0	1	0	VL26	VL25	VL24	VL23	VL22	VL21	VL20	0	VL16	VL15	VL14	VL13	VL12	VL11	VL10	Specifies the 1st-screen display-start raster-row (VL16-10) and 2nd-screen display-start raster-row (VL26-20).	0
R12h	Horizontal cursor position	0	1	0	HE6	HE5	HE4	HE3	HE2	HE1	HE0	0	HS6	HS5	HS4	HS3	HS2	HS1	HS0	Sets horizontal cursor start (HS6-0) and end (HE6-0).	0
R13h	Vertical cursor position	0	1	0	VE6	VE5	VE4	VE3	VE2	VE1	VE0	0	VS6	VS5	VS4	VS3	VS2	VS1	VS0	Sets vertical cursor start (VS6-0) and end (VE6-0).	0
R14h	1st screen driving position	0	1	0	SE16	SE15	SE14	SE13	SE12	SE11	SE10	0	SS16	SS15	SS14	SS13	SS12	SS11	SS10	Sets 1st-screen driving start (SS16-10) and end (SE16-10).	0
R15h	2nd screen driving position	0	1	0	SE26	SE25	SE24	SE23	SE22	SE21	SE20	0	SS26	SS25	SS24	SS23	SS22	SS21	SS20	Sets 2nd-screen driving start (SS26-20) and end (SE26-20).	0
R20h	RAM write data mask	0	1	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0	Specifies write data mask (WM15-0) at RAM write.	0
R21h	RAM address set	0	1	0	AD14-8 (upper)							0	0	AD6-0 (lower)						Initially sets the RAM address to the address counter (AC).	0
R22h	Write data to GRAM	0	1	Write Data (upper)								Write Data (lower)								Writes data to the RAM.	0
	Write data from GRAM	1	1	Read Data (upper)								Read Data (lower)								Reads data from the RAM.	0
R30h	R-grayscale palette control (1)	0	1	0	0	0	0	RK13	RK12	RK11	RK10	0	0	0	0	RK03	RK02	RK01	RK00	Specifies the R-grayscale palette.	0
R31h	R-grayscale palette control (2)	0	1	0	0	0	0	RK33	RK32	RK31	RK30	0	0	0	0	RK23	RK22	RK21	RK20	Specifies the R-grayscale palette.	0
R32h	R-grayscale palette control (3)	0	1	0	0	0	0	RK53	RK52	RK51	RK50	0	0	0	0	RK43	RK42	RK41	RK40	Specifies the R-grayscale palette.	0
R33h	R-grayscale palette control (4)	0	1	0	0	0	0	RK73	RK72	RK71	RK70	0	0	0	0	RK63	RK62	RK61	RK60	Specifies the R-grayscale palette.	0
R34h	G-grayscale palette control (1)	0	1	0	0	0	0	GK13	GK12	GK11	GK10	0	0	0	0	GK03	GK02	GK01	GK00	Specifies the G-grayscale palette.	0
R35h	G-grayscale palette control (2)	0	1	0	0	0	0	GK33	GK32	GK31	GK30	0	0	0	0	GK23	GK22	GK21	GK20	Specifies the G-grayscale palette.	0
R36h	G-grayscale palette control (3)	0	1	0	0	0	0	GK53	GK52	GK51	GK50	0	0	0	0	GK43	GK42	GK41	GK40	Specifies the G-grayscale palette.	0
R37h	G-grayscale palette control (4)	0	1	0	0	0	0	GK73	GK72	GK71	GK70	0	0	0	0	GK63	GK62	GK61	GK60	Specifies the G-grayscale palette.	0
R38h	B-grayscale palette control (1)	0	1	0	0	0	0	BK13	BK12	BK11	BK10	0	0	0	0	BK03	BK02	BK01	BK00	Specifies the B-grayscale palette.	0
R39h	B-grayscale palette control (2)	0	1	0	0	0	0	BK33	BK32	BK31	BK30	0	0	0	0	BK23	BK22	BK21	BK20	Specifies the B-grayscale palette.	0
R40h	Test register (1)	0	1	Test register (disabled)																Disables the use or setting of this register since this is the test register.	0
R41h	Test register (2)	0	1	Test register (disabled)																Disables the use or setting of this register since this is the test register.	0
R42h	Test register (3)	0	1	Test register (disabled)																Disables the use or setting of this register since this is the test register.	0
R43h	Test register (4)	0	1	Test register (disabled)																Disables the use or setting of this register since this is the test register.	0
R44h	Test register (5)	0	1	Test register (disabled)																Disables the use or setting of this register since this is the test register.	0

Note: '*' means 'doesn't matter'.

Reset Function

The HD66761 is internally initialized by RESET input. Because the busy flag (BF) indicates a busy state (BF = 1) during the reset period, no instruction or GRAM data access from the MPU is accepted. The reset input must be held for at least 1 ms. Do not access the GRAM or initially set the instructions until the R-C oscillation frequency is stable after power has been supplied (10 ms).

Instruction Set Initialization:

1. Start oscillation executed
2. Driver output control (NL3–0 = 1001, SGS = 0, CMS = 0)
3. B-pattern waveform AC drive (B/C = 0, ECR = 0, NW4–0 = 00000)
4. Power control (PS1–0 = 00, DC1–0 = 00, AP1–0 = 00: LCD power off, SLP = 0: Sleep mode off, STB = 0: Standby mode off)
5. 1/10 bias drive (BS2–0 = 001), Four-times step-up (BT1–0 = 00), Weak contrast (CT6–0 = 0000000)
6. Entry mode set (SWP = 0, I/D = 1: Increment by 1, AM = 0: Horizontal move, LG2–0 = 000: Replace mode)
7. Compare register (CP7–0: 00000000)
8. Display control (VLE2–1 = 00: No vertical scroll, SPT = 0, GS = 0: Eight-grayscale mode, REV = 0, D1–0 = 00: Display off)
9. Cursor control (CR/CG/CB = 000, C = 0: Cursor display off, CM1–0 = 00)
10. Horizontal scroll (HL4–0 = 00000)
11. Vertical scroll (VL26–20 = 000000, VL16–10 = 000000)
12. Window cursor display position (HS6–0 = HE6–0 = VS6–0 = VE6–0 = 00000000)
13. 1st screen division (DS16–10 = 00000000, DE16–10 = 11111111)
14. 2nd screen division (DS26–20 = 00000000, DE26–20 = 11111111)
15. RAM write data mask (WM15–0 = 0000H: No mask)
16. RAM address set (AD14–0 = 0000H)
17. Grayscale palette
    (RK03–00 = 0000, RK13–10 = 0011, RK23–20 = 0101, RK33–30 = 0111,
    RK43–40 = 1001, RK53–50 = 1011, RK63–60 = 1101, RK73–70 = 1111,
    GK03–00 = 0000, GK13–10 = 0011, GK23–20 = 0101, GK33–30 = 0111,
    GK43–40 = 1001, GK53–50 = 1011, GK63–60 = 1101, GK73–70 = 1111,
    BK03–00 = 0000, BK23–20 = 0101, BK43–40 = 1001, BK63–60 = 1111)

GRAM Data Initialization:

This is not automatically initialized by reset input but must be initialized by software while display is off (D1–0 = 00).

Output Pin Initialization:

1. LCD driver output pins (SEG/COM): Output GND level
2. Step-up circuit output pin (VLOUT): Outputs Vcc level
3. Oscillator output pin (OSC2): Outputs oscillation signal
4. Master/slave signals (CL1, CL2, M, and FLM): Halt

Parallel Data Transfer

16-bit Bus Interface

Setting the IM1/0 (interface mode) to the GND/GND level allows 68-system E-clock-synchronized 16-bit parallel data transfer. Setting the IM1/0 to the Vcc/GND level allows 80-system 16-bit parallel data transfer. When the number of buses or the mounting area is limited, use an 8-bit bus interface.

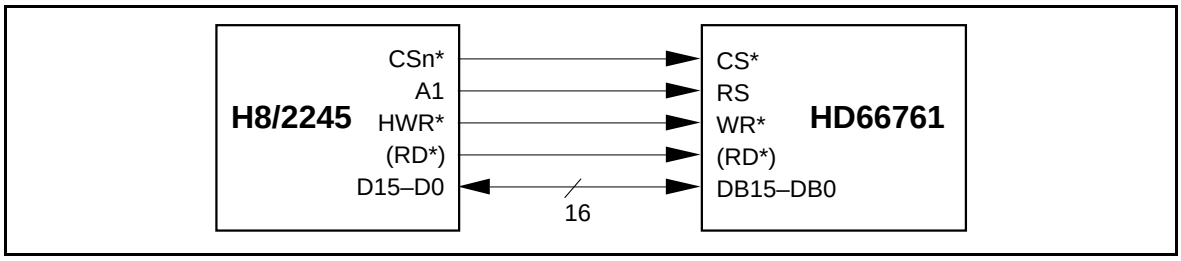


Figure 28 Interface to 16-bit Microcomputer

8-bit Bus Interface

Setting the IM1/0 (interface mode) to the GND/Vcc level allows 68-system E-clock-synchronized 8-bit parallel data transfer using pins DB15–DB8. Setting the IM1/0 to the Vcc/Vcc level allows 80-system 8-bit parallel data transfer. The 16-bit instructions and RAM data are divided into eight upper/lower bits and the transfer starts from the upper eight bits. Fix unused pins DB7–DB0 to the Vcc or GND level. Note that the upper bytes must also be written when the index register is written to.

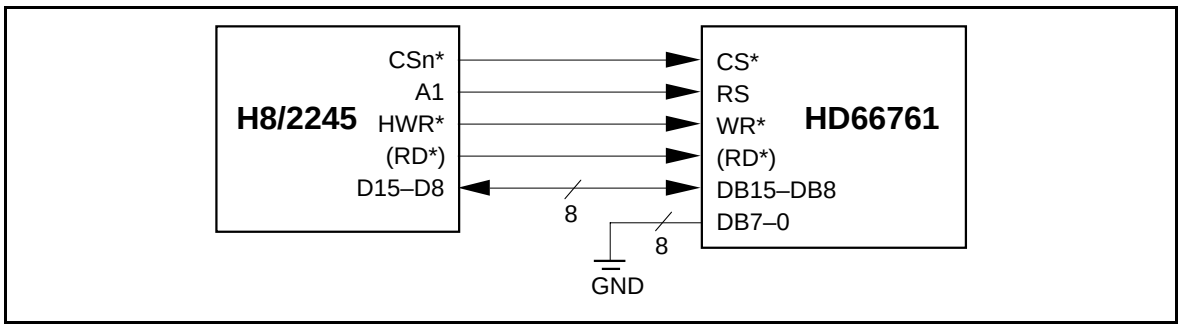


Figure 29 Interface to 8-bit Microcomputer

Note: Transfer synchronization function for an 8-bit bus interface
The HD66761 supports the transfer synchronization function which resets the upper/lower counter to count upper/lower 8-bit data transfer in the 8-bit bus interface. Noise causing transfer mismatch between the eight upper and lower bits can be corrected by a reset triggered by consecutively writing a 00H instruction four times. The next transfer starts from the upper eight bits. Executing synchronization function periodically can recover any runaway in the display system.

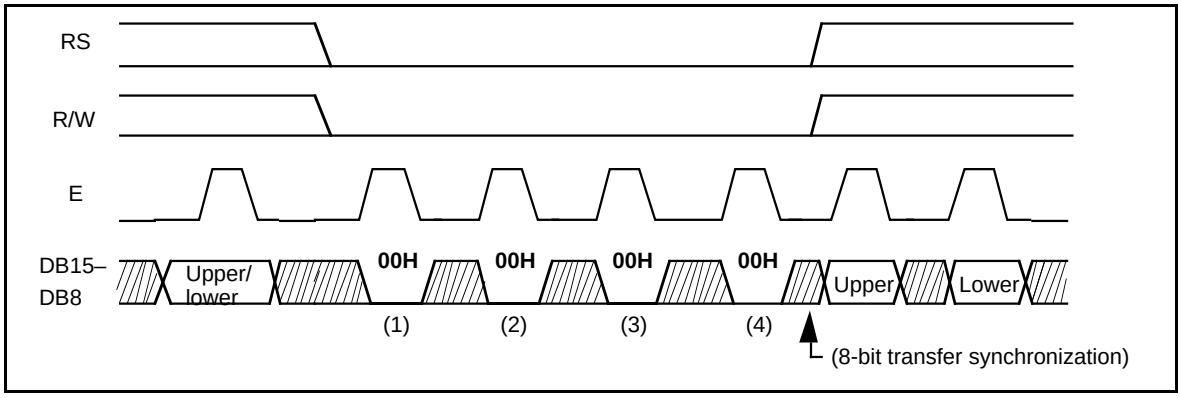


Figure 30 8-bit Transfer Synchronization

Graphics Operation Function

The HD66761 can greatly reduce the load of the microcomputer graphics software processing through the 16-bit bus architecture and internal graphics-bit operation function. This function supports the following:

1. A swap function that exchanges the upper and lower bytes in the 16-bit data sent from the microcomputer.
2. A write data mask function that selectively rewrites some of the bits in the 16-bit write data.
3. A logical operation write function that writes the data sent from the microcomputer and the original RAM data by a logical operation.
4. A conditional write function that compares the original RAM data or write data and the compare-bit data and writes the data sent from the microcomputer only when the conditions match.

Even if the display size is large, the display data in the graphics RAM (GRAM) can be quickly rewritten.

The graphics bit operation can be controlled by combining the entry mode register, the bit set value of the RAM-write-data mask register, and the read/write from the microcomputer.

Table 30 Graphics Operation

	Bit Setting			
Operation Mode	**I/D**	**AM**	**LG2–0**	**Operation and Usage**
Write mode 1	0/1	0	000	Horizontal data replacement, horizontal-border drawing
Write mode 2	0/1	1	000	Vertical data replacement, vertical-border drawing
Write mode 3	0/1	0	110 111	Conditional horizontal data replacement, horizontal-border drawing
Write mode 4	0/1	1	110 111	Conditional vertical data replacement, vertical-border drawing
Read/write mode 1	0/1	0	001 010 011	Horizontal data write with logical operation, horizontal-border drawing
Read/write mode 2	0/1	1	001 010 011	Vertical data write with logical operation, vertical-border drawing
Read/write mode 3	0/1	0	100 101	Conditional horizontal data replacement, horizontal-border drawing
Read/write mode 4	0/1	1	100 101	Conditional vertical data replacement, vertical-border drawing

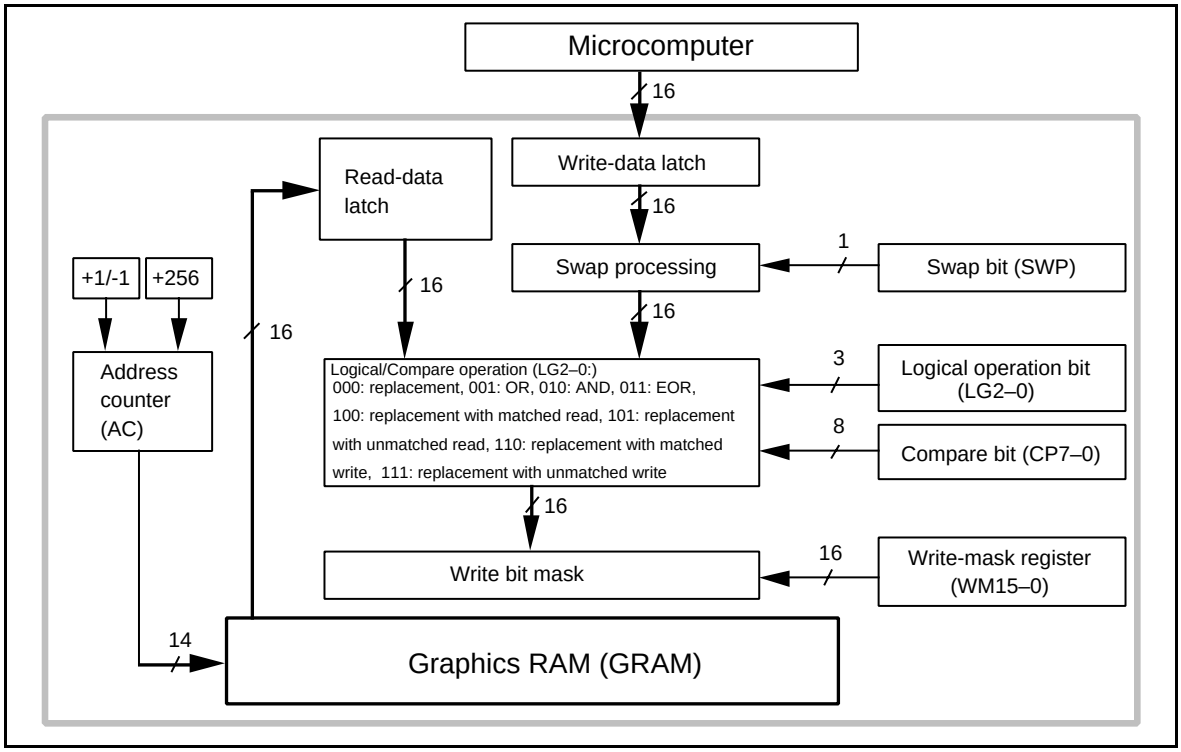


Figure 31 Data Processing Flow of the Graphics Bit Operation

Swap Function

The HD66761 has a byte-wise swap function that exchanges the upper and lower bytes in the two-byte data sent from the microcomputer. When SWP = 0, the data written by the microcomputer is directly transferred to the inside. When SWP = 1, the data written by the microcomputer is internally transferred by exchanging the upper and lower bytes.

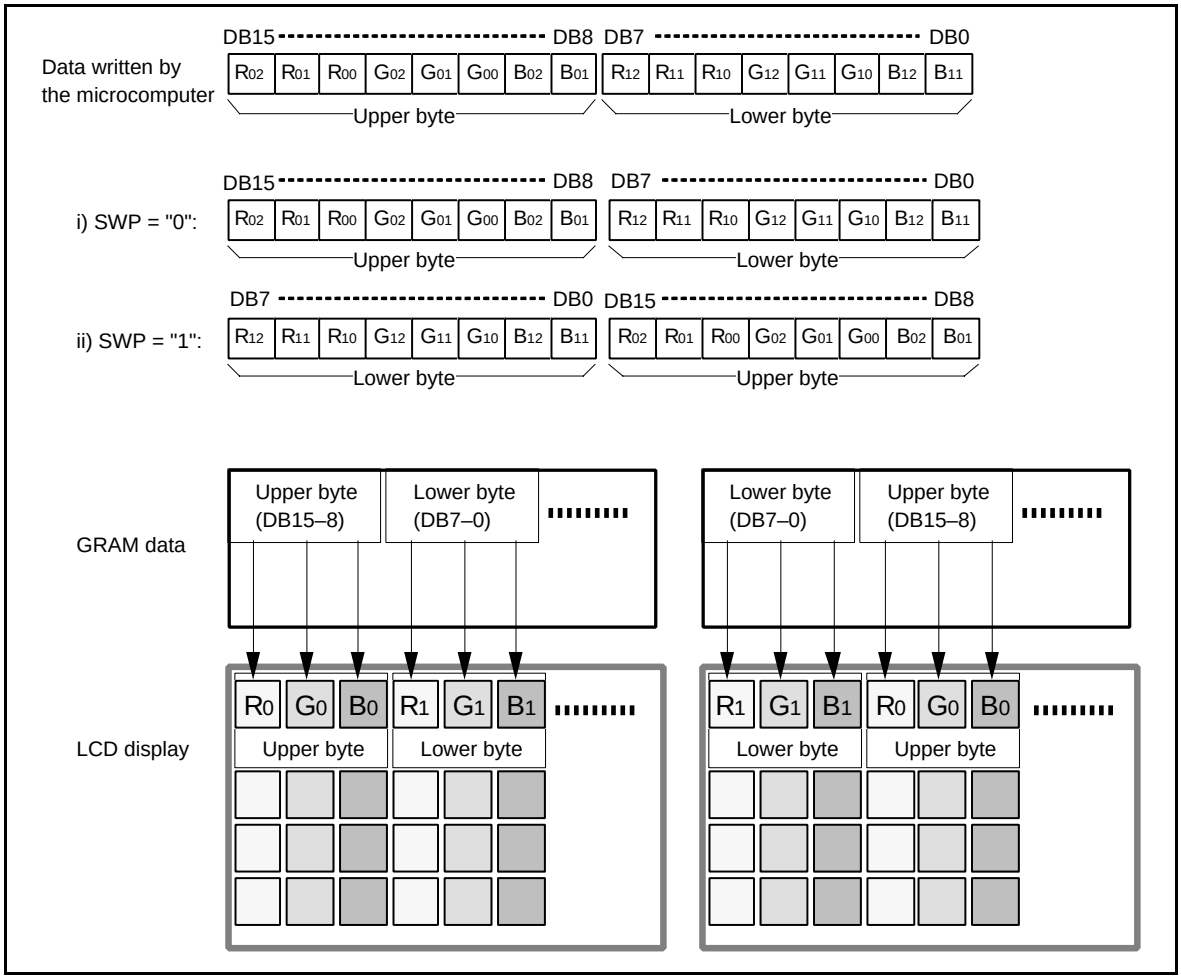


Figure 32 Example of Swap Function Operation

Write-data Mask Function

The HD66761 has a bit-wise write-data mask function that controls writing the two-byte data from the microcomputer to the GRAM. Bits that are 0 in the write-data mask register (WM15–0) cause the corresponding DB bit to be written to the GRAM. Bits that are 1 prevent writing to the corresponding GRAM bit to the GRAM; the data in the GRAM is retained. This function can be used when only one-pixel data is rewritten or the particular display color is selectively rewritten.

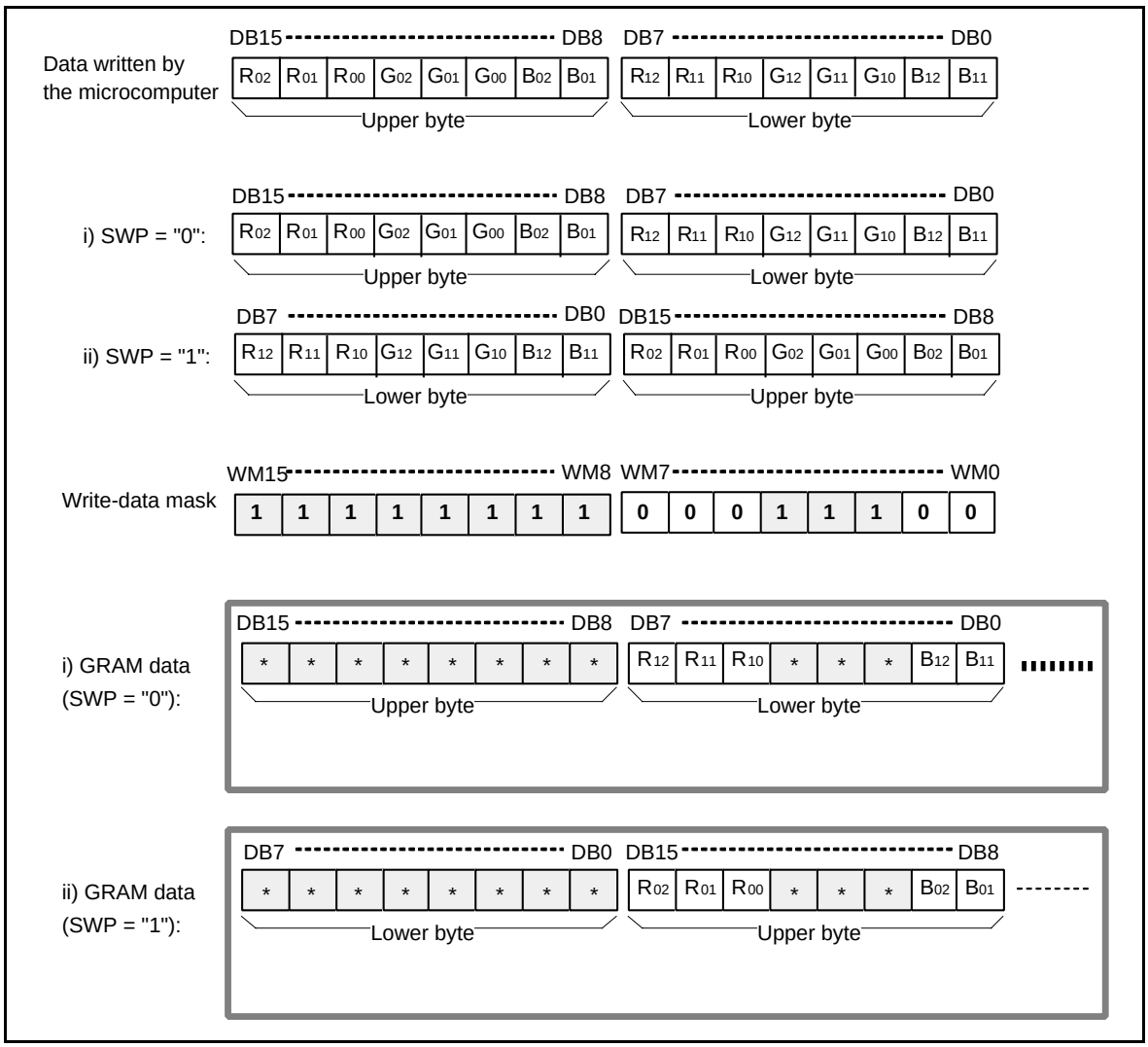


Figure 33 Example of Write-data Mask Function Operation

Logical/Compare Operation Function

The HD66761 performs a logical operation or conditional replacement between the two-byte write data sent from the microcomputer and the read data from the GRAM. The logical operation function has four types: replacement, OR, AND, and EOR. The conditional replacement performs a compare operation for the set value of the compare register (CP7–0) and the read data value from the GRAM, and rewrites only the pixel data in the GRAM that satisfies the conditions (in a byte unit). This function can be used when a particular color is selectively rewritten. The swap function or write-data mask function can be effectively used.

Table 31 Logical/Compare Operation

Bit Setting			
LG2	**LG1**	**LG0**	**Description of Logical/Compare Operation Function**
0	0	0	Writes the data written from the microcomputer directly to the GRAM. Only write processing is performed since the data in the read-data latch is not used.
0	0	1	ORs the data in the read-data latch and the data written by the microcomputer. Writes the result to GRAM. Read, modify, or write processing is performed.
0	1	0	ANDs the data in the read-data latch and the data written by the microcomputer. Writes the result to GRAM.
0	1	1	EORs the data in the read-data latch and the data written by the microcomputer. Writes the result to GRAM.
1	0	0	Compares the data in the read-data latch and the set value of the compare register (CP7–0). When the read data matches CP7–0, the data from the microcomputer is written to the GRAM. Only the particular color specified in the compare register can be rewritten. Read, modify, or write processing is performed.
1	0	1	Compares the data in the read-data latch and the set value of the compare register (CP7–0). When the read data does not match CP7–0, the data from the microcomputer is written to the GRAM. Colors other than the particular one specified in the compare register can be rewritten. Read, modify, or write processing is performed.
1	1	0	Compares the data written to the GRAM by the microcomputer and the set value of the compare register (CP7–0). When the write data matches CP7–0, the data from the microcomputer is written to the GRAM. Only write processing is performed.
1	1	1	Compares the data written to the GRAM by the microcomputer and the set value of the compare register (CP7–0). When the write data does not match CP7–0, the data from the microcomputer is written to the GRAM. Only write processing is performed.

Graphics Operation Processing

1. Write mode 1: AM = 0, LG2–0 = 000

   This mode is used when the data is horizontally written at high speed. It can also be used to initialize the graphics RAM (GRAM) or to draw borders. The swap function (SWP) and write-data mask function (WM15–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edge of the GRAM.

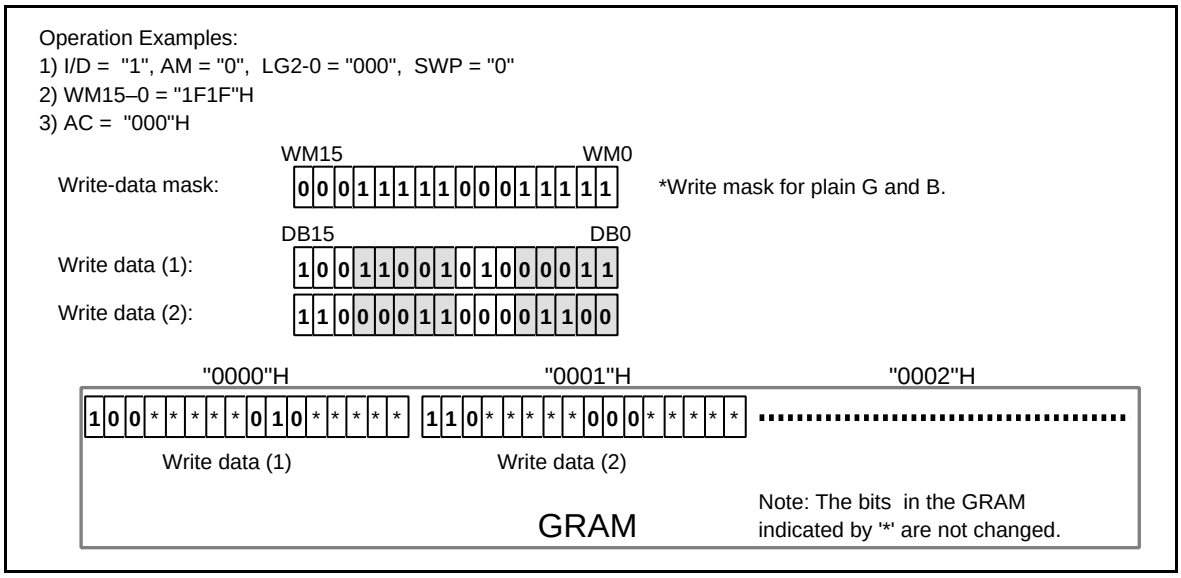
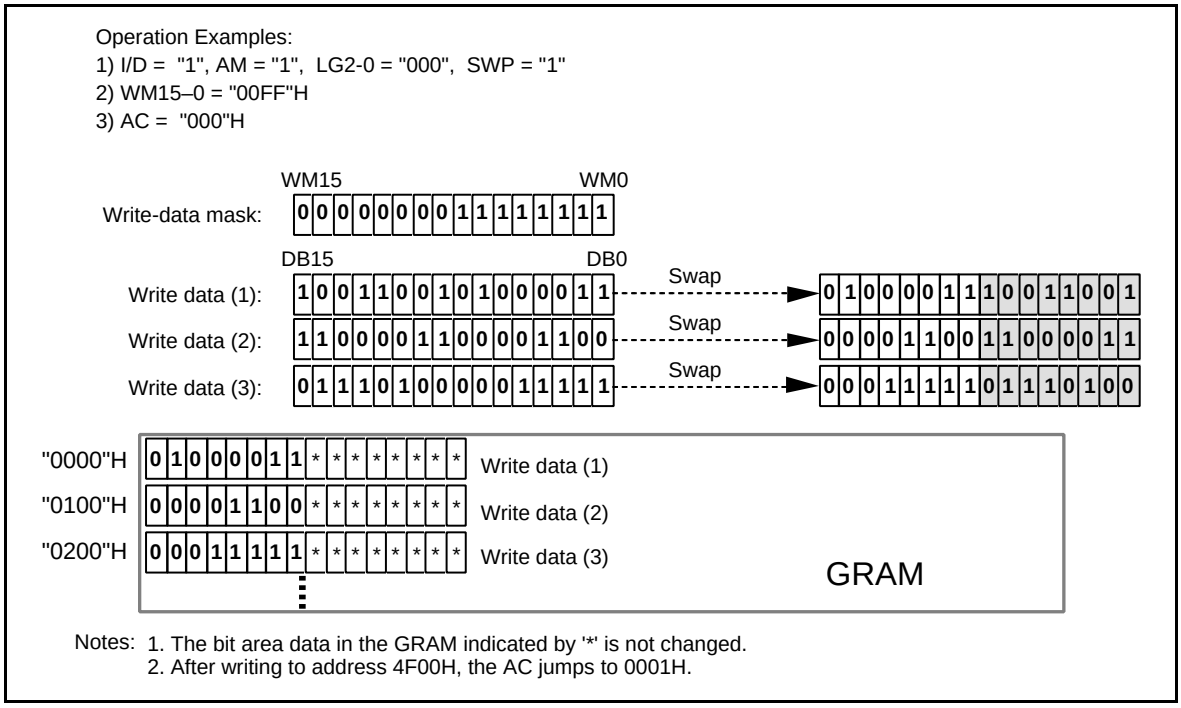


Figure 34 Writing Operation of Write Mode 1

2. Write mode 2: AM = 1, LG2–0 = 000

This mode is used when the data is vertically written at high speed. It can also be used to initialize the GRAM, develop the font pattern in the vertical direction, or draw borders. The swap function (SWP) and write-data mask function (WM15–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.



Notes: 1. The bit area data in the GRAM indicated by '*' is not changed.
2. After writing to address 4F00H, the AC jumps to 0001H.

Figure 35 Writing Operation of Write Mode 2

3. Write mode 3: AM = 0, LG2–0 = 110/111

This mode is used when the data is horizontally written by comparing the write data and the set value of the compare register (CP7–0). When the result of the comparison in a byte unit satisfies the condition, the write data sent from the microcomputer is written to the GRAM. In this operation, the swap function (SWP) and write-data mask function (WM15–0) are also enabled. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edge of the GRAM.

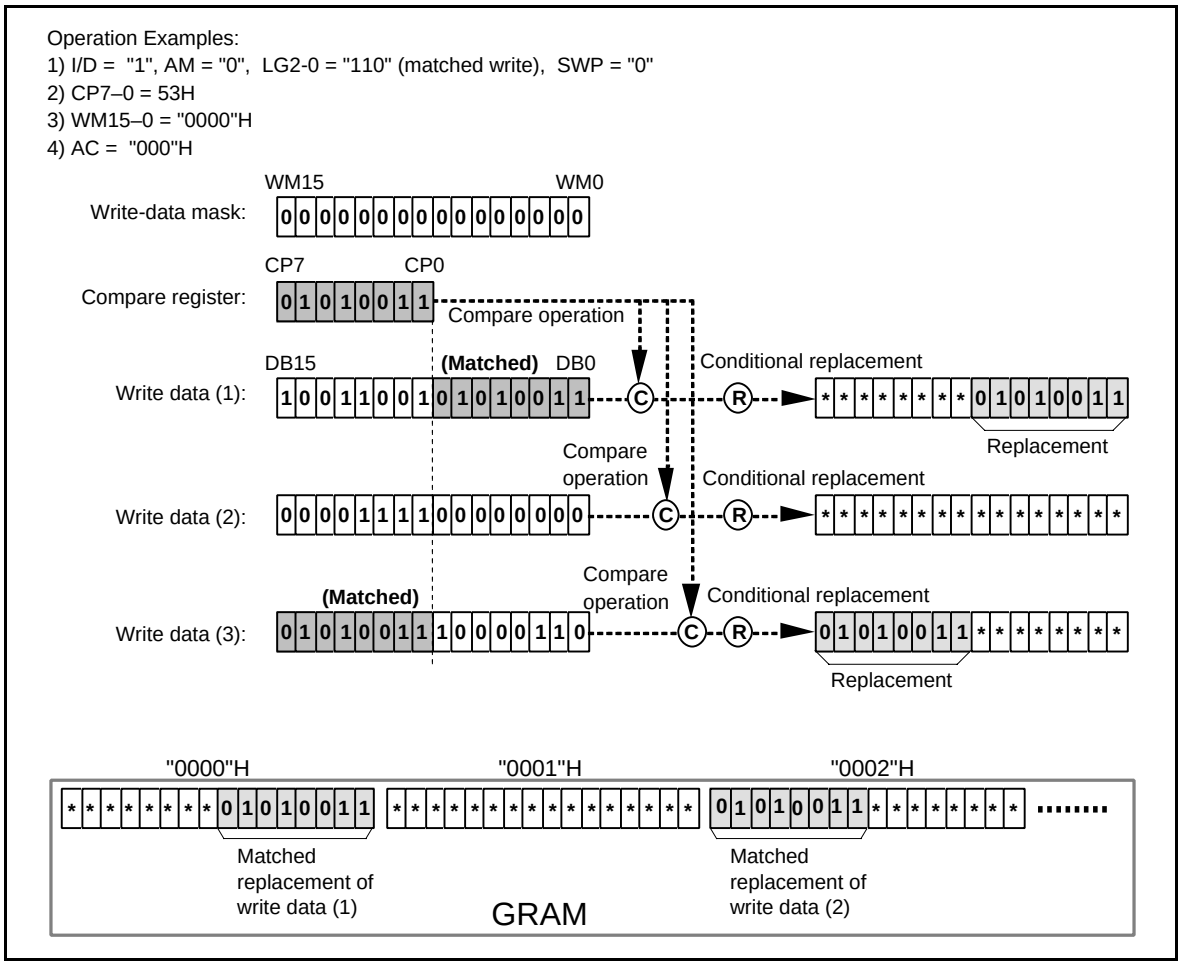


Figure 36 Writing Operation of Write Mode 3

4. Write mode 4: AM = 1, LG2–0 = 110/111

This mode is used when a vertical comparison is performed between the write data and the set value of the compare register (CP7–0) to write the data. When the result by the comparison in a byte unit satisfies the condition, the write data sent from the microcomputer is written to the GRAM. In this operation, the swap function (SWP) and write-data mask function (WM15–0) are also enabled. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.

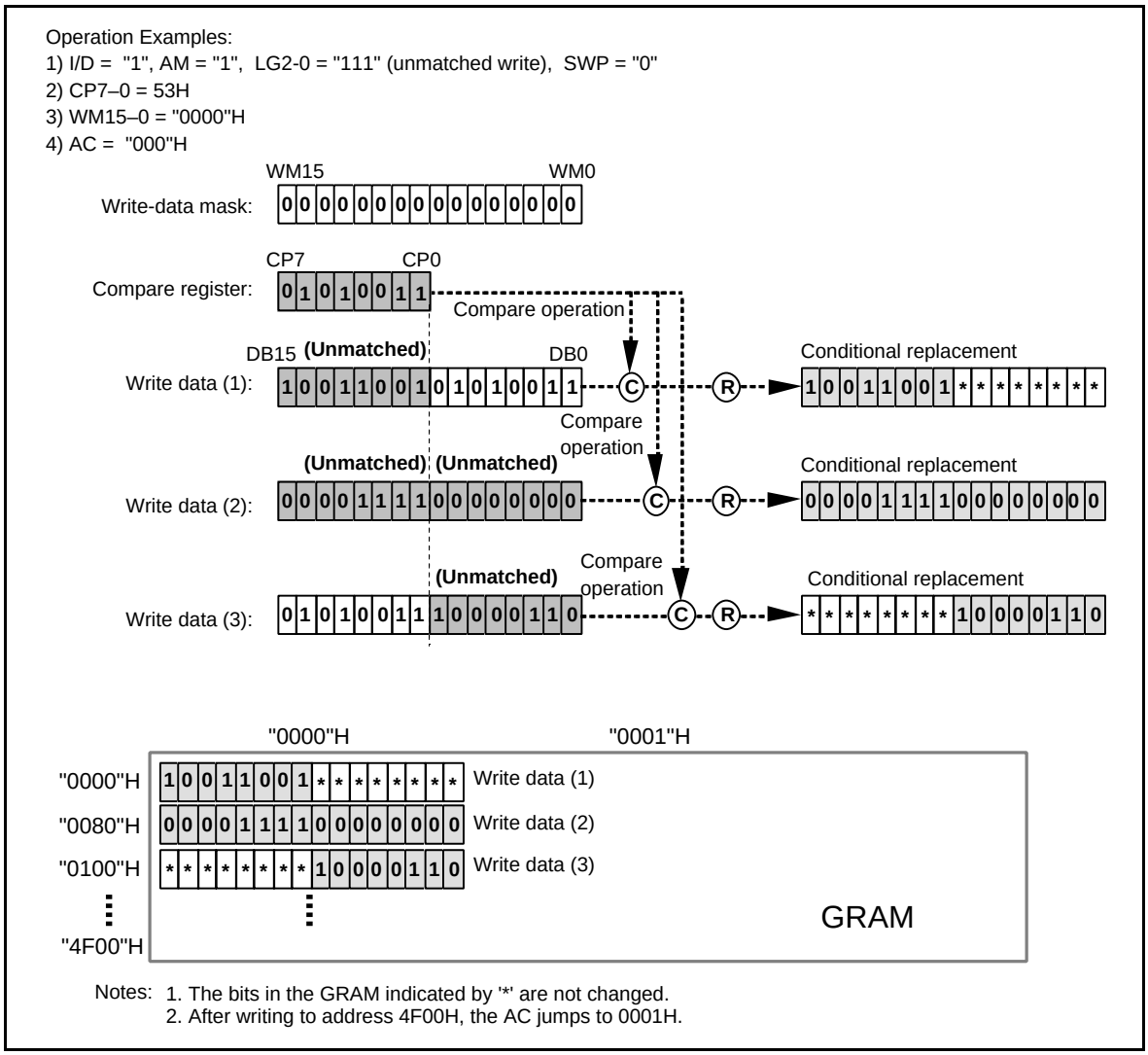


Figure 37 Writing Operation of Write Mode 4

5. Read/Write mode 1: AM = 0, LG2–0 = 001/010/011

This mode is used when the data is horizontally written at high speed by performing a logical operation with the original data. It reads the display data (original data), which has already been written in the GRAM, performs a logical operation with the write data sent from the microcomputer, and rewrites the data to the GRAM. This mode reads the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as the write operation since reading the original data does not latch the read data into the microcomputer but temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The swap function (SWP) or write-data mask function (WM15–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edges of the GRAM.

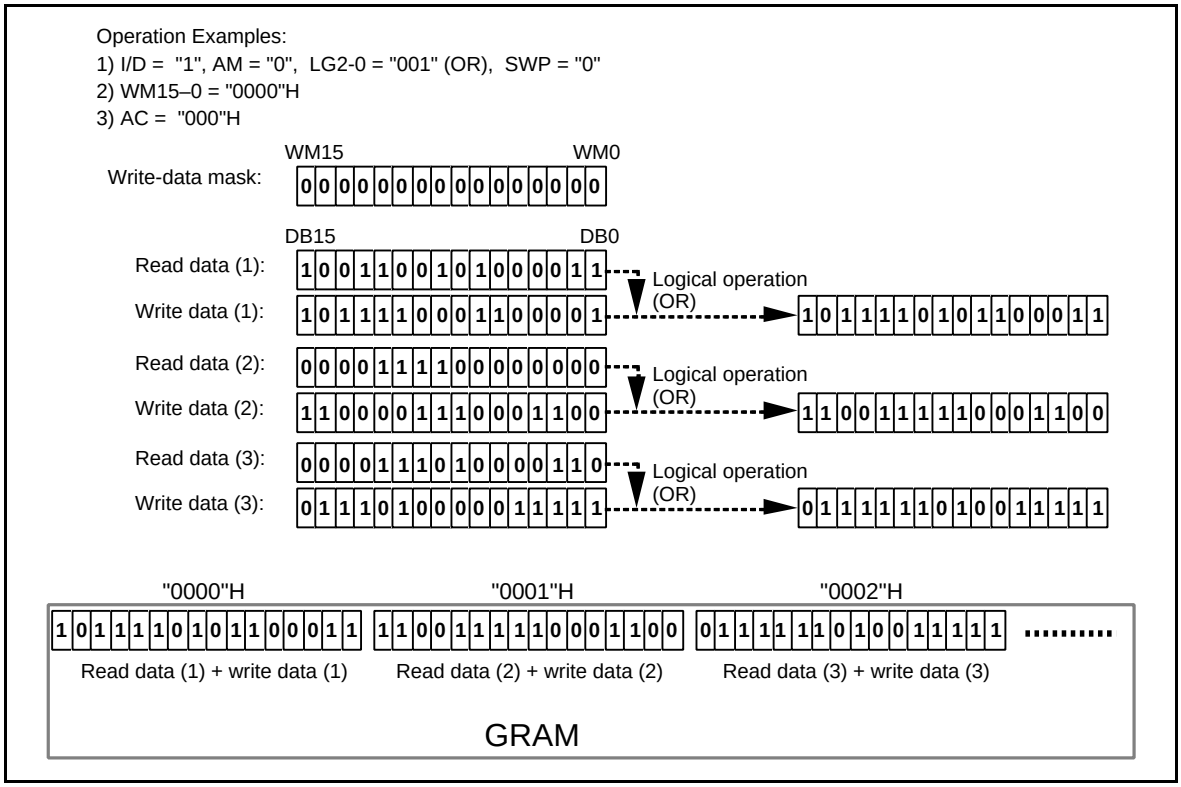


Figure 38 Writing Operation of Read/Write Mode 1

6. Read/Write mode 2: AM = 1, LG1–0 = 001/010/011

This mode is used when the data is vertically written at high speed by performing a logical operation with the original data. It reads the display data (original data), which has already been written in the GRAM, performs a logical operation with the write data sent from the microcomputer, and rewrites the data to the GRAM. This mode can read the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as for the write operation since the read operation of the original data does not latch the read data into the microcomputer and temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The swap function (SWP) or write-data mask function (WM15–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.

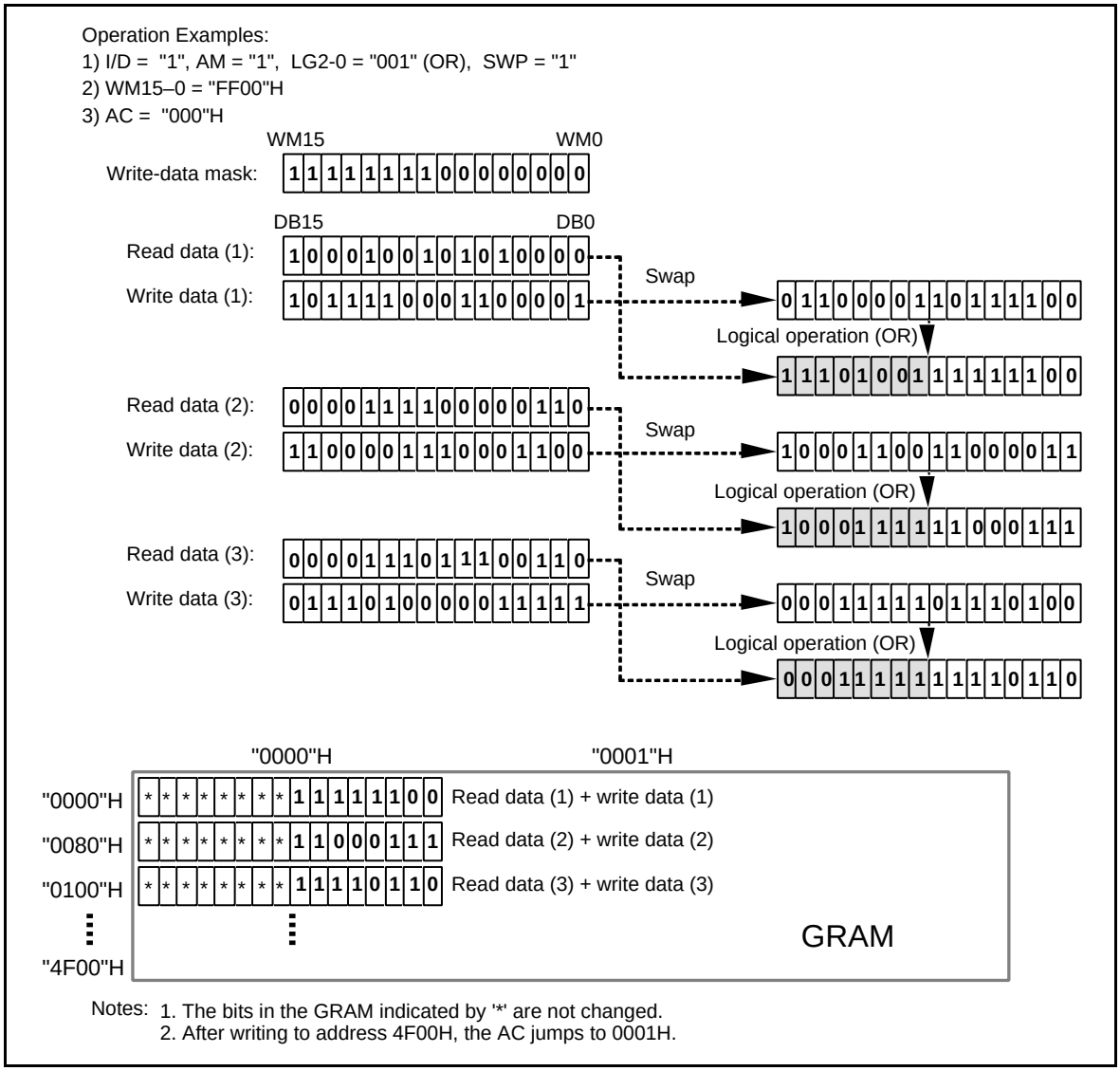


Figure 39 Writing Operation of Read/Write Mode 2

7. Read/Write mode 3: AM = 0, LG2–0 = 100/101

This mode is used when the data is horizontally written by comparing the original data and the set value of compare register (CP7–0). It reads the display data (original data), which has already been written in the GRAM, compares the original data and the set value of the compare register in byte units, and writes the data sent from the microcomputer to the GRAM only when the result of the comparison satisfies the condition. This mode reads the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as write operation since reading the original data does not latch the read data into the microcomputer but temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The swap function (SWP) and write-data mask function (WM15–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edges of the GRAM.

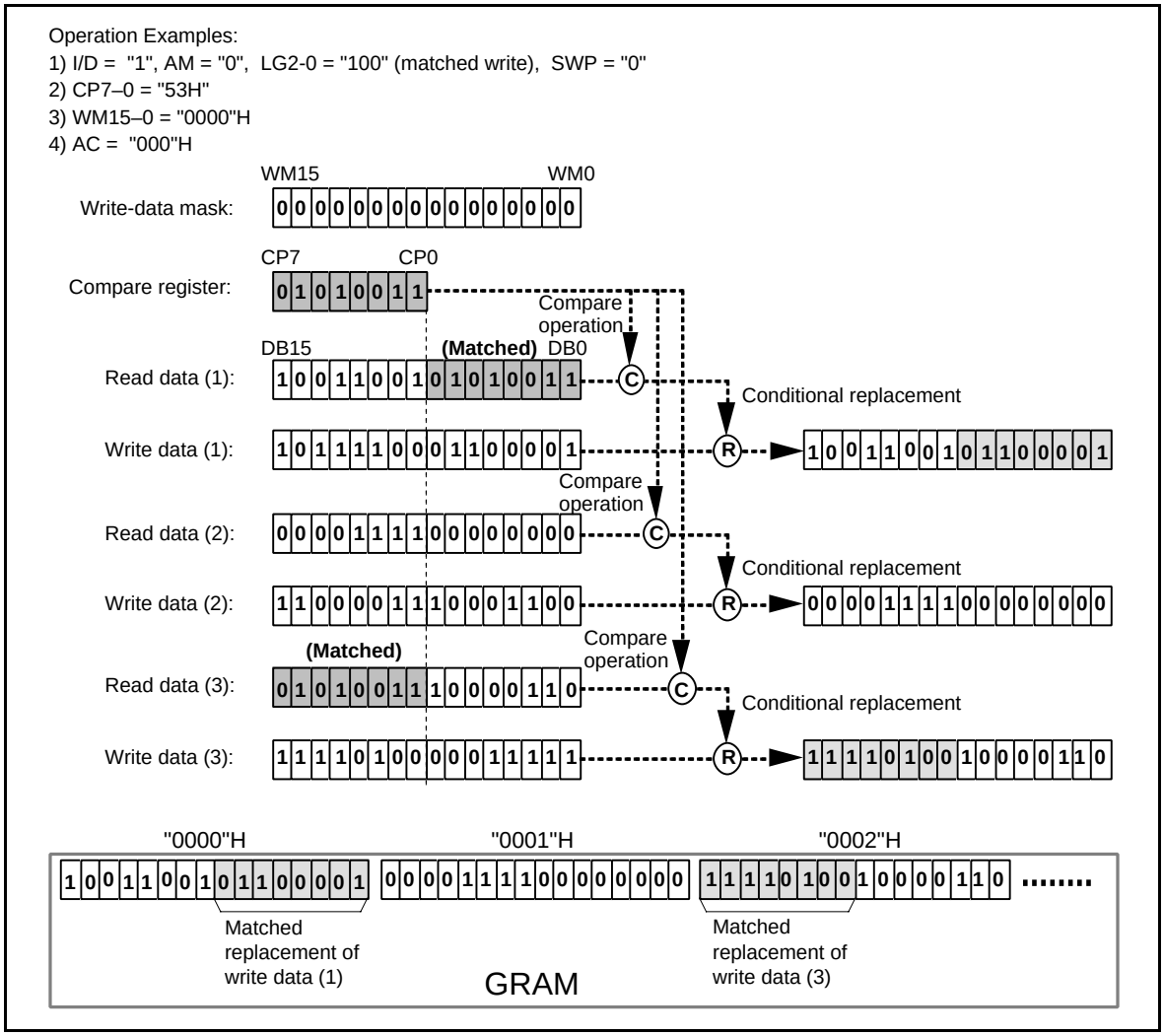
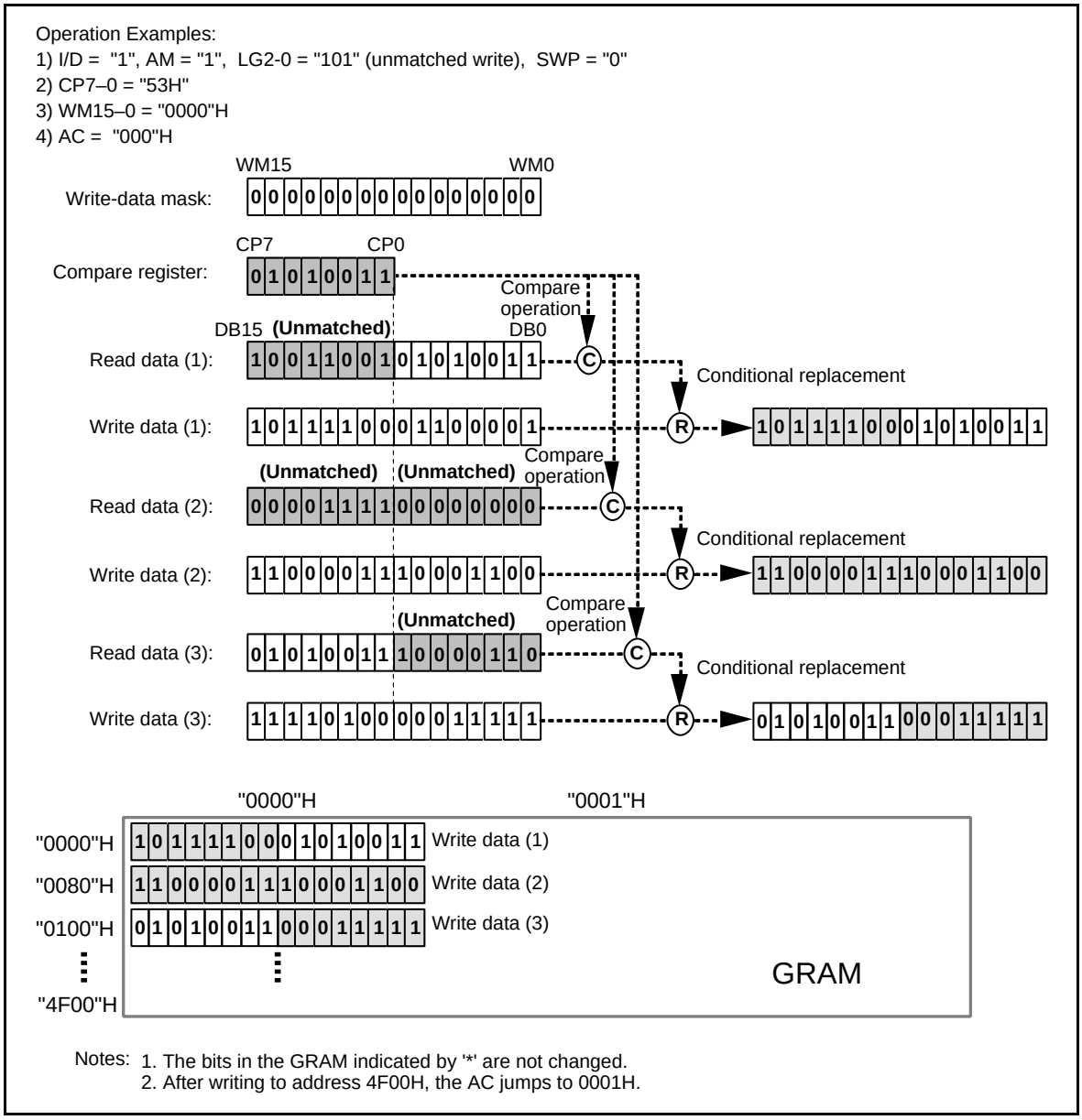


Figure 40 Writing Operation of Read/Write Mode 3

8. Read/Write mode 4: AM = 1, LG2–0 = 100/101

   This mode is used when the data is vertically written by comparing the original data and the set value of the compare register (CP7–0). It reads the display data (original data), which has already been written in the GRAM, compares the original data and the set value of the compare register in byte units, and writes the data sent from the microcomputer to the GRAM only when the result of the compare operation satisfies the condition. This mode reads the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as the write operation since reading the original data does not latch the read data into the microcomputer but temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The swap function (SWP) and write-data mask function (WM15–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.



Notes: 1. The bits in the GRAM indicated by '*' are not changed.
2. After writing to address 4F00H, the AC jumps to 0001H.

Figure 41 Writing Operation of Read/Write Mode 4

Grayscale Palette

The HD66761 incorporates a grayscale palette to simultaneously display 256 of the 4,096 possible colors. The R and G grayscales consist of eight four-bit palettes, and the B grayscale consists of four four-bit palettes. The 16-stage grayscale levels can be selected from the four-bit palette data.

For the display data of R and G, the three-bit data in the GRAM written from the microcomputer is used. For the display data of B, the two-bit data in the GRAM is used.

In this palette, a curtailed frame grayscale system, which has low charging current in the LCD panel, is used. Although the system is the same for each color, the curtailed frame timing is adjusted between adjacent dots to reduce flickering.

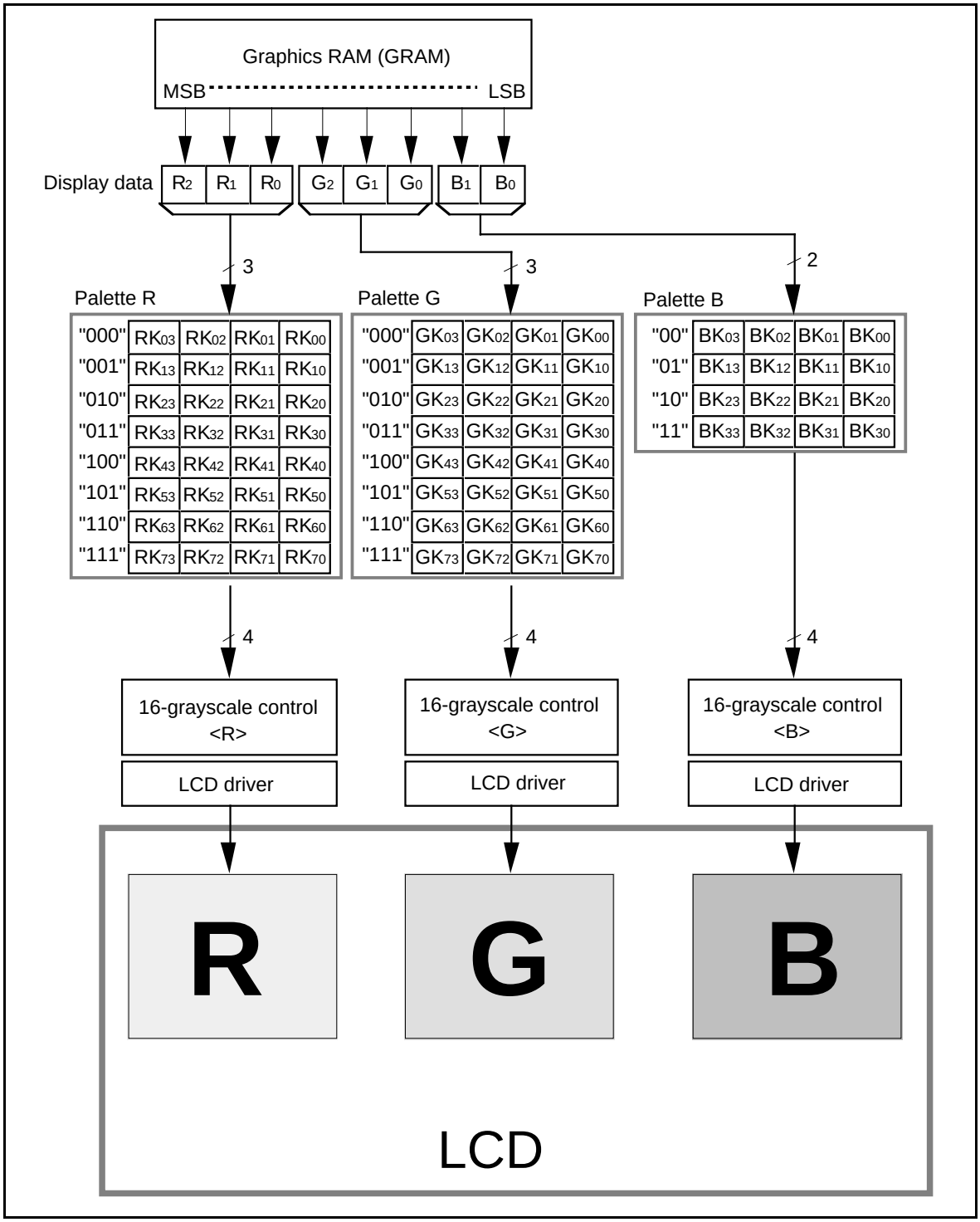


Figure 42 Grayscale Palette Control

Grayscale Palette Table

The grayscale register that is set for each palette register (RK, GK, or BK) can be set to any level. 16-grayscale lighting levels can be set according to palette values (0000 to 1111).

Table 32 Grayscale Control Level

Palette Register Value (RK, GK, or BK)				Grayscale Control Level
0	0	0	0	Unlit level*1
0	0	0	1	2/16 level
0	0	1	0	3/16 level
0	0	1	1	4/16 level
0	1	0	0	5/16 level
0	1	0	1	6/16 level
0	1	1	0	7/16 level
0	1	1	1	8/16 level
1	0	0	0	9/16 level
1	0	0	1	10/16 level
1	0	1	0	11/16 level
1	0	1	1	12/16 level
1	1	0	0	13/16 level
1	1	0	1	14/16 level
1	1	1	0	15/16 level
1	1	1	1	All-lit level*2

Notes: 1. The unlit level corresponds to a black display when a normally-black color-LCD panel is used, and a white display when a normally-white color-LCD panel is used.

2. The all-lit level corresponds to a white display when a normally-black color-LCD panel is used, and a black display when a normally-white color-LCD panel is used.

Four-color Display Mode

The HD66761 has the four-color display mode consisting of two-bit-per-pixel data. Since the byte-wise processing of four-pixel display data is enabled, the processing performance is four times that of the normal 256-color display. When the internal grayscale palette is used, four colors of the possible 4,096 colors can be displayed at the same time. The two-bit display data in the GRAM written from the microcomputer is assigned to the lower two bits of R and G; one of these bits, always 0, synthesizes the three-bit data. Therefore, this display mode uses 000, 001, 010, 011 in grayscale palettes R and G.

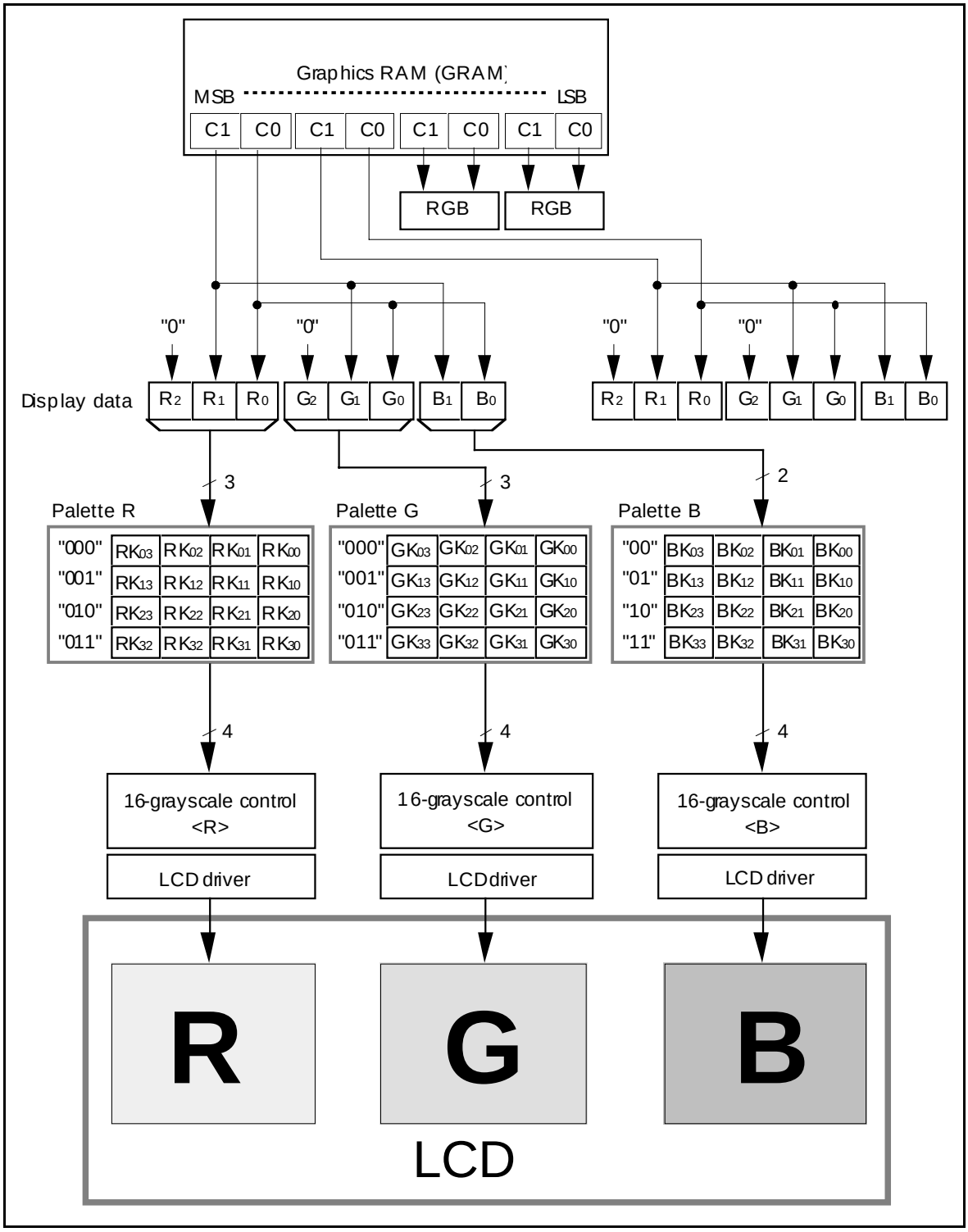


Figure 43 Four-color Display Control

Color Window Cursor Control

A cursor is displayed in the window area specified by the cursor-start position register (CSX or CSY) and cursor-end position register (CEX or CEY). The cursor display mode can be selected from four types in table 33 by changing cursor-mode bit (CM1–0).

The eight-color cursor display can be selected by the cursor-color bit (CR, CG, or CB) and displays red, blue, green, white, black or a combined color. However, the grayscale of the cursor color cannot be controlled.

Table 33 Cursor Display Control

Register Setting			
C	**CM1**	**CM0**	**Cursor Display Control**
0	*	*	Displays no cursor.
1	0	0	Displays eight colors specified by the cursor-color bit (CR, CG, or CB) in the window area.
1	0	1	Reverses and displays the four-bit grayscale data of each color in the window area.
1	1	0	Alternately repeats the normal display in the window area and the eight-color display specified by the cursor-color bit (CR, CG, or CB) every 32 frame for blinking display.
1	1	1	Alternately repeats the normal display in the window area and the reversal display of the four-bit grayscale data every 32 frame for blinking display.

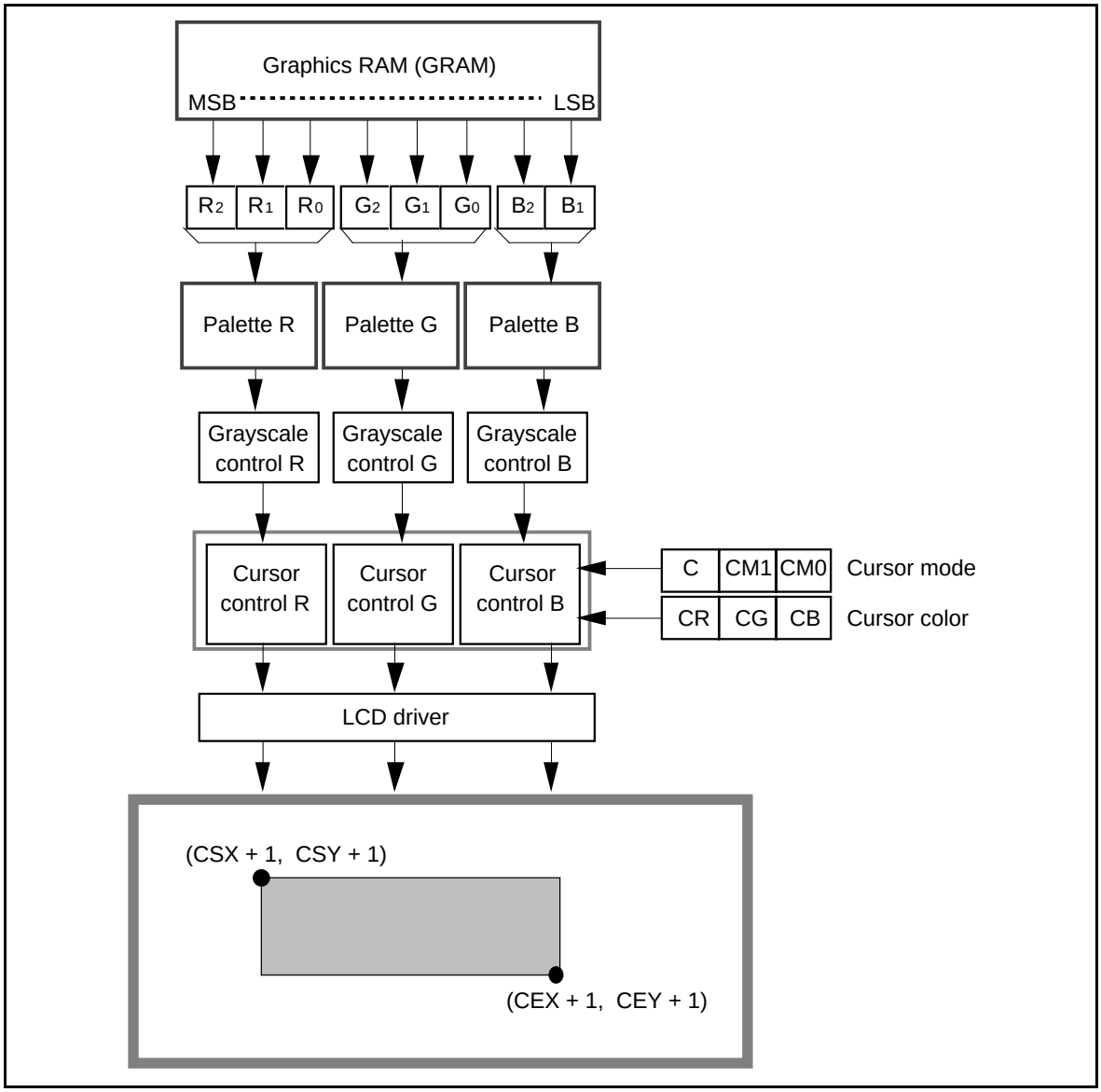


Figure 44 Color-cursor Display

Oscillation Circuit

The HD66761 can oscillate between the OSC1 and OSC2 pins on the master side using an internal R-C oscillator with an external oscillation resistor. The oscillation clock output from the CL2 pin on the master side is input to the CL2 pin on the slave side. Note that in R-C oscillation, the oscillation frequency is changed according to the external resistance value, wiring length, or operating power-supply voltage. If Rf is increased or power supply voltage is decrease, the oscillation frequency decreases. For the relationship between Rf resistor value and oscillation frequency, see the Electric Characteristics Notes section.

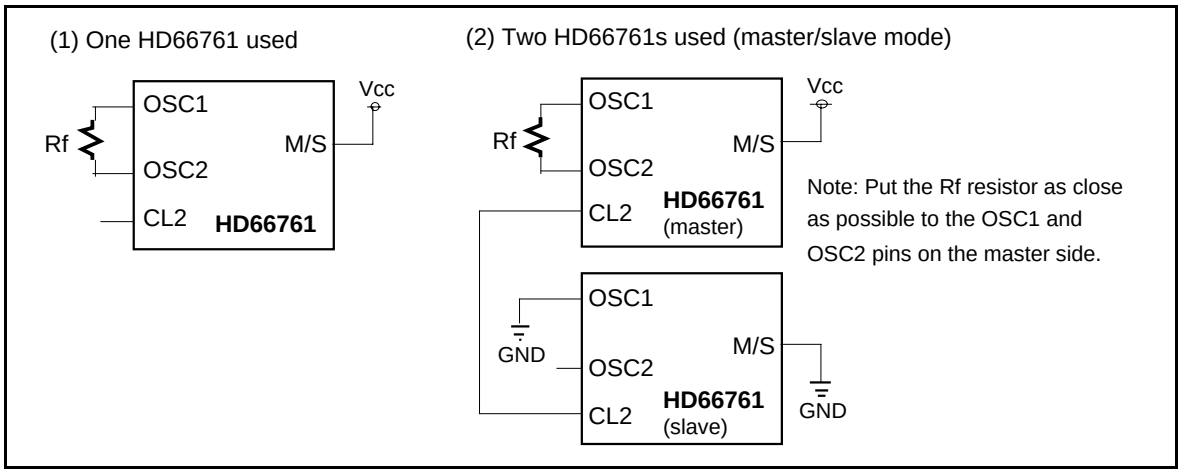


Figure 45 Oscillation Circuits

Table 34 Relationship between Liquid Crystal Drive Duty Ratio and Frame Frequency

LCD Duty	NL4–0 Set Value	Recommended Drive Bias Value	Frame Frequency	One-frame Clock
1/16	01H	1/5	70 Hz	2560
1/24	02H	1/6	70 Hz	2560
1/32	03H	1/6	70 Hz	2568
1/40	04H	1/7	70 Hz	2560
1/48	05H	1/8	71 Hz	2544
1/56	06H	1/8	70 Hz	2576
1/64	07H	1/9	70 Hz	2560
1/72	08H	1/9.5	71 Hz	2520
1/80	09H	1/10	70 Hz	2560

Note: The frame frequency above is for 180-kHz operation and proportions the oscillation frequency (fosc).

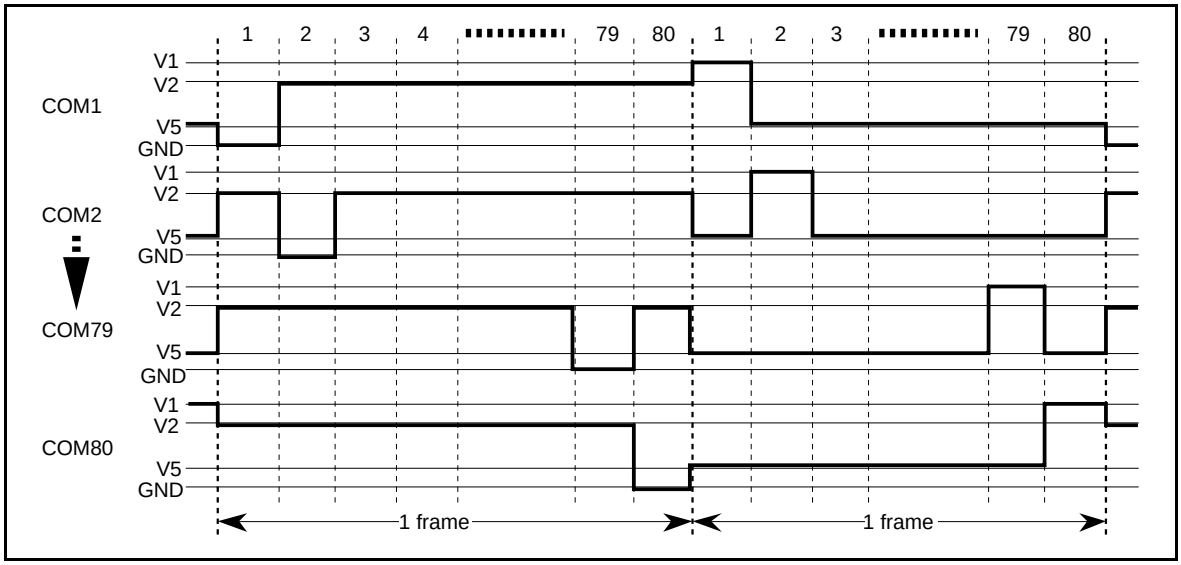


Figure 46 LCD Drive Output Waveform (B-pattern AC Drive with 1/80 Multiplexing Duty Ratio)

Multi-chip Operation

The HD66761 can extend the display size up to 128 (RGB)-by-160 dots by using two chips and vertically driving two screens. The chip on the master side generates the R-C oscillating frequency or step-up output voltage and adjusts contrast by electron volume. The display on/off is controlled on both the master and slave sides. After power is supplied to the master side, turn on the display on the slave side.

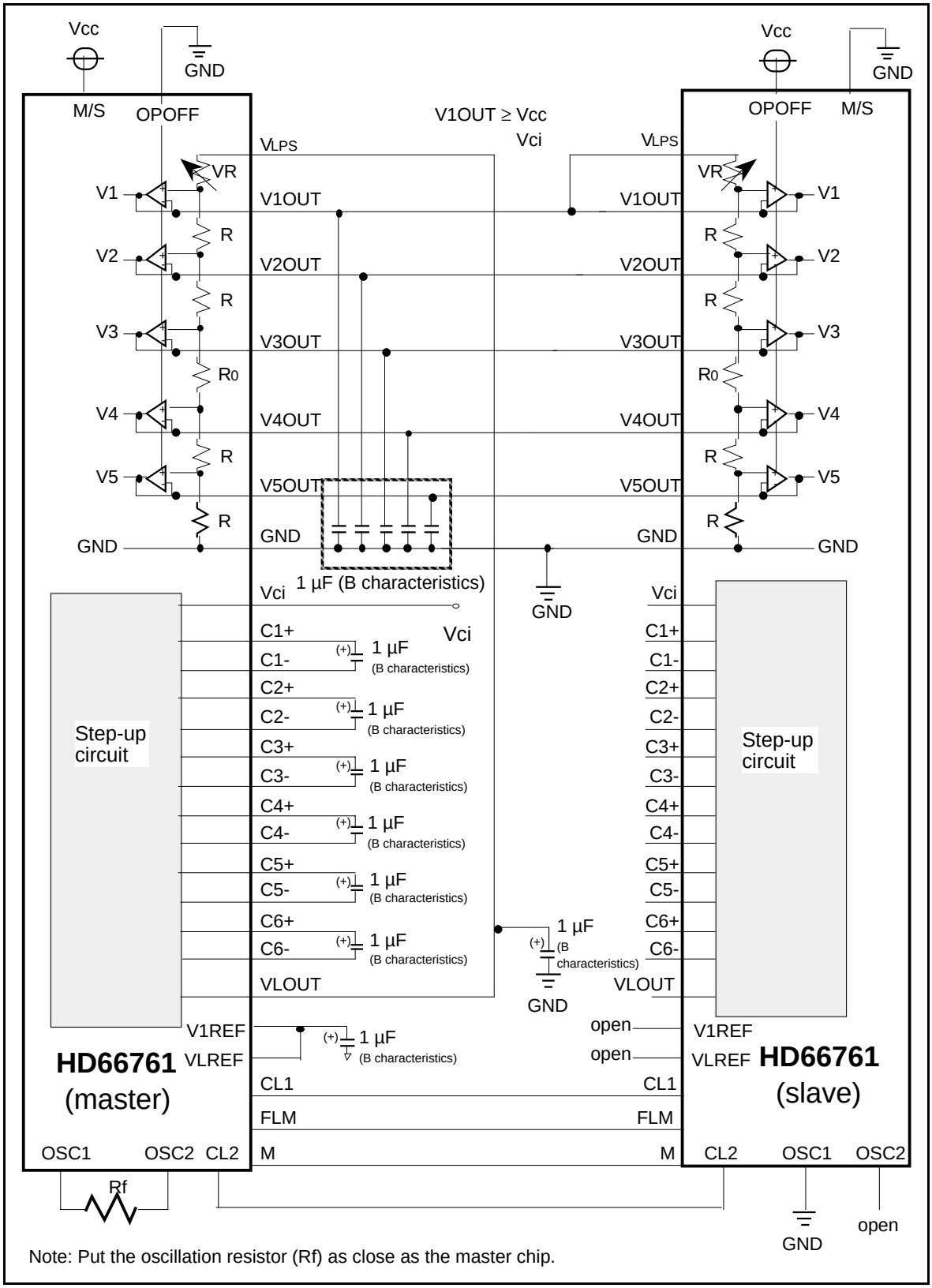
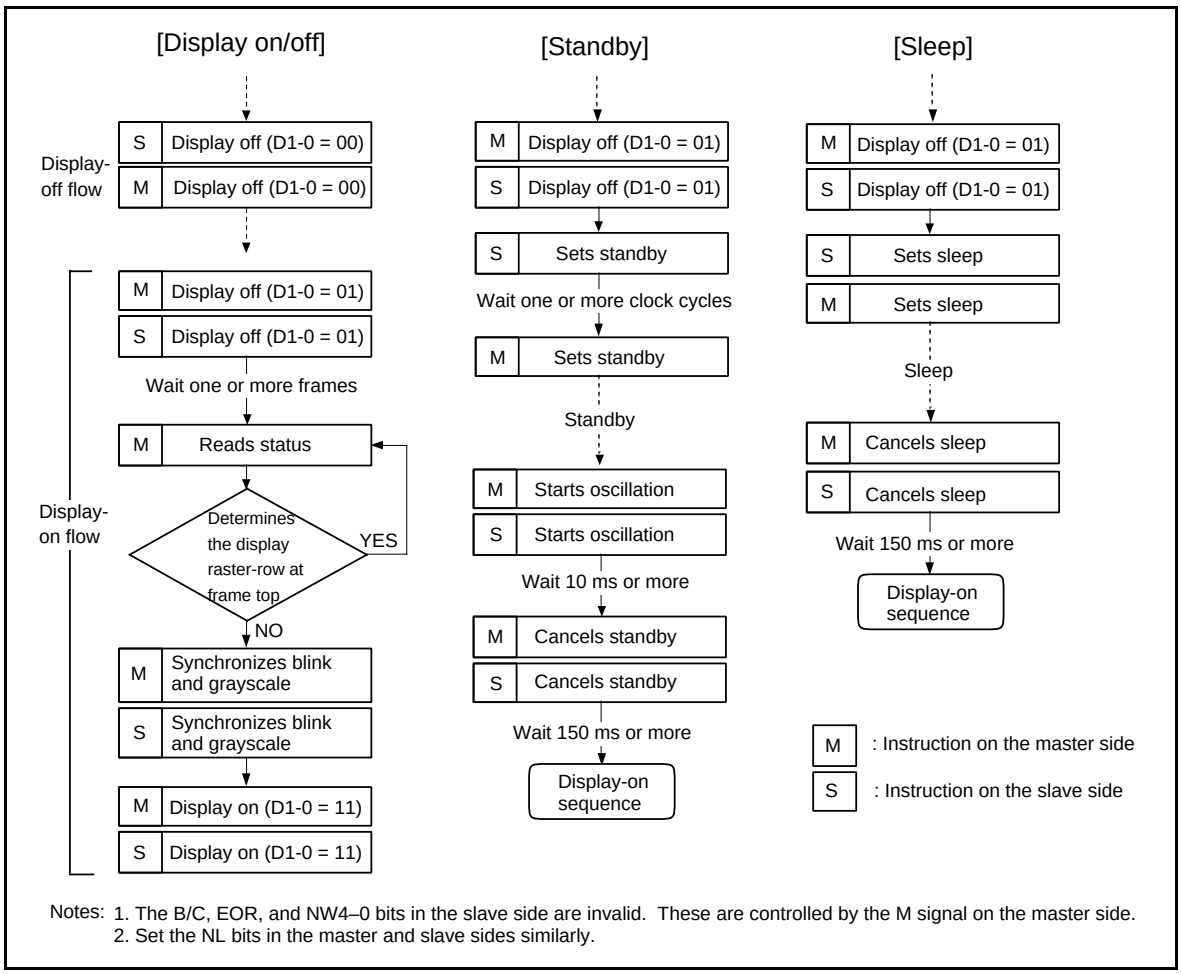


Figure 47 Multi-chip Configuration

Instruction Flow at Multi-chip Operation

The displays are turned on or off synchronously during multi-chip operation by a signal (M, FLM, CL1, or CL2) from the master to the slave. Turn the display on after synchronization because the blink and grayscale synchronize instruction synchronizes the blink cycle on the master/slave side with the grayscale-pattern generation cycle. When switching to standby, set the slave side to standby before the master side. After standby cancellation, stabilize the timing of the internal power supply and then turn the display on.



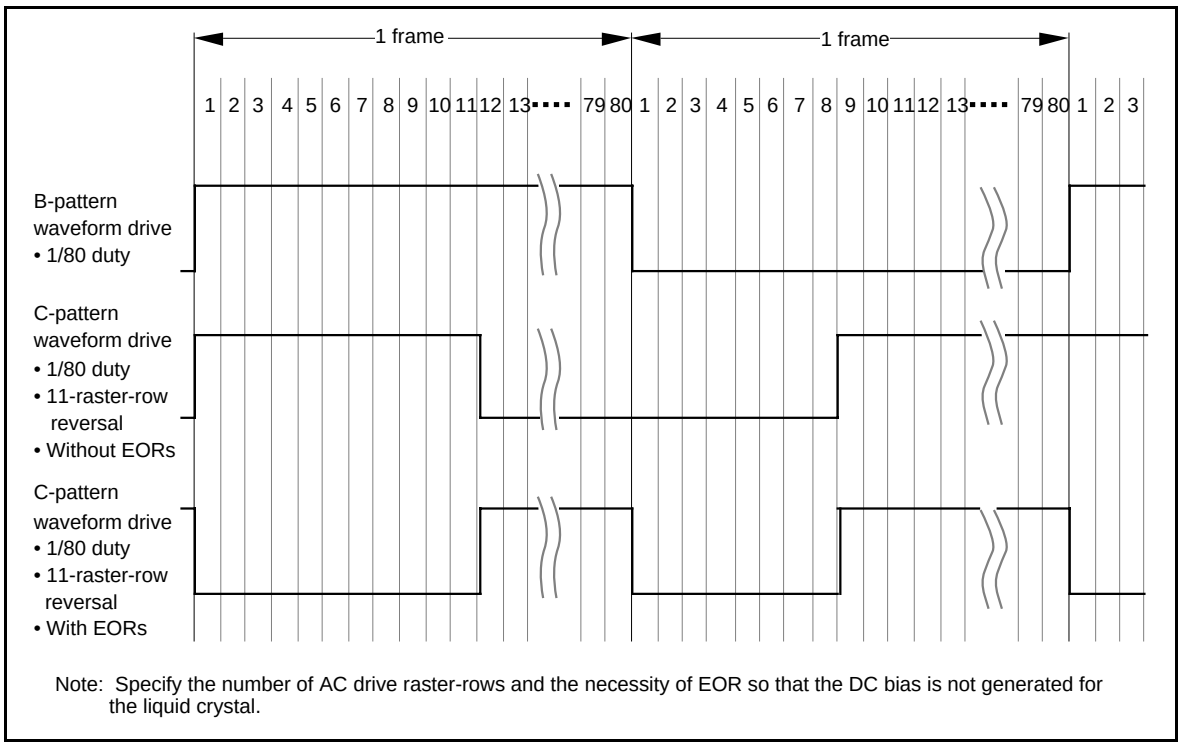
Notes: 1. The B/C, EOR, and NW4–0 bits in the slave side are invalid. These are controlled by the M signal on the master side.
2. Set the NL bits in the master and slave sides similarly.

Figure 48 Instruction Flow

n-raster-row Reversed AC Drive

The HD66761 supports not only the LCD reversed AC drive in a one-frame unit (B-pattern waveform) but also the n-raster-row reversed AC drive which alternates in an n-raster-row unit from one to 32 raster-rows (C-pattern waveform). When a problem affecting display quality occurs, such as crosstalk at high-duty driving of more than 1/64 duty, the n-raster-row reversed AC drive (C-pattern waveform) can improve the quality. When two HD66761s are used in a master/slave setup, the LCD drive polarity on the master and slave sides is reversed.

Determine the number of raster-rows n (NW bit set value + 1) for alternating after confirmation of the display quality with the actual LCD panel. However, if the number of AC raster-rows is reduced, the LCD alternating frequency becomes high. Because of this, the charge or discharge current is increased in the LCD cells.



Note: Specify the number of AC drive raster-rows and the necessity of EOR so that the DC bias is not generated for the liquid crystal.

Figure 49 Example of an AC Signal under n-raster-row Reversed AC Drive

Liquid-crystal-display Drive-bias Selector

An optimum liquid-crystal-display bias value can be selected using the BS2-0 bits, according to the liquid crystal drive duty ratio setting (NL3-0 bits). The liquid-crystal-display drive duty ratio and bias value can be displayed while switching software applications to match the LCD panel display status. The optimum bias value calculated using the following expression is a logical optimum value. Driving by using a lower value than the optimum bias value provides lower logical contrast and lower liquid-crystal-display voltage (the potential difference between V1 and GND), which results in better image quality. When the liquid-crystal-display voltage is insufficient even if a seven-times step-up circuit is used, when the step-up driving ability is lowered by setting a high factor for the step-up circuit, or when the output voltage is lowered because the battery life has been reached, the display can be made easier to see by lowering the liquid-crystal-display bias.

The liquid crystal display can be adjusted by using the contrast adjustment register (CT6-0 bits) and selecting the step-up output level (BT1/0 bits).

$$\text{Optimum bias value for 1/N duty ratio drive voltage} = \frac{1}{\sqrt{N} + 1}$$

Table 35 Optimum Drive Bias Values

LCD drive duty ratio	1/80	1/72	1/64	1/56	1/48	1/40	1/32	1/24	1/16
(NL3-0 set value)	1001	1000	0111	0111	0111	0111	0100	0011	0010
Optimum drive bias value	1/10	1/9	1/9	1/8	1/8	1/7	1/6	1/6	1/5
(BS2-0 set value)	001	010	010	010	010	010	101	101	100

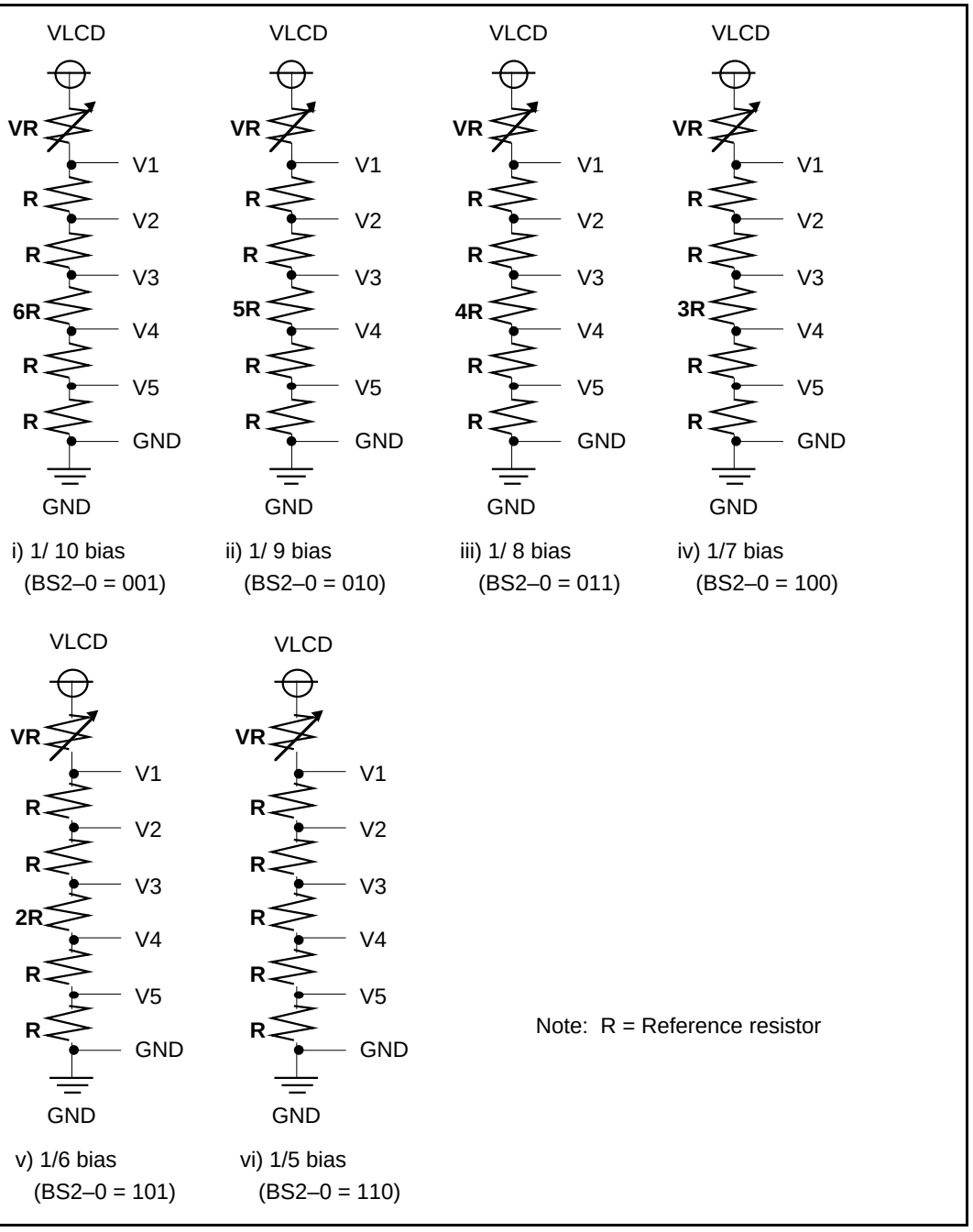


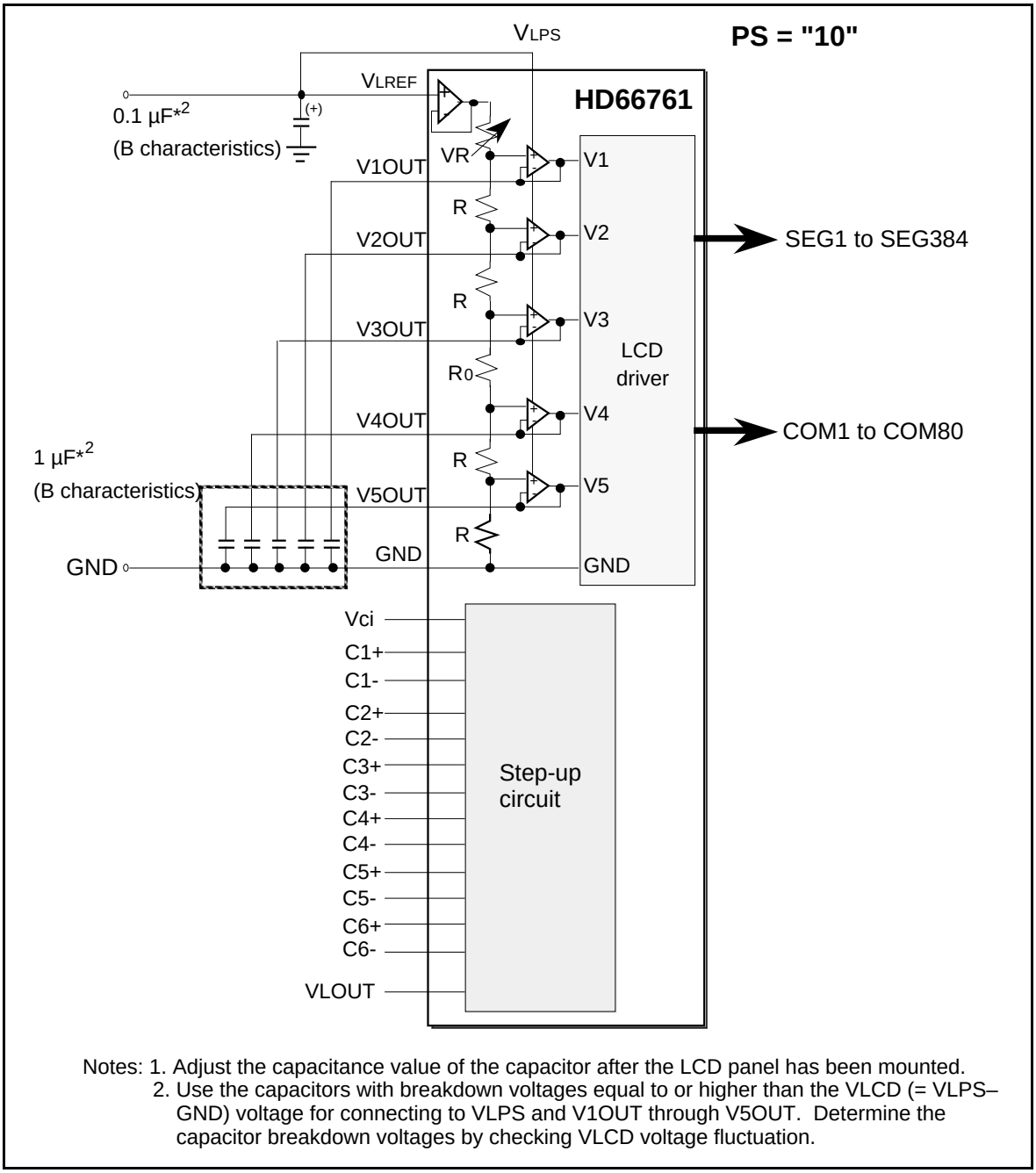
Figure 50 Liquid Crystal Display Drive Bias Circuit

Liquid Crystal Display Voltage Generator

When External Power Supply and Internal Operational Amplifiers are Used

To supply LCD drive voltage directly from the external power supply without using the internal step-up circuit, circuits should be connected as shown in figure 51. Here, contrast can be adjusted by software through the CT bits of the contrast adjustment register. Minimize the voltage variation since the VLREF input is a reference voltage that determines the LCD drive voltage.

The HD66761 incorporates a voltage-follower operational amplifier for each V1 to V5 to reduce current flowing through the internal bleeder-resistors, which generate different levels of liquid-crystal drive voltages. Thus, potential difference between V_{LPS} and V1 must be 0.1 V or higher, and that between V4 and GND must be 1.4 V or higher. Note that the OPOFF pin must be grounded when using the operational amplifiers. Place a capacitor of about 1 µF (B characteristics) between each internal operational amplifier (V1OUT to V5OUT outputs) and GND and stabilize the output level of the operational amplifier. Adjust the capacitance value of the stabilized capacitor after the LCD panel has been mounted and the screen quality has been confirmed.



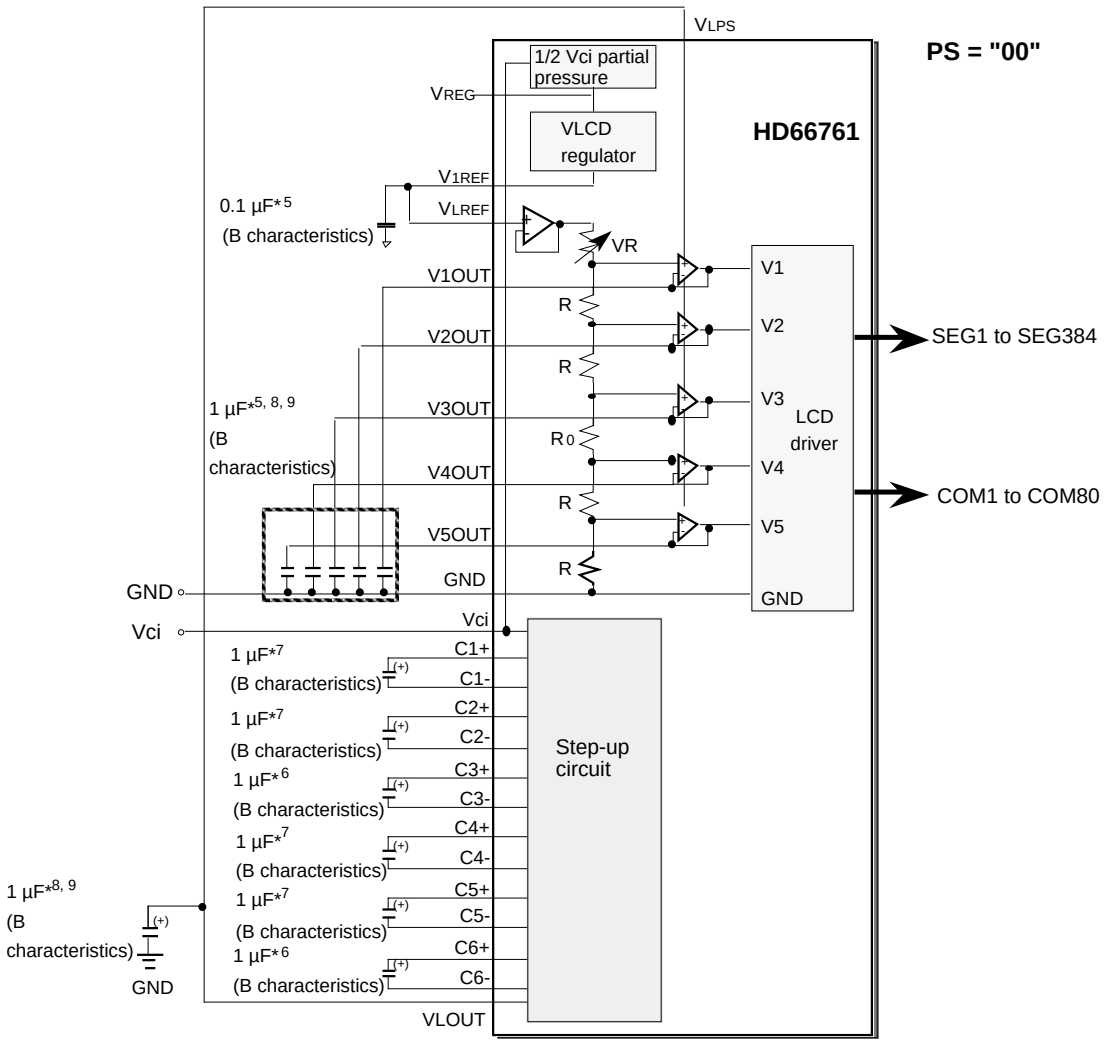
Notes: 1. Adjust the capacitance value of the capacitor after the LCD panel has been mounted.
2. Use the capacitors with breakdown voltages equal to or higher than the VLCD (= VLPS–GND) voltage for connecting to VLPS and V1OUT through V5OUT. Determine the capacitor breakdown voltages by checking VLCD voltage fluctuation.

Figure 51 External Power Supply Circuit for LCD Drive Voltage Generation

When an Internal Booster and Internal Operational Amplifiers are Used

To supply LCD drive voltage using the internal VLCD regulator and step-up circuit, an internal booster and internal operational amplifiers should be connected as shown in figure 52. Keep the power-supply voltage (VLPS) of the operational amplifier higher than the output voltage (V1REF) of the VLCD regulator. Contrast can be adjusted through the CT bits of the contrast control instruction.

The HD66761 incorporates a voltage-follower operational amplifier for each of V1 to V5 to reduce current flowing through the internal bleeder-resistors, which generate different liquid-crystal drive voltages. Thus, potential difference between V_{LPS} and V1 must be 0.1 V or higher, and that between V4 and GND must be 1.4 V or higher. Note that the OPOFF pin must be grounded when using the operational amplifiers. Place a capacitor of about 1 µF (B characteristics) between each internal operational amplifier (V1OUT to V5OUT outputs) and GND and stabilize the output level of the operational amplifier. Adjust the capacitance value of the stabilized capacitor after the LCD panel has been mounted and the screen quality has been confirmed.



Notes:
1. The reference voltage input (Vci) must be adjusted so that the output voltage after boosting will not exceed the absolute maximum rating for the liquid-crystal power supply voltage (16.5 V).
2. Vci is both a reference voltage and power supply for the step-up circuit; the sufficient current must be obtained.
3. Polarized capacitors must be connected correctly.
4. Circuits for temperature compensation should be based on the sample circuits in figures 53 and 54.
5. Adjust the capacitance value of the stabilized capacitor after the LCD panel has been mounted.
6. The breakdown voltages of the capacitors connected to C3+/C3– and C6+/C6– should be three times or higher than the Vci voltage.
7. The breakdown voltages of the capacitors connected to C1+/C1–, C2+/C2–, C4+/C4–, and C5+/C5– should be equal to or higher than the Vci voltage.
8. The breakdown voltages of the capacitors connected to VLOUT and V1OUT through V5OUT should be n times or higher than the Vci voltage (n: step-up magnification).
9. Determine thebreakdown voltages of the capacitors used in 6 to 8 above by checking Vci voltage fluctuation.

Figure 52 Internal Step-up Circuit for LCD Drive Voltage Generation

Temperature can be compensated either through the CT bits, by controlling the reference input voltage for the VLCD regulator (VREG pin) using a thermistor, or by controlling the reference output voltage of the VLCD regulator (V1REF pin).

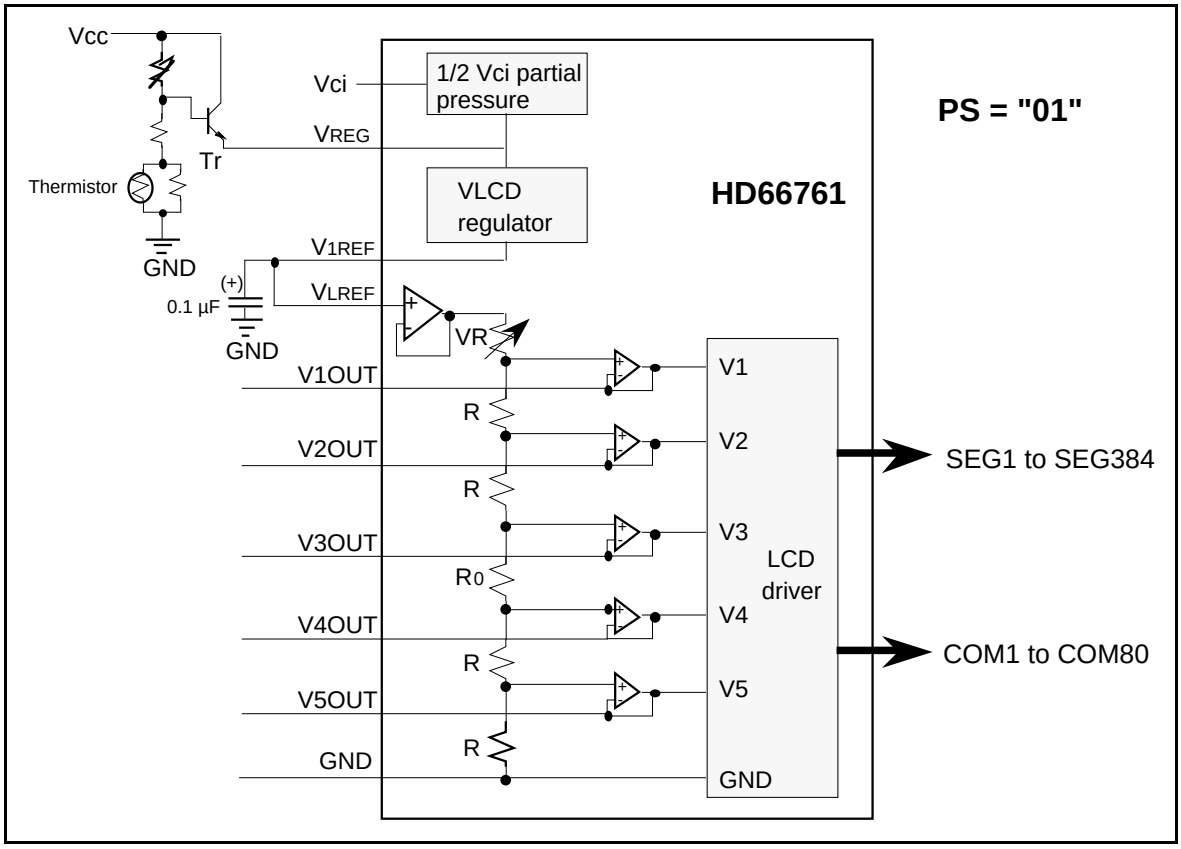


Figure 53 Temperature Compensation Circuits (1)

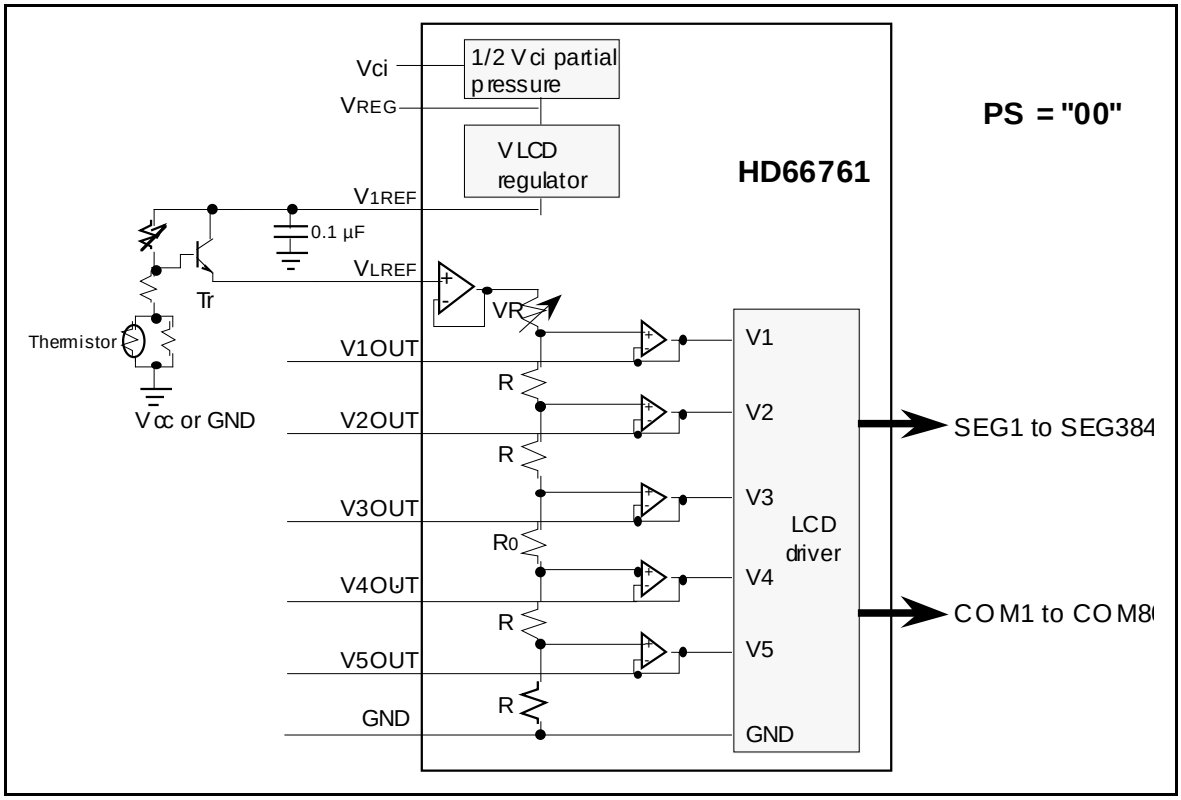


Figure 54 Temperature Compensation Circuits (2)

Switching the Step-up Factor

Instruction bits (BT1/0 bits) can optionally select the step-up factor of the internal step-up circuit. According to the display status, power consumption can be reduced by changing the LCD drive duty and the LCD drive bias, and by controlling the step-up factor for the minimum requirements. For details, see the Partial-display-on Function section.

According to the maximum step-up factor, external capacitors need to be connected. For example, when the maximum step-up is six times or five times, capacitors between C6+ and C6– or between C5+ and C5– are needed as in the case of the seven-times step-up.

Place a capacitor with a breakdown voltage of three times or more the Vci-GND voltage between C6+ and C6– and between C3+ and C3–, a capacitor with a breakdown voltage larger than the Vci-GND voltage between C1+ and C1–, C2+ and C2–, C4+ and C4–, and C5+ and C5–, and a capacitor with a breakdown voltage of n times or more the Vci-GND voltage to VLOUT (n: step-up factor) (see figure 55).

Note: Determine the capacitor breakdown voltages by checking Vci voltage fluctuation.

Table 36 VLOUT Output Status

BT1	BT0	VLOUT Output Status
0	0	Four-times step-up output
0	1	Five-times step-up output
1	0	Six-times step-up output
1	1	Seven-times step-up output

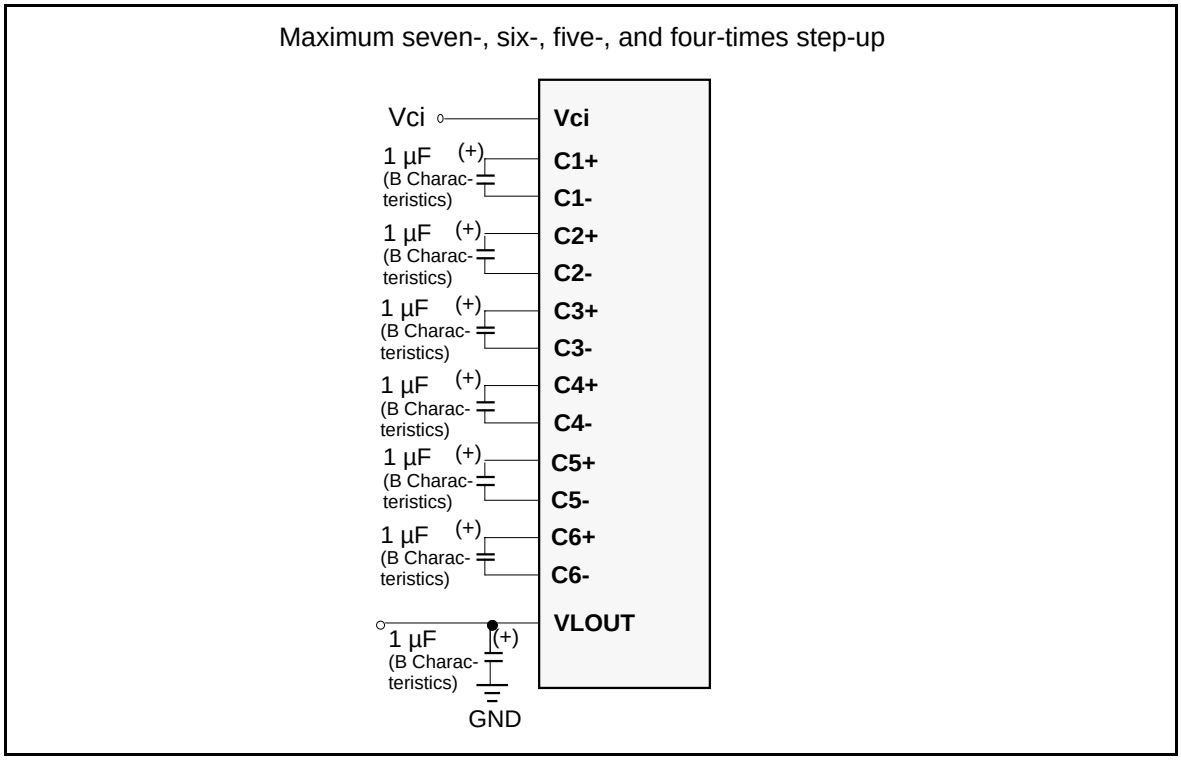


Figure 55 Step-up Circuit Output Factor Switching

Example of Power-supply Voltage Generator for More Than Seven-times Step-up Output

The HD66761 incorporates a step-up circuit for up to seven-times step-up. However, the LCD drive voltage (VLCD) will not be enough for seven-times step-up from Vcc when the power-supply voltage of Vcc is low or when the LCD drive voltage is high for the high-contrast LCD display. In this case, the reference voltage (Vci) for step-up can be set higher than the power-supply voltage of Vcc.

Set the Vci input voltage for the step-up circuit to 3.6 V or less within the range of Vcc + 1.0 V. Control the Vci voltage so that the step-up output voltage (VLOUT) should be less than the absolute maximum ratings (16.5 V).

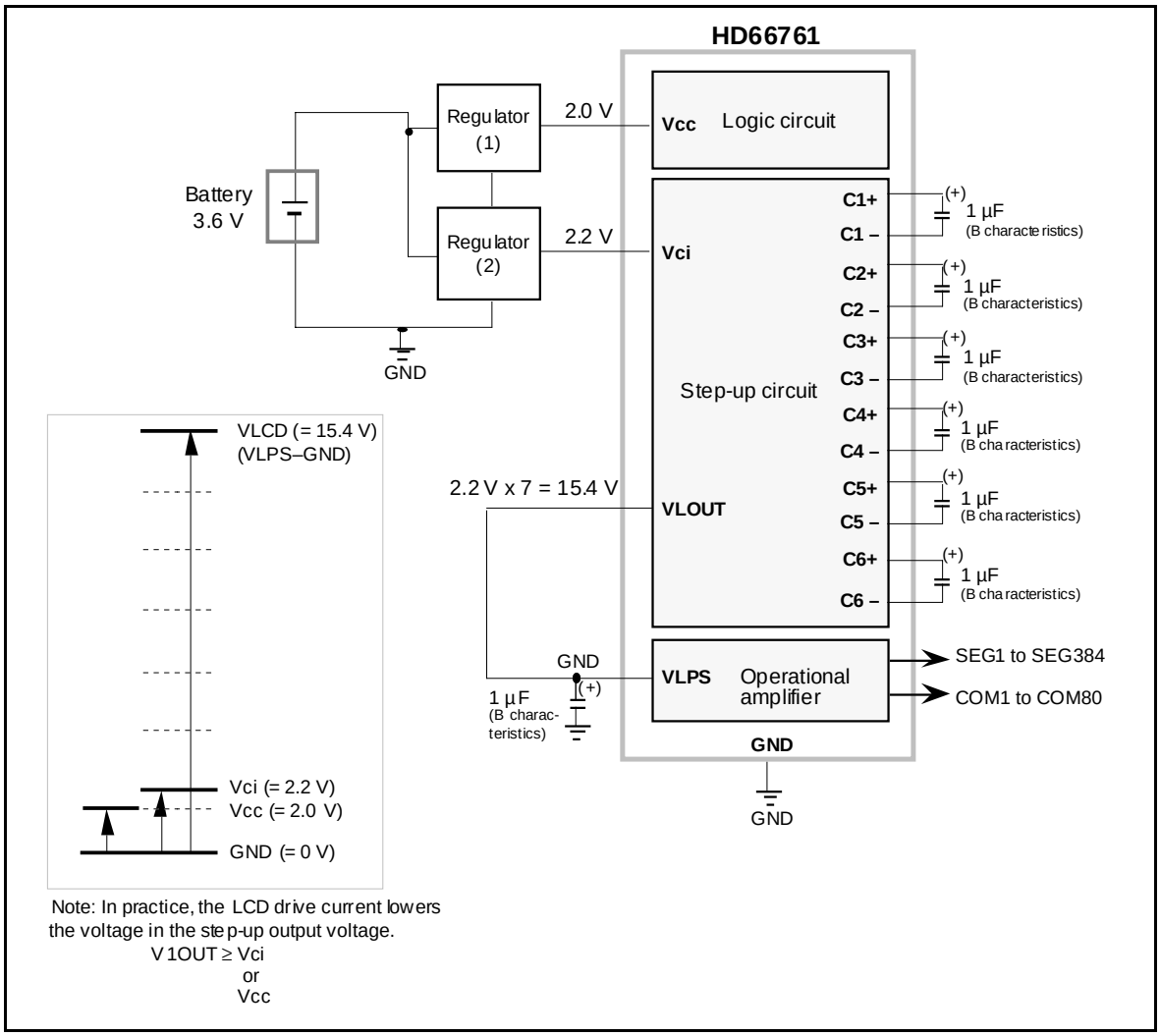


Figure 56 Usage Example of Step-up Circuit at Vci > Vcc

Restrictions on the 1st/2nd Screen Driving Position Register Settings

The following restrictions must be satisfied when setting the start line (SS16-10) and end line (SE16-10) of the 1st screen driving position register (R14) and the start line (SS26-20) and end line (SE26-20) of the 2nd screen driving position register (R15) for the HD66761. Note that incorrect display may occur if the restrictions are not satisfied.

Table 37 Restrictions on the 1st/2nd Screen Driving Position Register Settings

	1st Screen Driving (STP = 0)	2nd Screen Driving (STP = 1)
Register setting	SS16-10 ≤ SE16-0 ≤ 4FH	SS16-10 ≤ SE16-10 < SS26-20 ≤ SE26-20 ≤ 4FH
Display operation	• Time-sharing driving for COM pins (SS1+1) to (SE1+1) • Non-selection level driving for others	• Time-sharing driving for COM pins (SS1+1) to (SE1+1) and (SS2+1) to (SE2+1) • Non-selection level driving for others

Notes: 1. When the total line count in screen division driving settings is less than the duty setting, non-selection level driving is performed without the screen division driving setting range.
2. When the total line count in screen division driving settings is larger than the duty setting, the start line, the duty-setting line, and the lines between them are displayed and non-selection level driving is performed for other lines.
3. For the 1st screen driving, the SS26-20 and SE26-20 settings are ignored.

Sleep Mode

Setting the sleep mode bit (SLP) to 1 puts the HD66761 in the sleep mode, where the device stops all internal display operations, thus reducing current consumption. Specifically, LCD operation is completely halted. Here, all the SEG (SEG1 to SEG384) and COM (COM1 to COM132) pins output the GND level, resulting in no display. If the AP1-0 bits in the power control register are set to 00 in the sleep mode, the LCD drive power supply can be turned off, reducing the total current consumption of the LCD module.

Since master/slave signals (M, FLM, CL1, and CL2) are stopped during multi-chip operation, set the sleep mode on the slave side.

Table 38 Comparison of Sleep Mode and Standby Mode

Function	Sleep Mode (SLP = 1)	Standby Mode (STB = 1)
LCD control	Turned off	Turned off
R-C oscillation circuit	Operates normally	Operation stopped
Master/slave signal	Stopped	Stopped

Standby Mode

Setting the standby mode bit (STB) to 1 puts the HD66761 in the standby mode, where the device stops completely, halting all internal operations including the R-C oscillation circuit, thus further reducing current consumption compared to that in the sleep mode. Specifically, all the SEG (SEG1 to SEG384) and COM (COM1 to COM80) pins for the time-sharing drive output the GND level, resulting in no display. If the AP1-0 bits are set to 00 in the standby mode, the LCD drive power supply can be turned off.

During the standby mode, no instructions can be accepted other than the start-oscillation instruction. To cancel the standby mode, issue the start-oscillation instruction to stabilize R-C oscillation before setting the STB bit to 0.

During multi-chip operation, set the standby mode on the slave side.

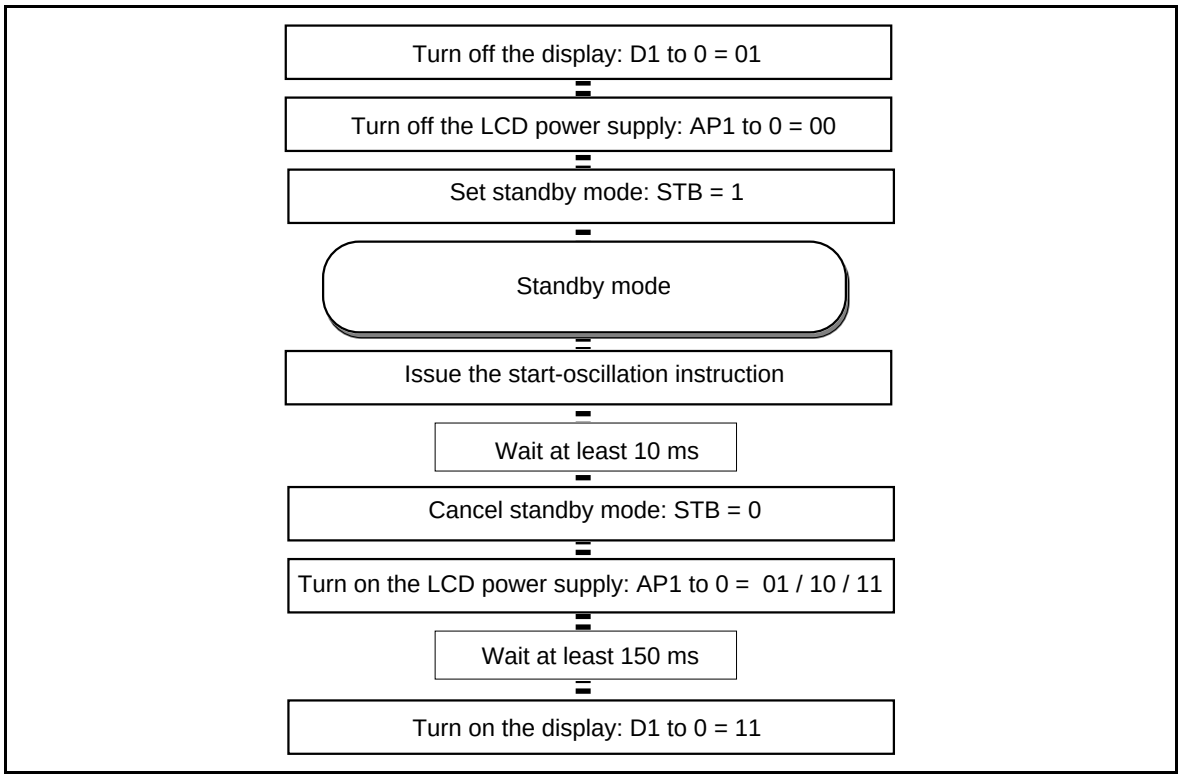


Figure 58 Procedure for Setting and Canceling Standby Mode

Power-on/off Sequence

To prevent pulse lighting of LCD screens at power-on/off, the power-on/off sequence is activated as shown below. However, since the sequence depends on LCD materials to be used, confirm the conditions by using your own system.

Power-on Sequence

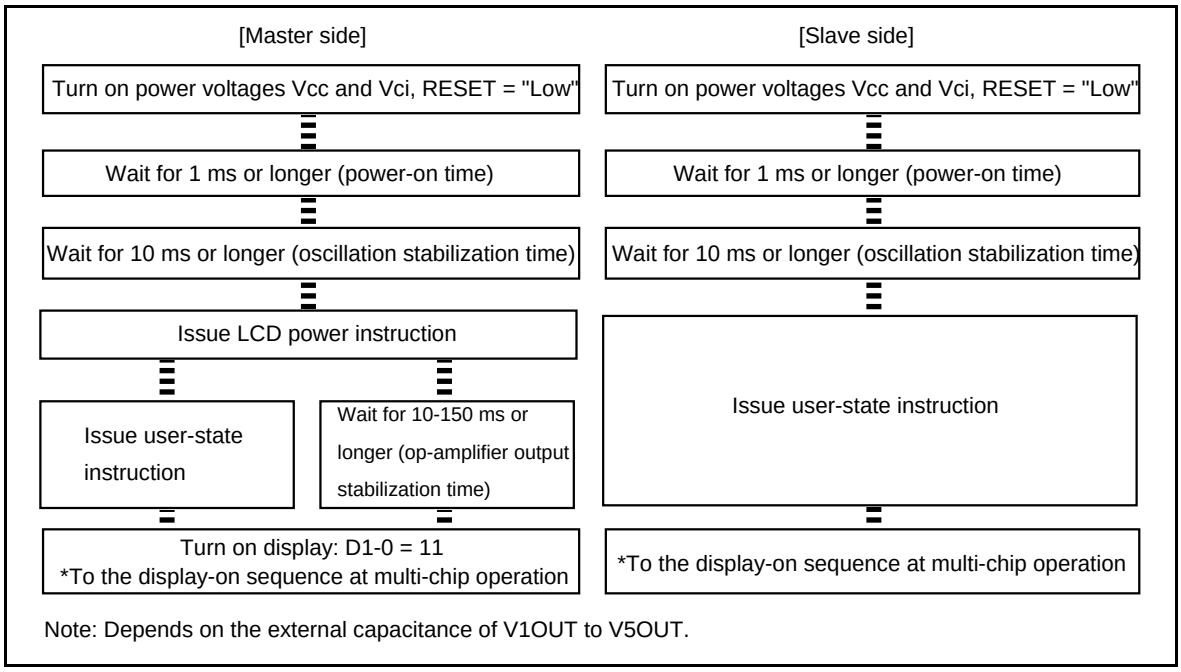


Figure 59 Power-on Sequence

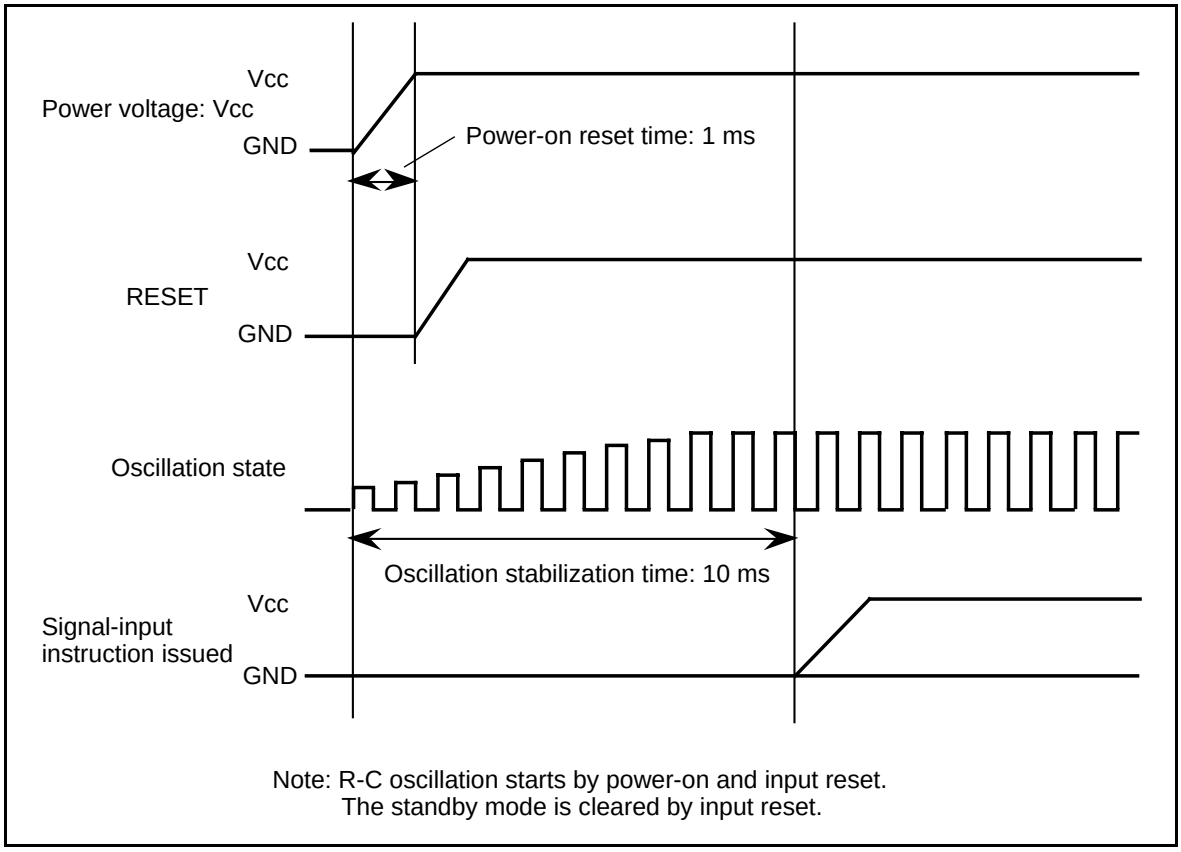


Figure 60 Power-on Timing

Power-off Sequence

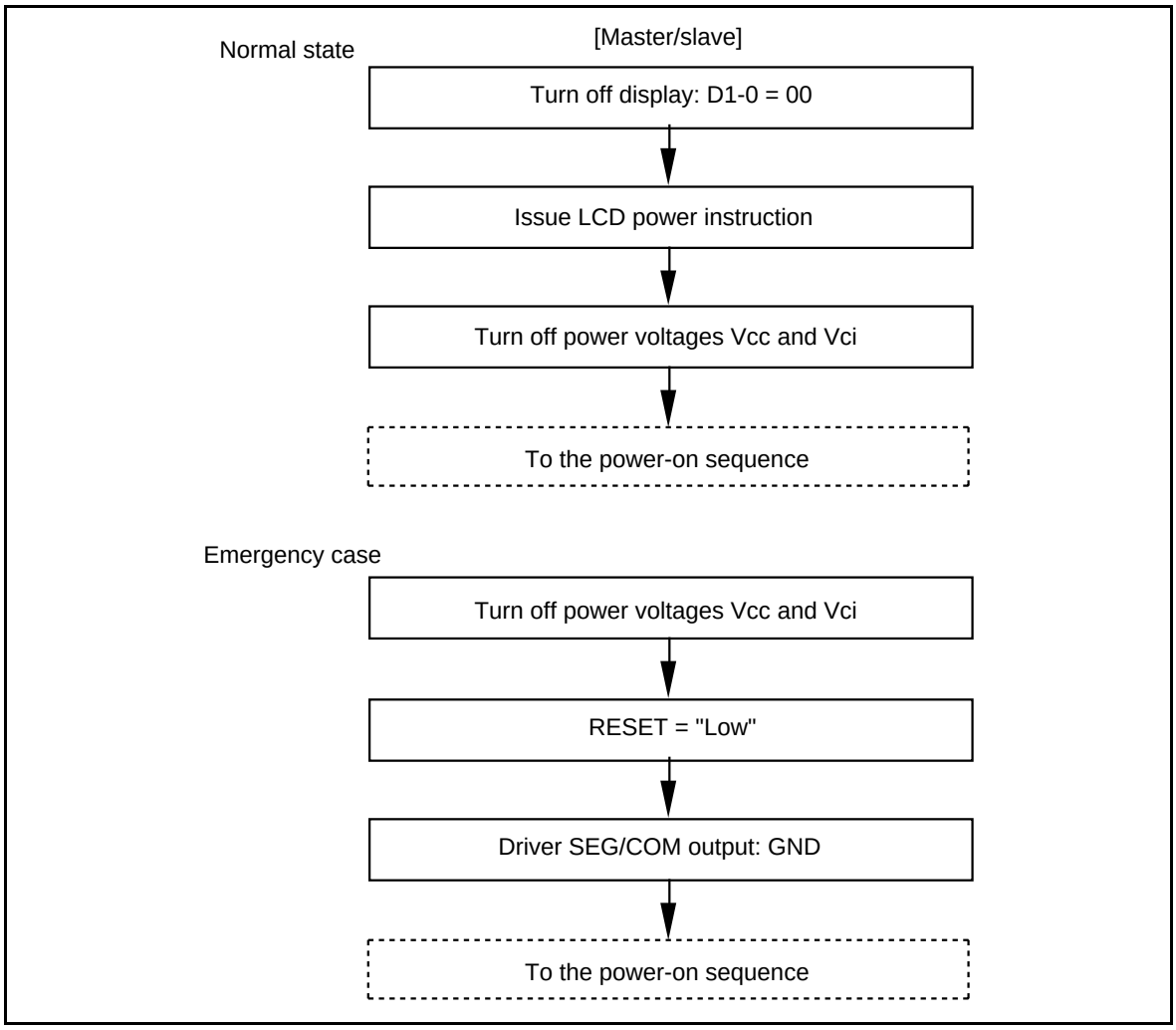
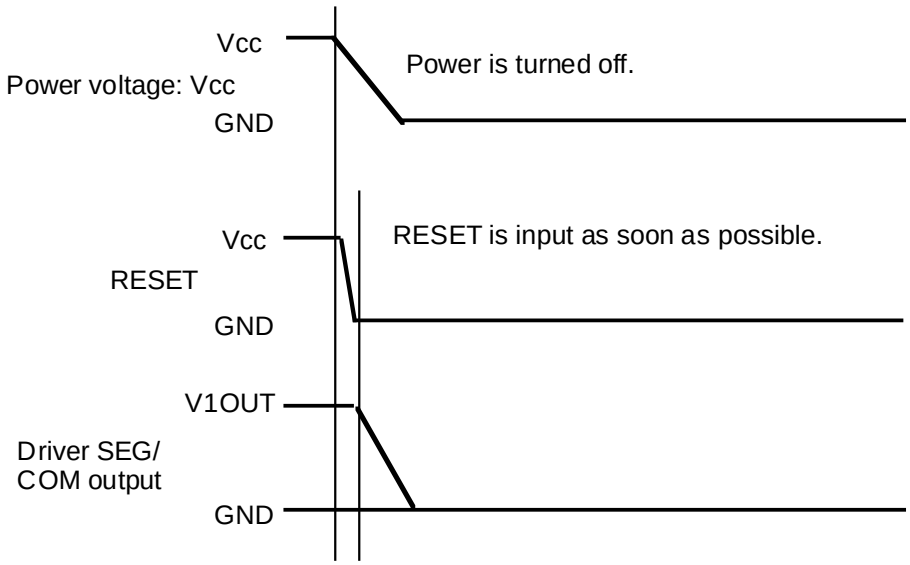


Figure 61 Power-off Sequence



Note: When hardware reset is input during the power-off period, the D bit is cleared to 0 and SEG/COM output is forcibly lowered to the GND level.

Figure 62 Power-off Timing

Absolute Maximum Ratings

Item	Symbol	Unit	Value	Notes*
Power supply voltage (1)	V_{CC}	V	–0.3 to +4.6	1, 2
Power supply voltage (2)	V_{LCD} – GND	V	–0.3 to +16.5	1, 3
Input voltage	Vt	V	–0.3 to V_{CC} + 0.3	1
Operating temperature	Topr	°C	–40 to +85	1, 4
Storage temperature	Tstg	°C	–55 to +110	1, 5

Notes: 1. If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristics limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.
2. VCC ≥ GND must be maintained.
3. VLCD ≥ GND must be maintained.
4. For bare die and wafer products, specified up to 85˚C.
5. This temperature specifications apply to the TCP package.

DC Characteristics (V_{CC} = 2.2 to 3.6 V, Ta = –40 to +85°C*[1])

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	0.7 V_{CC}	—	V_{CC}	V	V_{CC} = 2.2 to 3.6 V	2, 3
Input low voltage	V_{IL}	–0.3	—	0.15 V_{CC}	V	V_{CC} = 2.2 to 3.6 V	2, 3
Output high voltage (1) (DB0-15 pins)	V_{OH1}	0.75 V_{CC}	—	—	V	I_{OH} = –0.1 mA	2
Output low voltage (1) (DB0-15 pins)	V_{OL1}	—	—	0.2 V_{CC}	V	V_{CC} = 2.2 to 2.4 V, I_{OL} = 0.1 mA	2
		—	—	0.15 V_{CC}	V	V_{CC} = 2.4 to 3.6 V, I_{OL} = 0.1 mA	2
Driver ON resistance (COM pins)	R_{COM}	—	3	10	kΩ	±Id = 0.05 mA, V_{LCD} = 10 V	4
Driver ON resistance (SEG pins)	R_{SEG}	—	3	10	kΩ	±Id = 0.05 mA, V_{LCD} = 10 V	4
I/O leakage current	I_{Li}	–1	—	1	µA	Vin = 0 to V_{CC}	5
Current consumption during normal operation (V_{CC} – GND)	I_{OP}	—	T.B.D.	T.B.D.	µA		6, 7
Current consumption during sleep mode (V_{CC} – GND)	I_{SL}	—	T.B.D.	—	µA		6, 7
Current consumption during standby mode (V_{CC} – GND)	I_{ST}	—	T.B.D.	T.B.D.	µA	V_{CC} = 3 V, Ta = 25°C	6, 7
LCD drive power supply current (V_{LPS} – GND)	I_{LCD}	—	T.B.D.	T.B.D.	µA		7
LCD drive voltage (V_{LPS} – GND)	V_{LCD}	5.0	—	15.5	V		8
VREG input voltage (VREG pin)	V_{REG}	T.B.D.	T.B.D.	T.B.D.	V		
V1REF output voltage (V1REF pin)	V_{1REF}	T.B.D.	T.B.D.	T.B.D.	V		

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

Step-up Circuit Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Four-times step-up output voltage (VLOUT pin)	V_{UP4}	10.3	10.6	10.8	V	V_{CC} = Vci = 2.7 V, I_O = 30 µA, C = 1 µF, f_{OSC} = 180 kHz, Ta = 25°C	11
Five-times step-up output voltage (VLOUT pin)	V_{UP5}	13	13.3	13.5	V	V_{CC} = Vci = 2.7 V, I_O = 30 µA, C = 1 µF, f_{OSC} = 180 kHz, Ta = 25°C	11
Six-times step-up output voltage (VLOUT pin)	V_{UP6}	12.7	12.9	13.2	V	V_{CC} = Vci = 2.2 V, I_O = 30 µA, C = 1 µF, f_{OSC} = 180 kHz, Ta = 25°C	11
Seven-times step-up output voltage (VLOUT pin)	V_{UP7}	13.9	15.1	15.4	V	V_{CC} = Vci = 2.2 V, I_O = 30 µA, C = 1 µF, f_{OSC} = 180 kHz, Ta = 25°C	11
Use range of step-up output voltages	V_{UP4} V_{UP5} V_{UP6} V_{UP7}	Vcc	—	15.5	V	For four- to seven-times step-up	11

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 2.2 to 3.6 V, Ta = –40 to +85°C*[1])

Clock Characteristics (V_{CC} = 2.2 to 3.6 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
External clock frequency	fcp	T.B.D.	180	T.B.D.	kHz	V_{CC} = 2.2 to 3.6 V	9
External clock duty ratio	Duty	45	50	55	%	V_{CC} = 2.2 to 3.6 V	9
External clock rise time	trcp	—	—	0.2	µs	V_{CC} = 2.2 to 3.6 V	9
External clock fall time	tfcp	—	—	0.2	µs	V_{CC} = 2.2 to 3.6 V	9
R-C oscillation clock	f_{OSC}	T.B.D.	180	T.B.D.	kHz	Rf = kΩ, V_{CC} = 3 V	10

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

68-system Bus Interface Timing Characteristics

(Vcc = 2.2 to 2.4 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	t_{CYCE}	600	—	—	ns	Figure 70
	Read	t_{CYCE}	800	—	—		
Enable high-level pulse width	Write	PW_{EH}	120	—	—	ns	Figure 70
	Read	PW_{EH}	350	—	—		
Enable low-level pulse width	Write	PW_{EL}	300	—	—	ns	Figure 70
	Read	PW_{EL}	400	—	—		
Enable rise/fall time		t_{Er}, t_{Ef}	—	—	25	ns	Figure 70
Setup time (RS, R/W to E, CS*)		t_{ASE}	50	—	—	ns	Figure 70
Address hold time		t_{AHE}	20	—	—	ns	Figure 70
Write data setup time		t_{DSWE}	60	—	—	ns	Figure 70
Write data hold time		t_{HE}	20	—	—	ns	Figure 70
Read data delay time		t_{DDRE}	—	—	300	ns	Figure 70
Read data hold time		t_{DHRE}	5	—	—	ns	Figure 70

(Vcc = 2.4 to 3.6 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	t_{CYCE}	300	—	—	ns	Figure 70
	Read	t_{CYCE}	500	—	—		
Enable high-level pulse width	Write	PW_{EH}	70	—	—	ns	Figure 70
	Read	PW_{EH}	250	—	—		
Enable low-level pulse width	Write	PW_{EL}	100	—	—	ns	Figure 70
	Read	PW_{EL}	200	—	—		
Enable rise/fall time		t_{Er}, t_{Ef}	—	—	25	ns	Figure 70
Setup time (RS, R/W to E, CS*)		t_{ASE}	50	—	—	ns	Figure 70
Address hold time		t_{AHE}	5	—	—	ns	Figure 70
Write data setup time		t_{DSWE}	60	—	—	ns	Figure 70
Write data hold time		t_{HE}	15	—	—	ns	Figure 70
Read data delay time		t_{DDRE}	—	—	200	ns	Figure 70
Read data hold time		t_{DHRE}	5	—	—	ns	Figure 70

80-system Bus Interface Timing Characteristics

(Vcc = 2.2 to 2.4 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write	t_{CYCW}	600	—	—	ns	Figure 71
	Read	t_{CYCR}	800	—	—	ns	Figure 71
Write low-level pulse width		PW_{LW}	120	—	—	ns	Figure 71
Read low-level pulse width		PW_{LR}	350	—	—	ns	Figure 71
Write high-level pulse width		PW_{HW}	300	—	—	ns	Figure 71
Read high-level pulse width		PW_{HR}	400	—	—	ns	Figure 71
Write/Read rise/fall time		t_{WRr} , $_{WRf}$	—	—	25	ns	Figure 71
Setup time (RS to CS*, WR*, RD*)		t_{AS}	50	—	—	ns	Figure 71
Address hold time		t_{AH}	20	—	—	ns	Figure 71
Write data setup time		t_{DSW}	60	—	—	ns	Figure 71
Write data hold time		t_{H}	20	—	—	ns	Figure 71
Read data delay time		t_{DDR}	—	—	300	ns	Figure 71
Read data hold time		t_{DHR}	5	—	—	ns	Figure 71

(Vcc = 2.4 to 3.6 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write	t_{CYCW}	300	—	—	ns	Figure 71
	Read	t_{CYCR}	500	—	—	ns	Figure 71
Write low-level pulse width		PW_{LW}	70	—	—	ns	Figure 71
Read low-level pulse width		PW_{LR}	250	—	—	ns	Figure 71
Write high-level pulse width		PW_{HW}	100	—	—	ns	Figure 71
Read high-level pulse width		PW_{HR}	200	—	—	ns	Figure 71
Write/Read rise/fall time		$t_{WRr, WRf}$	—	—	25	ns	Figure 71
Setup time (RS to CS*, WR*, RD*)		t_{AS}	50	—	—	ns	Figure 71
Address hold time		t_{AH}	5	—	—	ns	Figure 71
Write data setup time		t_{DSW}	60	—	—	ns	Figure 71
Write data hold time		t_{H}	15	—	—	ns	Figure 71
Read data delay time		t_{DDR}	—	—	200	ns	Figure 71
Read data hold time		t_{DHR}	5	—	—	ns	Figure 71

Reset Timing Characteristics (V_{CC} = 2.2 to 3.6 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reset low-level width	t_{RES}	1	—	—	ms	Figure 72

Electrical Characteristics Notes

1. For bare die and wafer products, specified up to 85˚C.
2. The following three circuits are I/O pin configurations (figure 63).

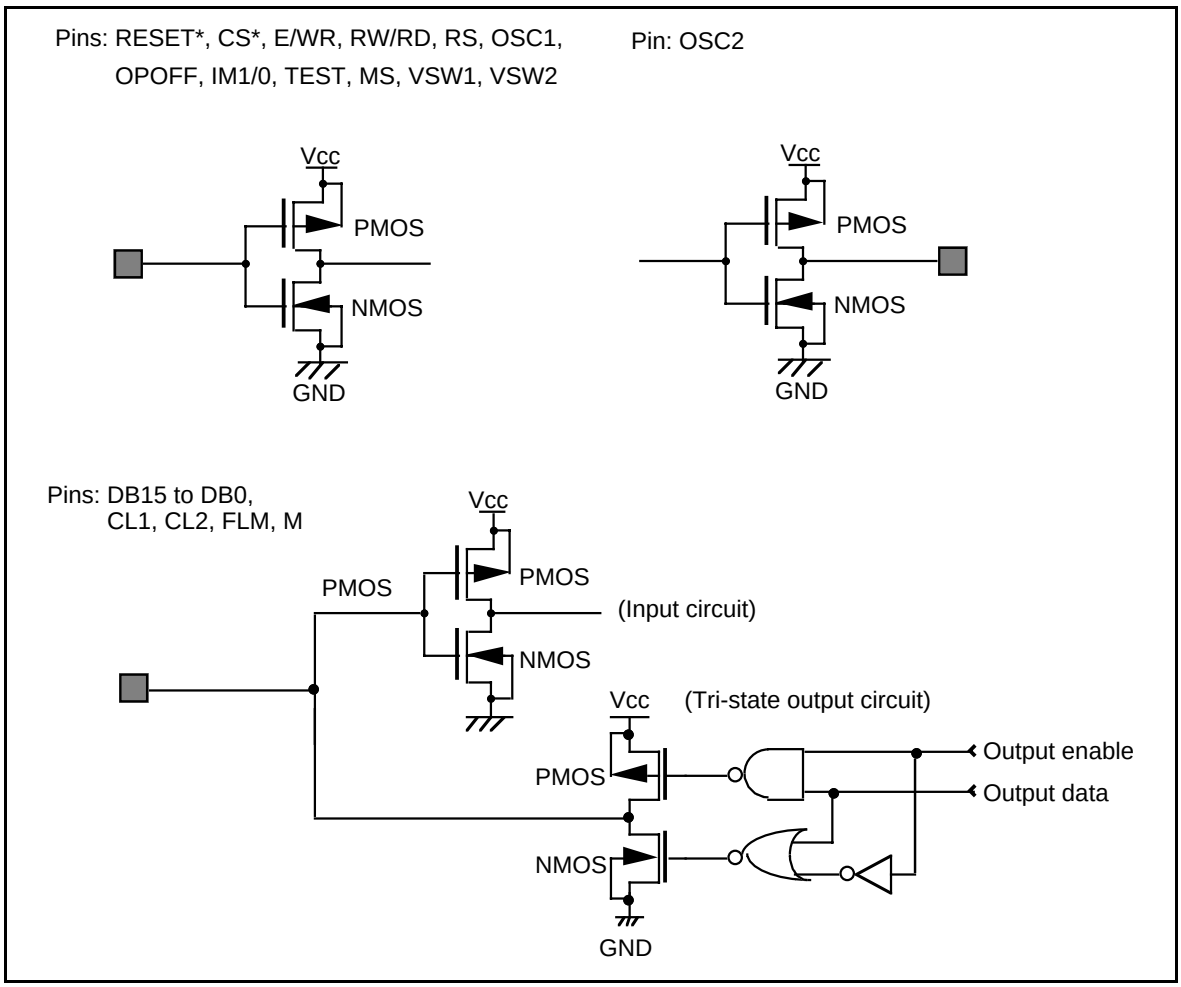


Figure 63 I/O Pin Configuration

3. The TEST, VSW1, and VSW2 pins must be grounded and the IM1/0, OPOFF, and MS pins must be grounded or connected to Vcc.
4. Applies to the resistor value (RCOM) between power supply pins V1OUT, V2OUT, V5OUT, GND and common signal pins, and resistor value (RSEG) between power supply pins V1OUT, V3OUT, V4OUT, GND and segment signal pins.
5. This excludes the current flowing through output drive MOSs.
6. This excludes the current flowing through the input/output units. The input level must be fixed high or low because through current increases if the CMOS input is left floating. Even if the CS pin is low or high when an access with the interface pin is not performed, current consumption does not change.
7. The following shows the relationship between the operation frequency (fosc) and current consumption (Icc) (figure 64).

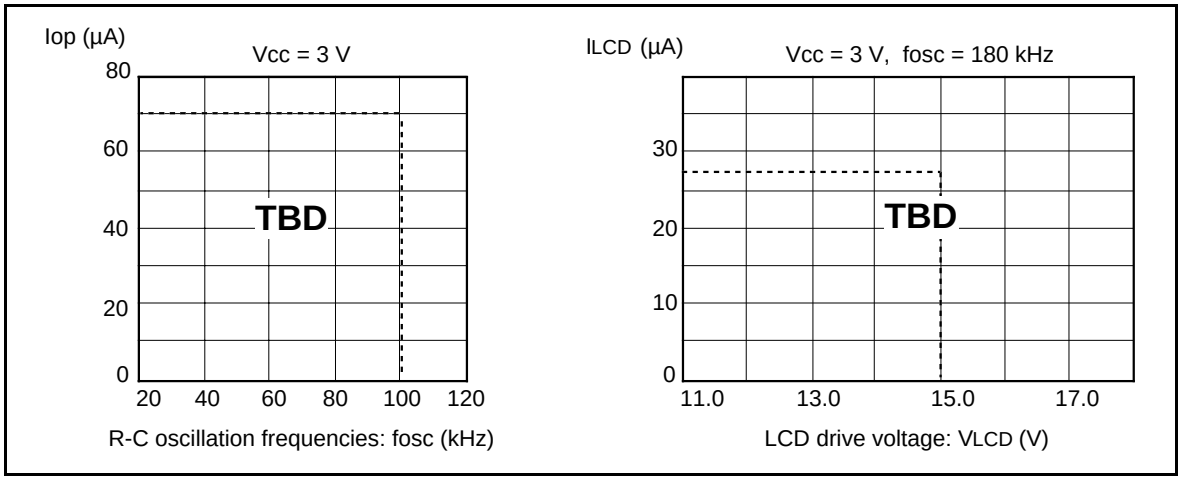


Figure 64 Relationship between the Operation Frequency and Current Consumption

8. Each COM and SEG output voltage is within ±0.15 V of the LCD voltage (Vcc, V1, V2, V3, V4, V5) when there is no load.
9. Applies to the external clock input (figure 65).

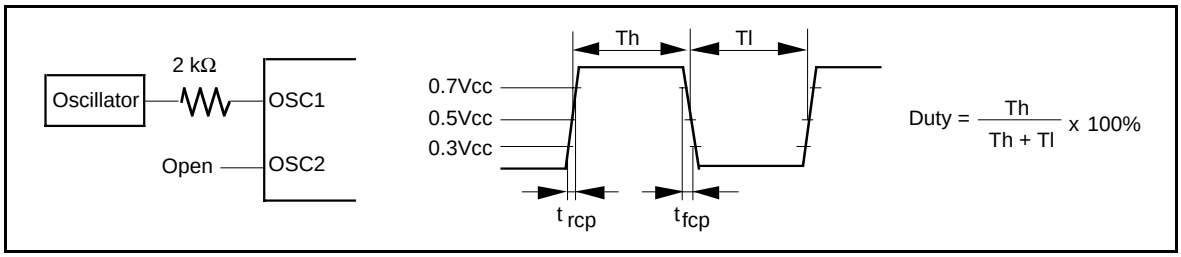
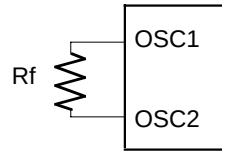


Figure 65 External Clock Supply

10. Applies to the internal oscillator operations using external oscillation resistor Rf (figure 66 and table 39).



Since the oscillation frequency varies depending on the OSC1 and OSC2 pin capacitance, the wiring length to these pins should be minimized.

Figure 66 Internal Oscillation

Table 39 External Resistance Value and R-C Oscillation Frequency (Referential Data)

External Resistance (Rf)	R-C Oscillation Frequency: fosc		
	Vcc = 2.2 V	Vcc = 3.0 V	Vcc = 3.6 V
200 kΩ			
270 kΩ			
300 kΩ			
330 kΩ			
360 kΩ			
390 kΩ			
430 kΩ			
470 kΩ			

11. The step-up characteristics test circuit is shown in figure 67.

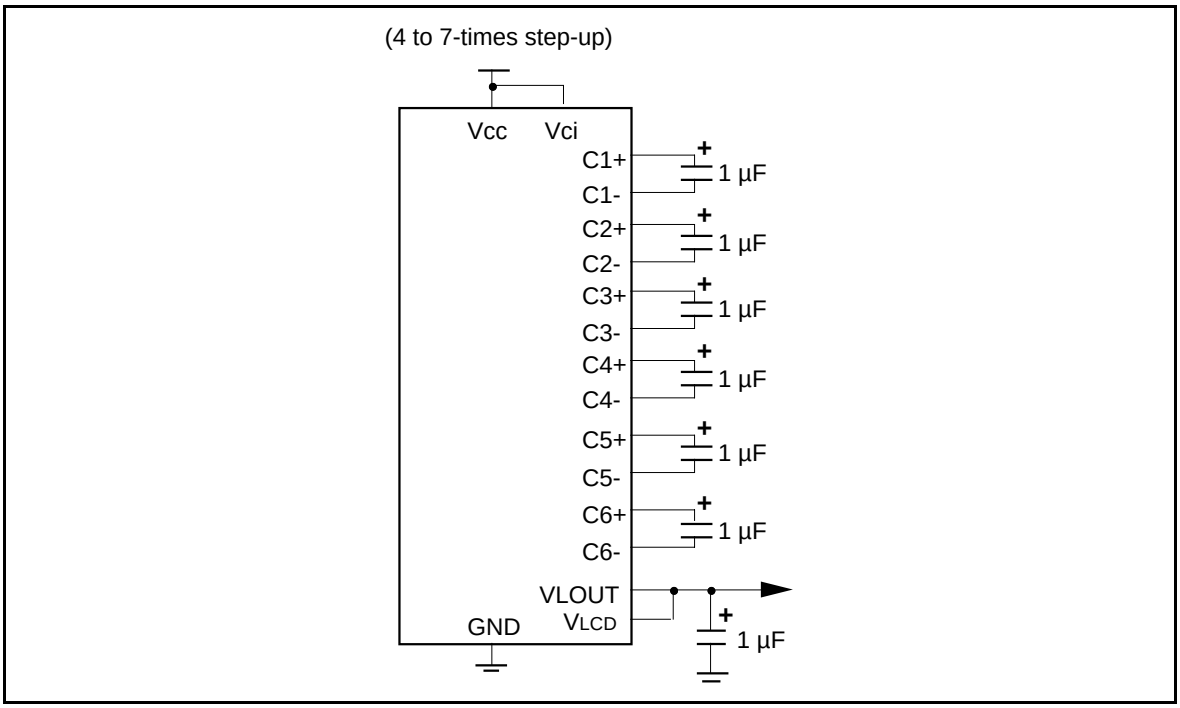


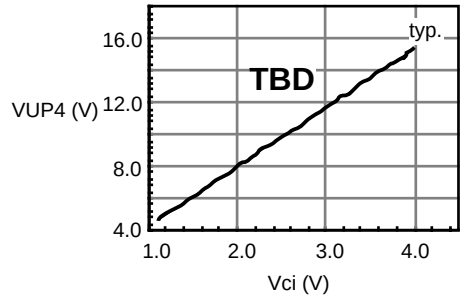
Figure 67 Step-up Characteristics Test Circuit

Referential data

VUP6 = VLCD - GND, VUP7 = VLCD - GND

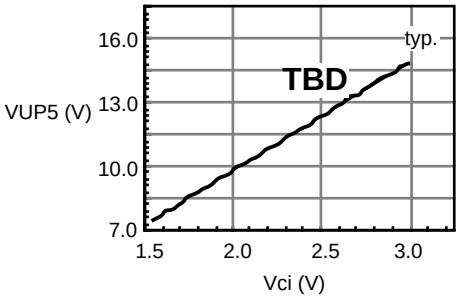
(i) Relation between the obtained voltage and input voltage

Four-times step-up



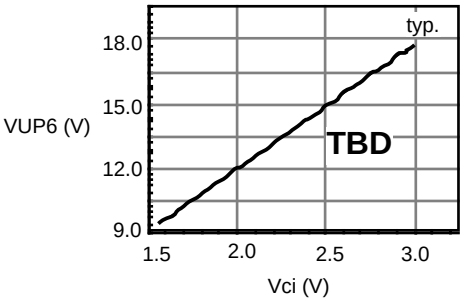
Vci = Vcc, fosc = 180 kHz, Ta = 25°C, DC1/0= 00

Five-times step-up



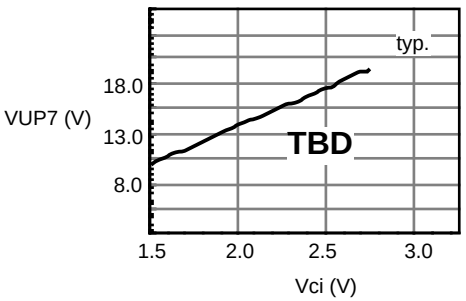
Vci = Vcc, fosc = 180 kHz, Ta = 25°C, DC1/0= 00

Six-times step-up



Vci = Vcc, fosc = 180 kHz, Ta = 25°C, DC1/0= 00

Seven-times step-up



Vci = Vcc, fosc = 180 kHz, Ta = 25°C, DC1/0= 00

Figure 68 Step-up

(ii) Relation between the obtained voltage and temperature

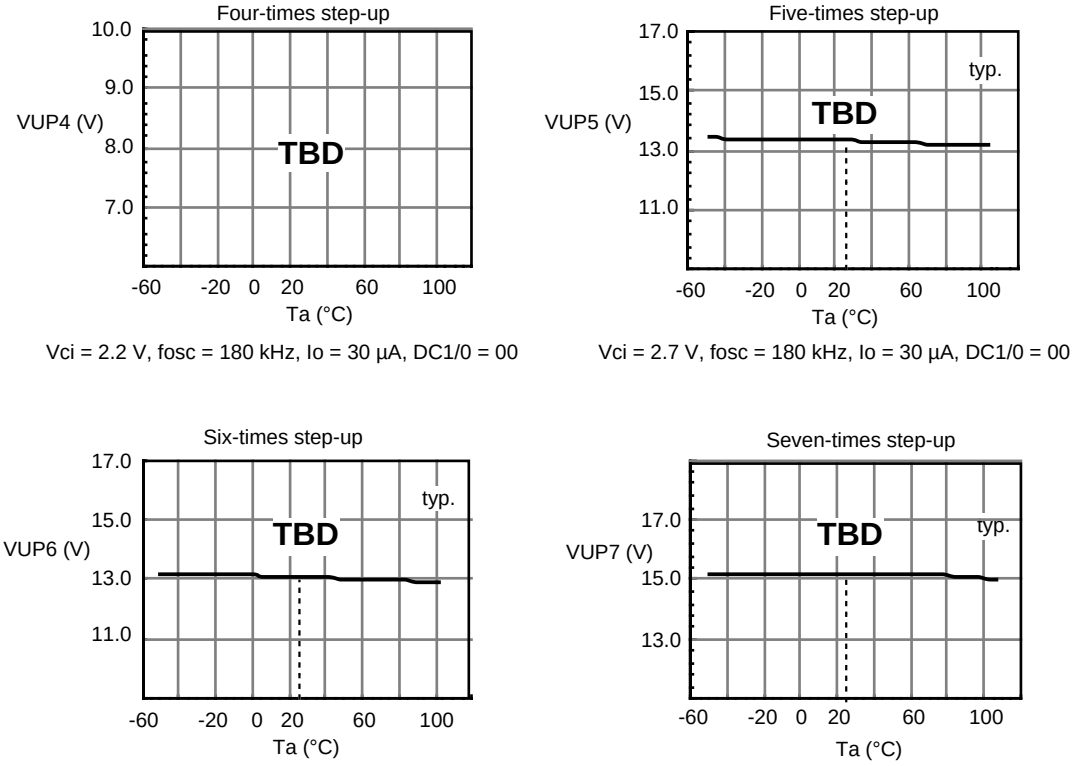
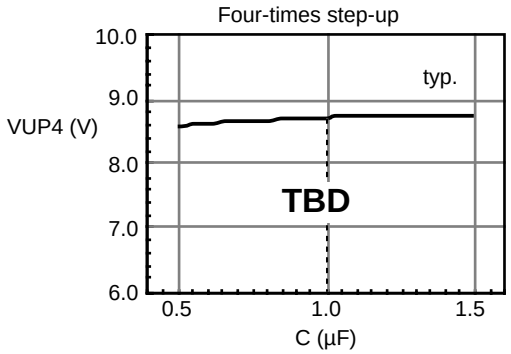
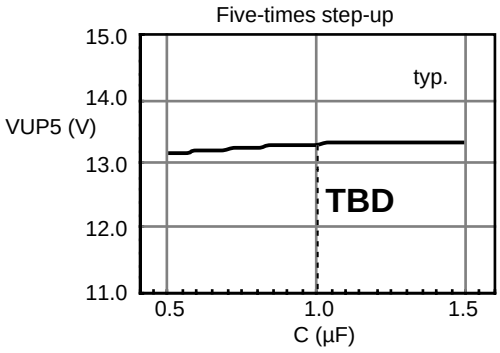


Figure 68 Step-up (cont)

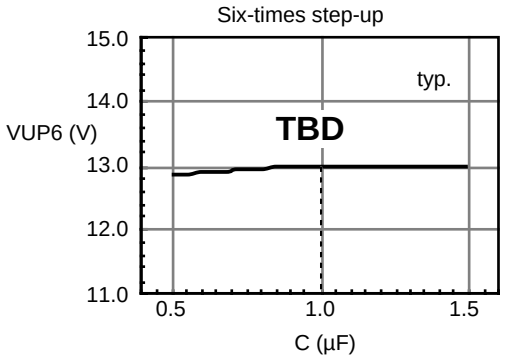
(iii) Relation between the obtained voltage and capacity



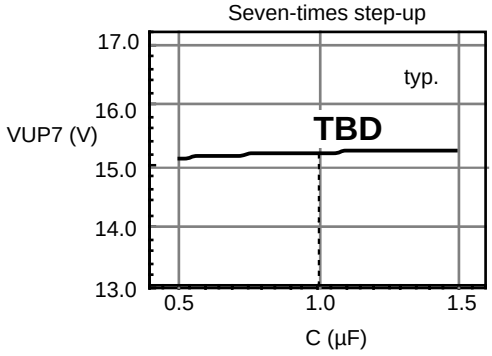
Vci = 2.2 V, fosc = 180 kHz, Io = 30 µA, DC1/0 = 00



Vci = 2.7 V, fosc = 180 kHz, Io = 30 µA, DC1/0 = 00



Vci = 2.2 V, fosc = 180 kHz, Io = 30 µA, DC1/0 = 00



Vci = 2.2 V, fosc = 180 kHz, Io = 30 µA, DC1/0 = 00

Figure 68 Step-up (cont)

(iv) Relation between the obtained voltage and current

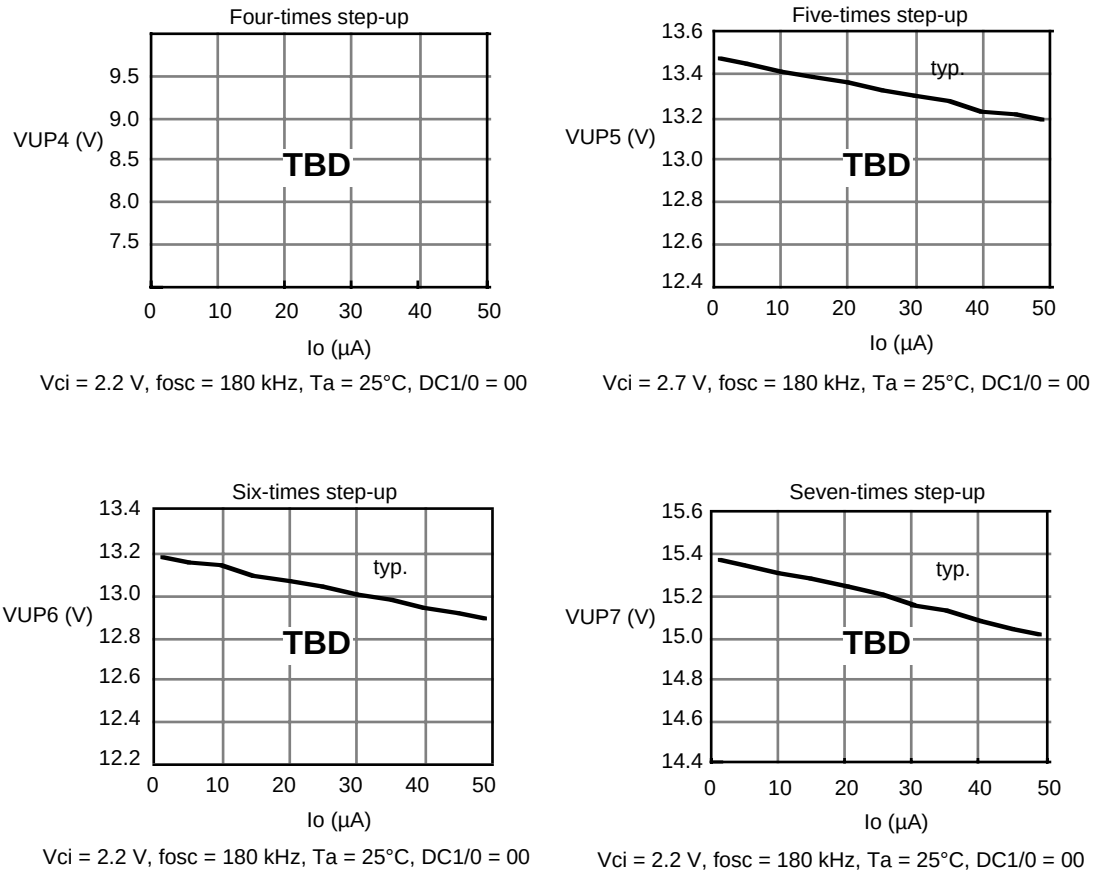


Figure 68 Step-up (cont)

Load Circuits

AC Characteristics Test Load Circuits

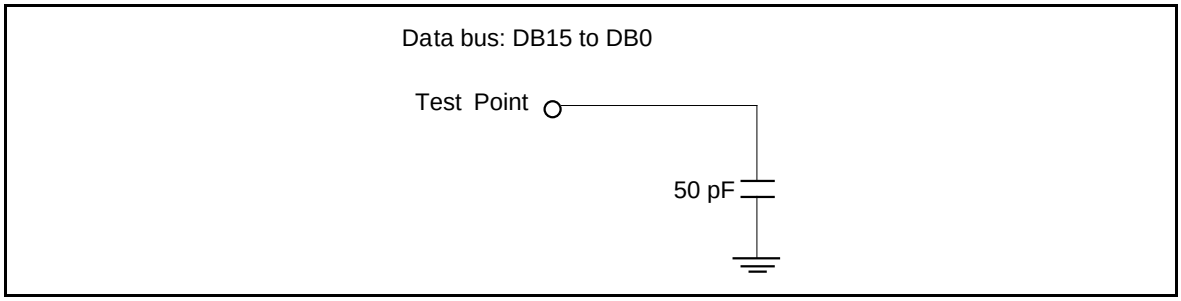
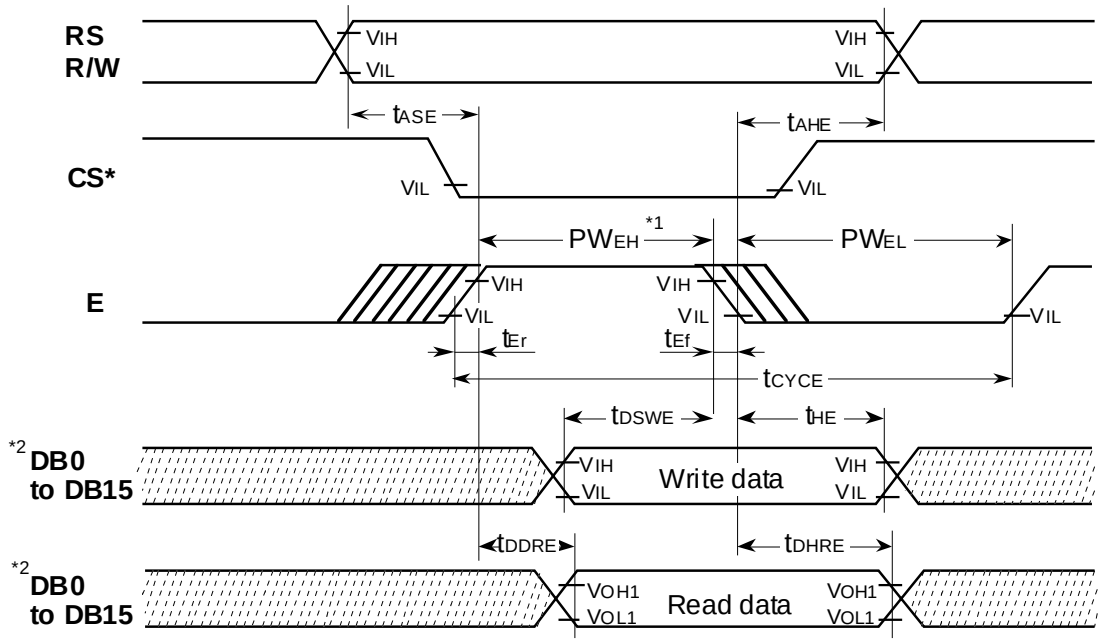


Figure 69 Load Circuit

Timing Characteristics

68-system Bus Operation



Notes: 1. PWEH is specified in the overlapped period when CS* is low and E is high.
2. Parallel data transfer is enabled on the DB15-8 pins when the 8-bit bus interface is used.
Fix the DB7-0 pins to Vcc or GND.

Figure 70 68-system Bus Timing

80-system Bus Operation

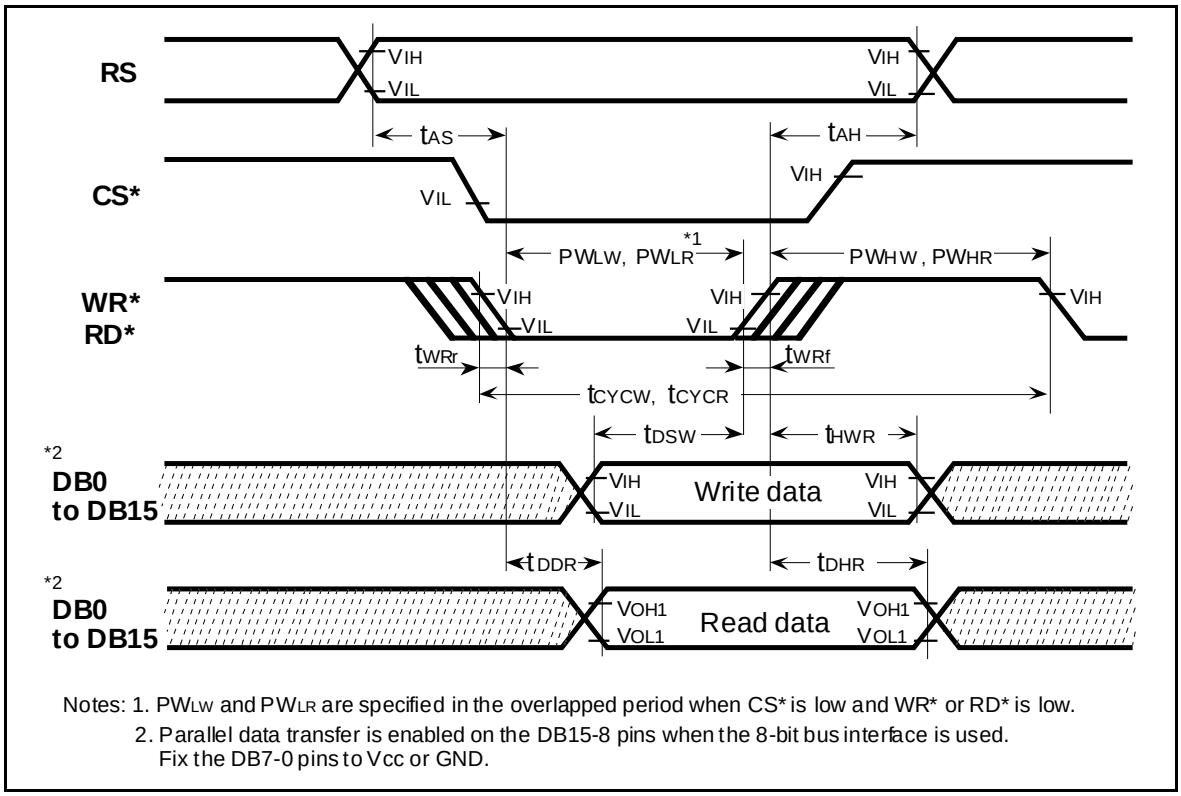


Figure 71 80-system Bus Timing

Reset Operation

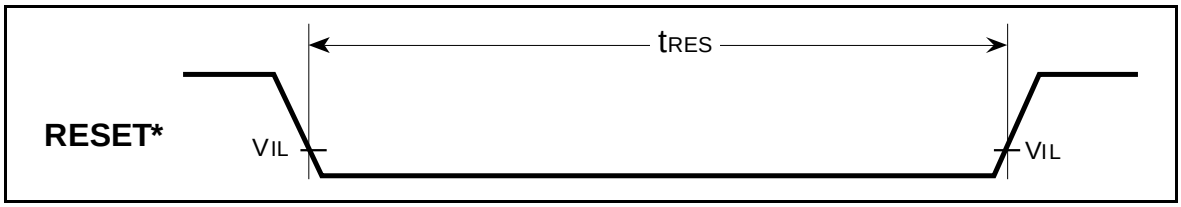


Figure 72 Reset Timing

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