# FLOPPY DISK CONTROLLER

## ■ DESCRIPTION

The SPC2052FOA is a floppy disk controller that interfaces directly to the IBM–PC/AT bus. It is fully compatible with the NEC μPD765 disk controller and supports all of the standard PC/AT (XT) disk controller commands.

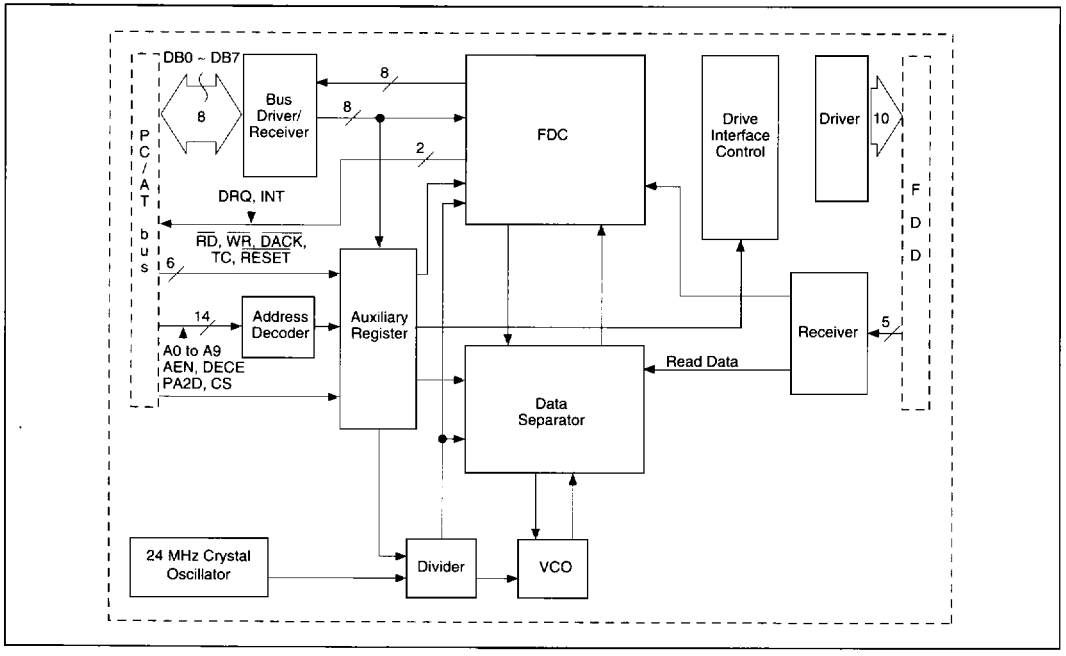
It incorporates a high-performance analog PLL data separator and high-current line drivers for the host and disk drive interfaces, minimizing the external support circuitry required.

The SPC2052FOA is available in 80-pin plastic flatpaks.

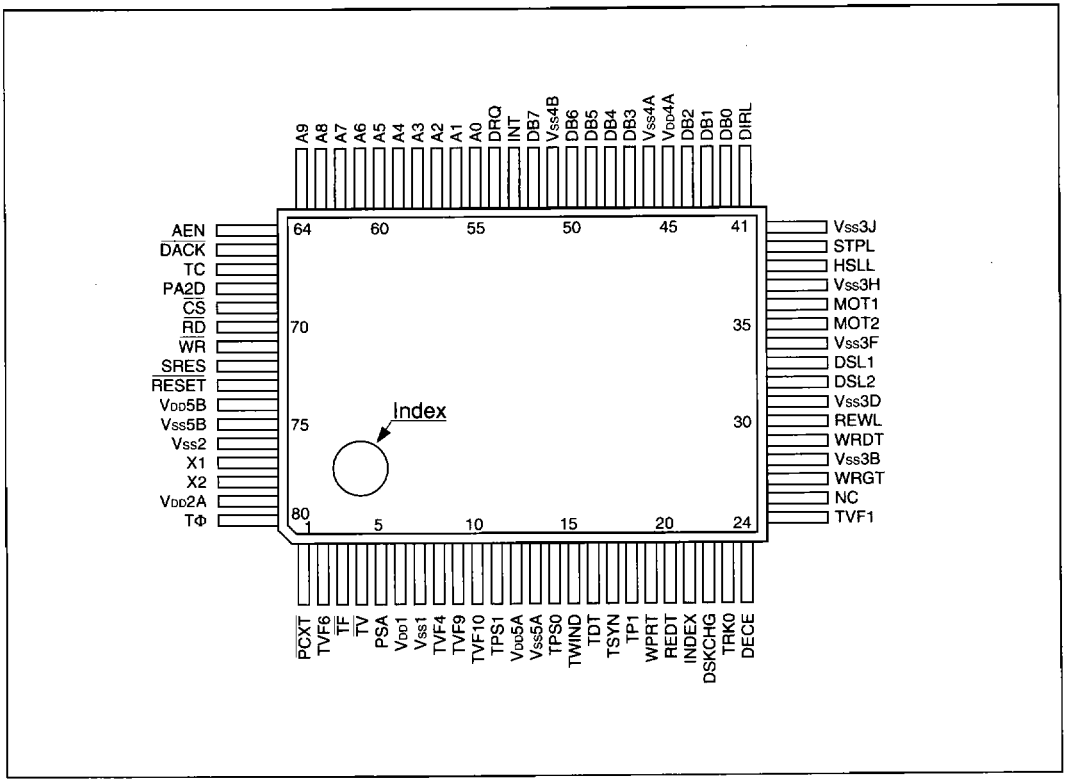
## ■ FEATURES

- Controls two floppy disk drives
- CRC generator/checker
- Data scanning function
- Can be recalibrated for up to 77 tracks
- Supports DMA and program data transfer
- Simultaneous seek operations on both disk drives
- Programmable data transfer rates of 250, 300, 500 kbps
- IBM/PC AT standard bus and command set
- On-chip adjustment-free analog PLL data separator
- 24 MHz crystal oscillator with feedback resistor and capacitor on-chip
- Supports both 5.25 and 3.5-inch floppy disks
- Chip select address decoder on address lines A0 to A9
- 12mA host bus drivers and 38 mA disk drive interface drivers
- Single +5V power supply
- 80-pin QFP flat plastic package
- CMOS technology

## ■ BLOCK DIAGRAM



## ■ PIN CONFIGURATION



## ■ PIN DESCRIPTION

### ● Host Interface

| Pin | | Type | Input/ Output | Description |
|---|---|---|---|---|
| Name | Number | | | |
| A0 to A9 | 55 to 64 | Schmitt | I | PC/AT bus address select inputs |
| DB0 to DB7 | 42 to 44, 47 to 50, 52 | TTL/Tri-state | I/O | PC/AT bus bi-directional tri-state data pins |
| $\overline{RD}$ | 70 | Schmitt | I | Active—LOW status or data read control signal from PC/AT bus |
| $\overline{WR}$ | 71 | Schmitt | I | Active—LOW command or data write signal from PC/AT bus |
| AEN | 65 | Schmitt | I | PC/AT bus address enable input. High during DMA transfer. |
| DRQ | 54 | Tri-state | O | Active—HIGH request to host for DMA transfer. |
| INT | 53 | Tri-state | O | Active—HIGH interrupt request to host indicates that servicing is required at completion of a command. |
| $\overline{DACK}$ | 66 | TTL input | I | Active—LOW DMA acknowledge from host |
| TC | 67 | TTL input | I | Active—HIGH data transfer complete signal from host |
| SRES | 72 | TTL input | I | Active—HIGH system reset signal from PC/AT bus |
| $\overline{RESET}$ | 73 | TTL input | I | Active—LOW reset input. This pin performs the same function as SRES, but is of opposite polarity. |
| X1 | 77 | CMOS | I | Crystal oscillator. An external 24MHz crystal is required for oscillator operation. |
| X2 | 78 | | O | |
| DECE | 24 | CMOS input | I | Chip select control. When HIGH, the chip is selected according to the output of the internal address decoder. When LOW, the chip select signal is input on pin $\overline{CS}$. |
| $\overline{CS}$ | 69 | Schmitt | I | Chip select if DECE (pin 84) is LOW. Ignored if DECE is HIGH. See note 3. |
| PA2D | 68 | CMOS input | I | I/O port address select inputs<br>PA2D = LOW: 03FXH<br>PA2D = HIGH: 037XH |
| $\overline{PCXT}$ | 1 | CMOS input | I | Data transfer rate control input. If this pin is LOW, data transfer rate is fixed at 250 kbps. |

Notes:

1. An explanation of pin types follows these tables.
2. All registers in the controller are cleared by a hardware reset, and the disk drive interface signals all set to their non-active states.
3. For chip select to be performed by address lines A0 to A9 from the PC/AT bus, pull both DECE and $\overline{CS}$ up to $V_{CC}$.

## ■ PIN DESCRIPTION (cont.)

### ● Drive Interface

| Pin | | Type | Input/ Output | Description |
|---|---|---|---|---|
| Name | Number | | | |
| DIRL | 41 | Driver | O | Head seek direction control. LOW indicates IN, HIGH indicates OUT. |
| STPL | 39 | Driver | O | Head step pulse. Outputs the required number of pulses to move the heads to the required positions. |
| HSLL | 38 | Driver | O | Head select. LOW selects head 1, HIGH selects head 2 |
| MOT1 | 36 | Driver | O | Drive 1 motor-on signal |
| MOT2 | 35 | Driver | O | Drive 2 motor-on signal |
| DSL1 | 33 | Driver | O | Drive 1 select |
| DSL2 | 32 | Driver | O | Drive 2 select |
| REWL | 30 | Driver | O | Indicates high bit density that is, track numbers 43 and over; active—HIGH if POLT is HIGH, active—LOW if POLT is LOW. |
| WRDT | 29 | Driver | O | Write data signal. See note 1. |
| WRGT | 27 | Driver | O | Write gate |
| TRKO | 23 | Schmitt | I | Active—LOW input indicates that the heads are positioned over track 00. |
| DSKCHG | 22 | Schmitt | I | This active–LOW input is the disk change signal from the drive. |
| INDEX | 21 | Schmitt | I | Active—LOW input indicates detection of the index hole |
| REDT | 20 | TTL | I | Active—LOW read data input. |
| WPRT | 19 | Schmitt | I | Active—LOW input indicates that the inserted diskette is write protected. |
| TPI | 18 | CMOS pull-up | I | Index control input. If this input is HIGH, the index signal from the drive is connected directly to the controller circuitry. If it is LOW, only every second index pulse from the drive is input to the controller. |
| PSA | 5 | CMOS pull-up | I | Write precompensation control input. If this pin is HIGH, precompensation is on. The amount of shift applied to the write data pulse is different for each data transfer rate. If this pin is LOW, write pre-compensation is on only if bit 2 of the diskette control register (PRECOMP) is set. See note 2. |

Notes:

1. The WRDT output is active only while the WRGT signal is active.
2. When using a 3.5-inch drive, set PSA to LOW and PRECOMP to 0. Write precompensation is disabled.

## ■ PIN DESCRIPTION (cont.)

### ● Test and Monitor

| Pin | | Type | Input/ Output | Description |
|---|---|---|---|---|
| Name | Number | | | |
| $\overline{TV}$ | 4 | CMOS pull-up | I | Active-LOW input puts the internal PLL into test mode. |
| $\overline{TF}$ | 3 | CMOS pull-up | I | Active-LOW input puts the internal controller into test mode |
| TΦ | 80 | CMOS | I/O | Internal controller master clock monitor TΦ is an input when either $\overline{TV}$ or $\overline{TF}$ is LOW. |
| TSYN | 17 | CMOS | I/O | Internal controller SYNC signal monitor. TSYN is an input when $\overline{TV}$ is LOW. |
| TDT | 16 | CMOS | I/O | Internal PLL synchronized output data monitor. TDT input is an input when $\overline{TF}$ is LOW. |
| TWIND | 15 | CMOS | I/O | Internal PLL synchronized window signal monitor. TWIND is an input when $\overline{TF}$ is LOW. |
| TPS0 | 14 | CMOS | O | This pin is a KV measurement output if pin $\overline{TV}$ is LOW. |
| TPS1 | 11 | CMOS | I/O | This is the write precompensation control output signal. It is a KV measurement output if pin $\overline{TV}$ is LOW. |
| TVF1 | 25 | CMOS | I/O | Loop gain switching monitor. |
| TVF4 | 8 | CMOS | O | Analog one-shot monitor |
| TVF6 | 2 | CMOS | I/O | Reference clock switching signal output |
| TVF9 | 9 | CMOS pull-up | I | VFO test pin |
| TVF10 | 10 | CMOS | O | VFO monitor test pin |

Note: The test and monitor pins are used for factory test and engineering design testing. They are not used in normal operation.

### ● Power Supply

| Pin | | Description |
|---|---|---|
| Name | Number | |
| $V_{DD1}$ | 6 | PLL analog +5V supply |
| $V_{SS}$ | 7 | PLL analog ground |
| $V_{DD2A}$ | 79 | Oscillator +5V supply |
| $V_{SS2}$ | 76 | Oscillator ground |
| $V_{SS3B}$~$V_{SS3J}$ | 28,31,34,37,40 | 38 mA driver ground |
| $V_{DD5A}$, $V_{DD5B}$ | 12, 74 | Digital +5V supply |
| $V_{SS5A}$, $V_{SS5B}$ | 13, 75 | Digital ground |
| $V_{DD4}$ | 45 | Tri-state driver +5V supply |
| $V_{SS4A}$, $V_{SS4B}$ | 46, 51 | Tri-state driver ground |

Note:

1. Each group of supply pins are connected internally to each other.
2. Pin types:
   - TTL: TTL logic-level
   - CMOS: CMOS logic-level
   - CMOS pull-up: CMOS logic-level input with internal pull-up resistor
   - Schmitt: Schmitt trigger input
   - Tri-state: Tri-state bus driver
   - Driver: Active—LOW 38mA high-current drivers for disk drive interface

## ■ ELECTRICAL CHARACTERISTICS

### ● Absolute Maximum Ratings

| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Power supply voltage | $V_{DD}$ max | −0.5 to +7.0 | V |
| Applied input voltage | $V_I$ max | −0.5 to $V_{DD}$+0.5 | V |
| Applied output voltage | $V_O$ max | | |
| Output driver current | $I_{OLD}$ | 70 | mA |
| Operating temperature | $T_{opg}$ | 0 to 65 | °C |
| Storage temperature | $T_{stg}$ | −65 to 150 | °C |
| Soldering temperature, 10s at pins | $T_{sol}$ | 260 | °C |

### ● DC Characteristics

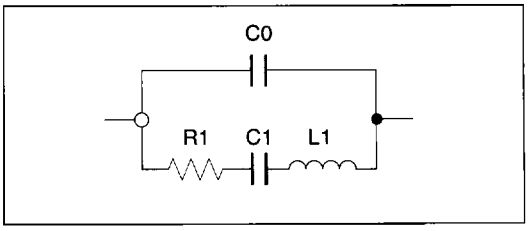
$V_{DD}$=5V±5%, $T_a$=0 to 65°C

| Item | Symbol | Condition | | Rating Min | Rating Typ | Rating Max | Unit |
|---|---|---|---|---|---|---|---|
| Operating supply voltage | $V_{DD}$ | | | 4.75 | 5.0 | 5.25 | V |
| Power supply current | $I_{CC}$ | 24MHz clock, output open, command wait state, VCO=4MHz | 500 kbit/s | — | 30 | 60 | mA |
| | | | 250 kbit/s | — | 25 | 50 | mA |
| Standby current | $I_{STB}$ | Standby mode 2, oscillator off, input terminal fixed, output open | | — | — | 10 | µA |
| **TTL Level Inputs** | | | | | | | |
| HIGH-level input voltage | $V_{IH}$ | | | 2.0 | — | $V_{DD}$+0.3 | V |
| LOW-level input voltage | $V_{IL}$ | | | −0.3 | — | 0.8 | V |
| HIGH-level input leakage current | $I_{LIH}$ | $V_I$=$V_{DD}$ | | — | — | 10 | µA |
| LOW-level input leakage current | $I_{LIL}$ | $V_I$=0V, no pull-up resistor | | — | — | −10 | µA |
| **Driver outputs to disk drive** | | | | | | | |
| LOW-level output voltage | $V_{OLD}$ | $I_{OLD}$=38 mA | | — | — | 0.4 | V |
| HIGH-level output leakage current | $I_{LOH}$ | $V_O$=$V_{DD}$ | | — | — | 10 | µA |
| LOW-level output leakage current | $I_{LOL}$ | $V_O$=0V | | — | — | −10 | µA |
| **Tri-state outputs** | | | | | | | |
| HIGH-level output voltage | $V_{OHT}$ | $I_{OHT}$=−2 mA | | 4.0 | — | — | V |
| LOW-level output voltage | $V_{OLT}$ | $I_{OLT}$=12 mA | | — | — | 0.4 | V |
| HIGH-level tri-state output leakage current | $I_{OZH}$ | $V_O$=$V_{DD}$ | | — | — | 10 | µA |
| LOW-level tri-state output leakage current | $I_{OZL}$ | $V_O$=0V | | — | — | −10 | µA |

## ● AC Characteristics

| Item | Condition | Rating | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Supply ripple (PLL circuit) | | — | — | 50 | mV p-p |
| Supply ripple (excluding PLL) | | — | — | 100 | mV p-p |
| Oscillator frequency | See circuit below | — | 24 | — | MHz |
| **Data Separator** | | | | | |
| One-shot pulse accuracy width | $V_{DD}$=5V±5%, 0 to 65°C | –10 | — | 10 | % |
| VCO center frequency accuracy | $V_{DD}$=5V±5%, 0 to 65°C | –10 | — | 10 | % |
| | control voltage=$V_{DD}$ or 2 | | | | |
| VCO sensitivity (Kv) | $V_{DD}$=5V, $T_a$=25°C | 1.6 | — | 2.3 | MHz/V |
| | control voltage=2 to 3V | | | | |
| Sync Detector pulse range period | Transfer rate = 500 kbps | 1.6 | 2.0 | 2.4 | µs |
| | Transfer rate = 300 kbps | 2.67 | 3.33 | 4.0 | |
| | Transfer rate = 250 kbps | 3.2 | 4.0 | 4.8 | |

### Crystal Equivalent Circuit

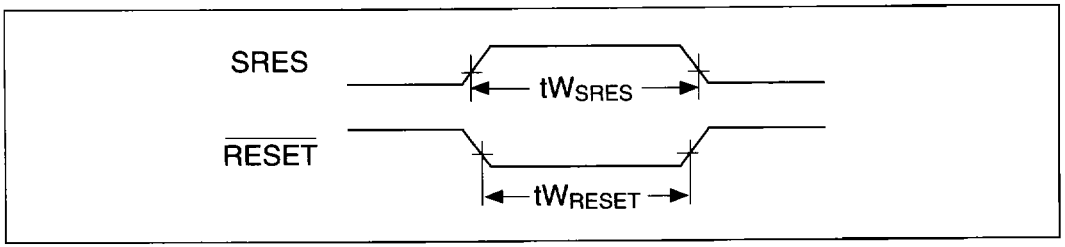



Standard values: Q = 190000
C0 = 2.3 pF
C1 = 9.8 pF
R1 = 5Ω
L0 = 4.5 mH

## ● Timing Characteristics

$V_{DD}$ = 4.5 V, $V_{IH}$ = $V_{DD}$, $V_{IL}$ = 0V, $T_a$ = 25°C, rise/fall time = 10 ns max., TΦ = 125 ns at a transfer rate of 500 kbps; 208 ns at 300 kbps; 250 ns at 250 kbps

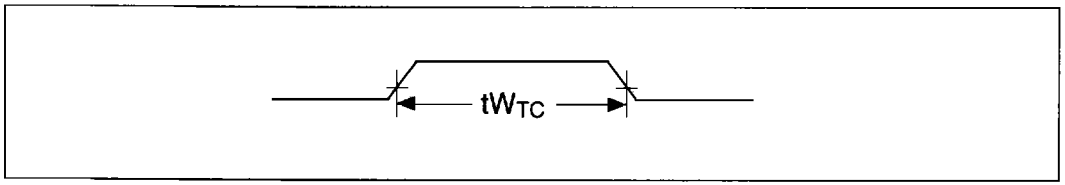
○Hardware Reset Waveforms




Note: Do not read from or write to registers within 2 µs of releasing the reset signal.

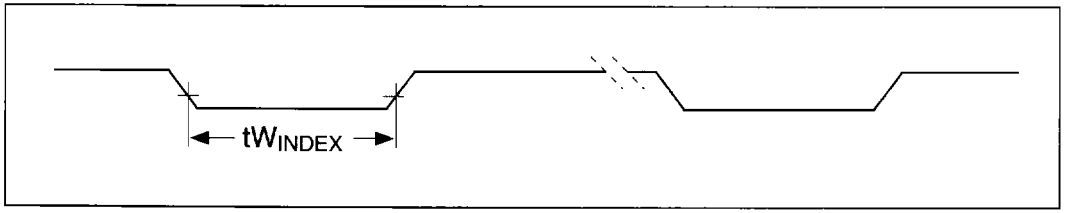
| Item | Symbol | Condition | Rating | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| SRES valid pulsewidth | tWSRES | | 400 | — | ns |
| $\overline{\text{RESET}}$ valid pulsewidth | tWRESET | | 400 | — | ns |

oTC Waveforms



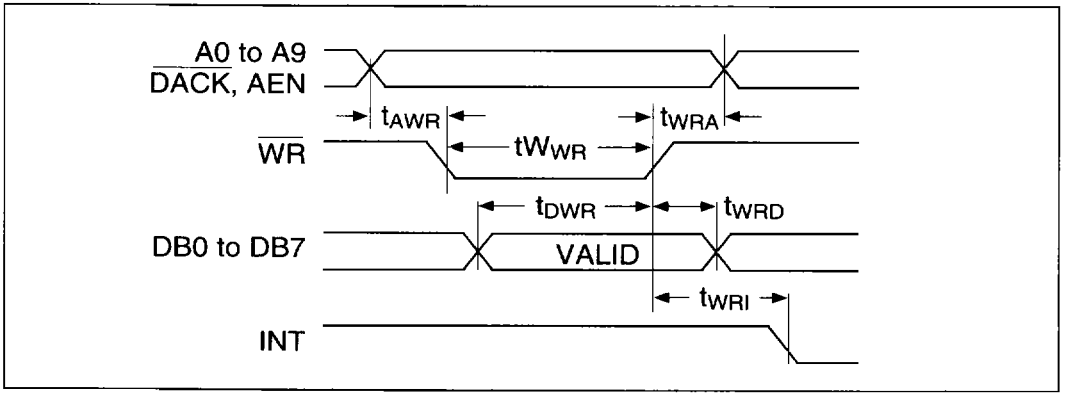

| Item | Symbol | Condition | Rating | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| TC pulsewidth | tWTC | | 125 | — | ns |

oIndex Waveforms



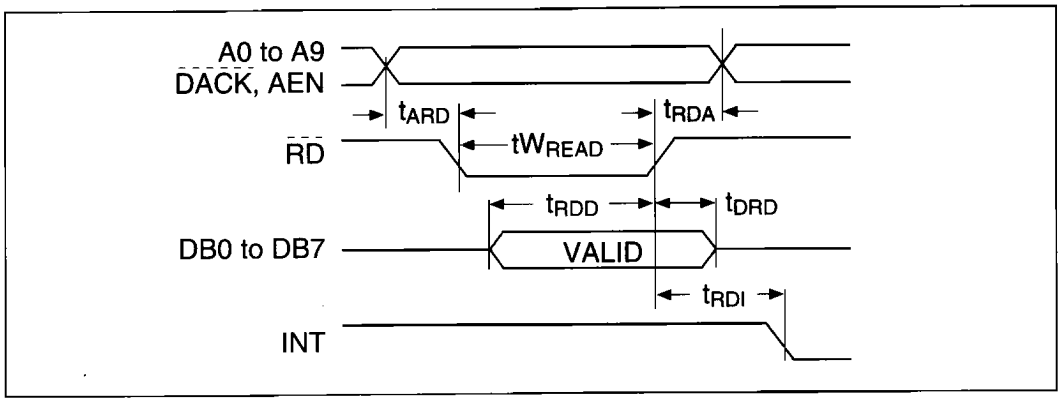

| Item | Symbol | Condition | Rating | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| INDEX pulsewidth | tWINDEX | | 4 | — | TΦ |

oCommand and Data Write Timing



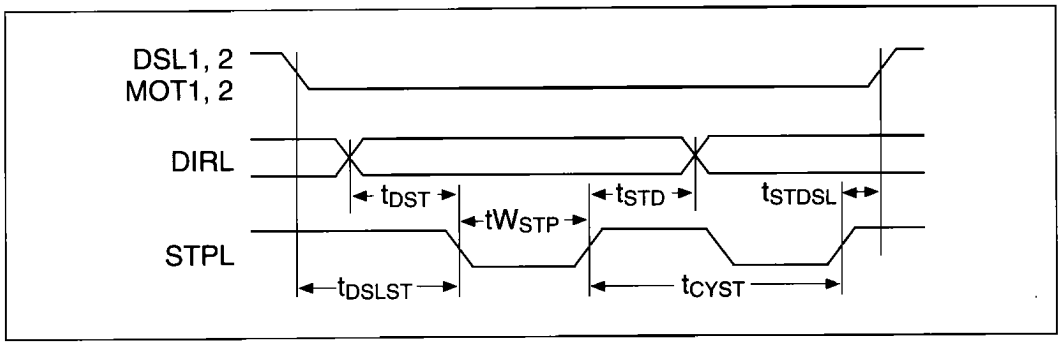

| Item | Symbol | Condition | Rating | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| Address or DACK setup time | tAWR | | 0 | — | ns |
| Address or DACK hold time | tWRA | | 0 | — | ns |
| WR pulsewidth | tWWR | | 200 | — | ns |
| Data setup time (with respect to WR) | tWDWR | | 100 | — | ns |
| Data hold time (with respect to WR) | tWWRD | | 5 | — | ns |
| WR ↑ to INT ↓ delay time | tWWRI | Non-DMA mode | — | 100 | ns |

oStatus and Data Read Timing



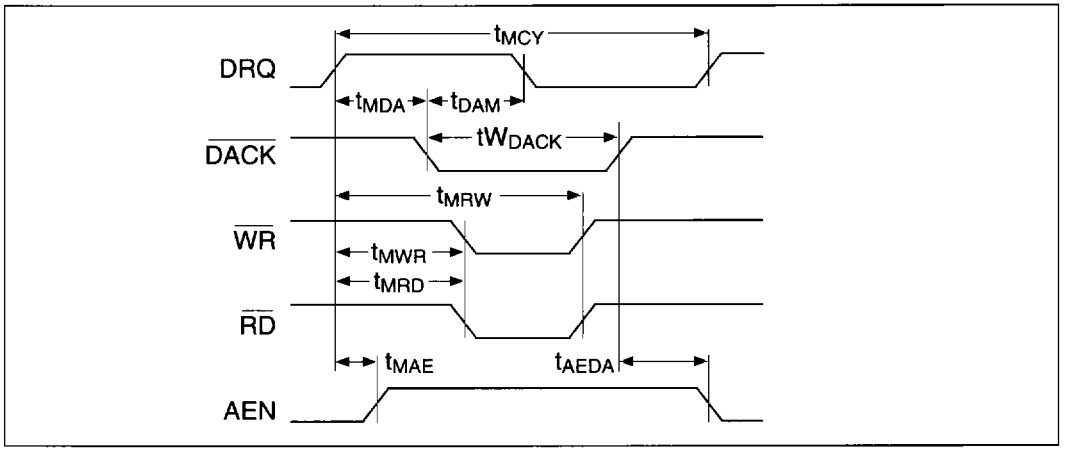

| Item | Symbol | Condition | Rating | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| Address or DACK setup time | tARD | | 0 | — | ns |
| Address or DACK hold time | tRDA | | 0 | — | ns |
| RD pulsewidth | tWREAD | | 200 | — | ns |
| Data setup time (with respect to RD) | tWRDD | | — | 120 | ns |
| Data hold time (with respect to RD) | tWDRD | | 0 | — | ns |
| RD ↑ to INT ↓ delay time | tWRDI | Non–DMA mode | — | 100 | ns |

oSeek Timing



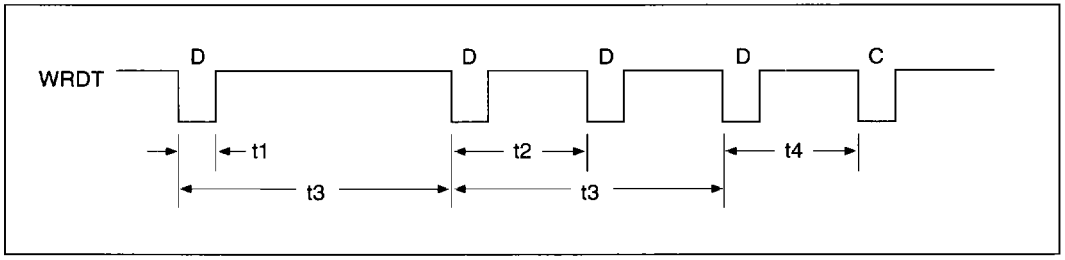

| Item | Symbol | Condition | Rating | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| DIRL setup time (with respect to STPL) | tDST | | 8 | — | TΦ |
| DIRL hold time (with respect to STPL) | tSTD | | 192 | — | TΦ |
| STPL pulsewidth | tWSTP | | 48 | 64 | TΦ |
| DSL1 and DSL2 setup time (with respect to STPL) | tDSLST | | 336 | — | TΦ |
| DSL1 and DSL2 hold time (with respect to STPL) | tSTDSL | | 80 | — | TΦ |
| STPL cycle time | tCYST | | 264 | — | TΦ |

oDMA Timing




| Item | Symbol | Condition | Rating | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| DRQ cycle time | tMCY | | 104 | — | TΦ |
| DRQ ↑ to DACK ↓ response time | tMDA | Transfer rate = 500 kbps | 200 | — | ns |
| | | Transfer rate = 250 kbps | 400 | — | |
| DACK ↓ to DRQ ↓ delay time | tDAM | | — | 140 | ns |
| DACK pulsewidth | tWDACK | Transfer rate = 250 kbps | 550 | — | ns |
| DRQ ↑ to RD ↓ response time | tMRD | | 1 | — | TΦ |
| DRQ ↑ to RW ↓ response time | tMWR | | 2 | — | TΦ |
| DRQ ↑ to WR/RD response time | tMRW | | — | 96 | TΦ |
| DRQ setup time (with respect to AEN) | tMAE | | 0 | — | ns |
| DACK hold time (with respect to AEN) | tAEDA | | 0 | — | ns |

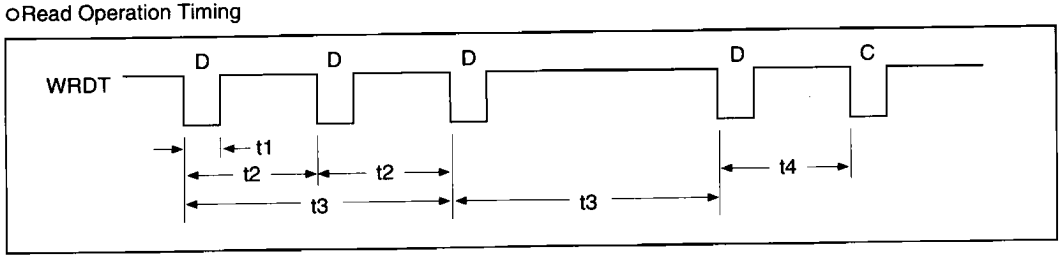
oWrite Timing




| Recording Density | Time | | | |
|---|---|---|---|---|
| | t1 | t2 | t3 | t4 |
| High density (500 Kbit/s) | 250 ns ±100 ns | 2 µs | 3 µs | 4 µs |
| Normal density (250 Kbit/s) | 500 ns ±100 ns | 4 µs | 8 µs | 6 µs |
| Normal density (300 Kbit/s) | 417 ns ±100 ns | 3.33 µs | 6.67 µs | 5 µs |

Notes: 1. No write precompensation 2. t2 to t4 are standard values 3. MFM recording format used

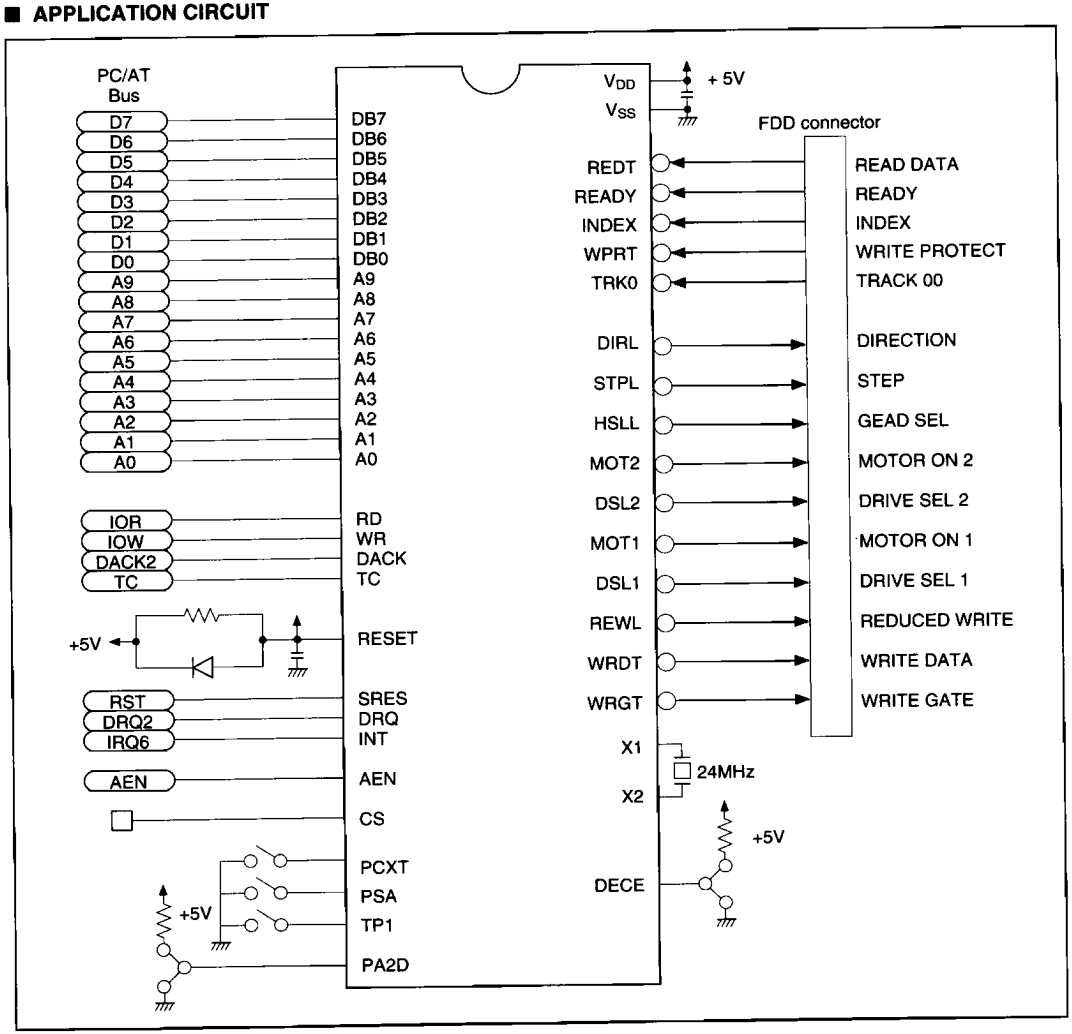
○Read Operation Timing




| Recording Density | Time | | | |
|---|---|---|---|---|
| | t1 | t2 | t3 | t4 |
| High density (500 Kbit/s) | 200 ns ±50 ns | 2 µs | 4 µs | 3 µs |
| Normal density (250 Kbit/s) | 200 ns ±50 ns | 4 µs | 8 µs | 6 µs |
| Normal density (300 Kbit/s) | 200 ns ±50 ns | 3.33 µs | 6.67 µs | 5 µs |

Notes: 1. t2 to t4 are standard values 2. MFM recording format used

## ■ APPLICATION CIRCUIT



## ■ PACKAGE DIMENSIONS