Contents

S70L41B is a fully integrated CMOS POCSAG (CCIR Radio Paging code No.1) decoder and page controller for display pagers.The decoded POCSAG data are transferred over a serial interface to a microcontroller according to its commands for processing and subsequent storage and display.
Its on chip buffer register allows the microcontroller to stay in subclock (lower frequency) mode in receiving interrupt requests from S70L41B.
S70L41B also has an improved synchronization algorithm for efficient power saving.
In addition to its conventional decoding and error correcting function, it has a data conversion function for Chinese characters.
With 76.8kHz X'tal oscillator, the decoder can be applied to any one of 512,1200 and 2400 bps system by using its internal registers.

■ Features

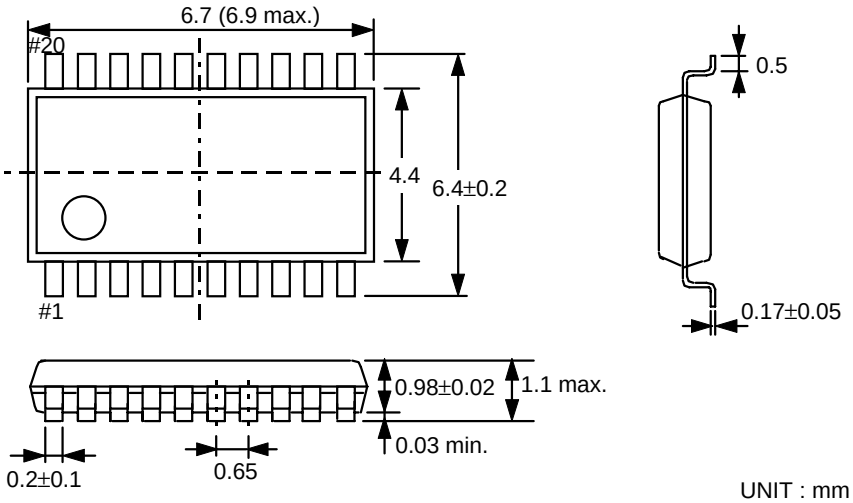
- Low voltage operation 0.9Vmin
- Low current consumption 50μA max. @1.5V
- 8bit serial interface for a CPU with on-chip level shifters
- Data conversion function (data lenghth of 4, 7 or 8 bits)
- 512/1200/2400bps register selectable
- 6 addresses and two frames (programmable address assignment)
- Programmable receiver warm-up's
- Multistage warm-up's(BS1,2,3)
- Stop (power-down) mode provided for clock function only
- Up to 2 bit random error correction
- On-chip command decoder for CPU control
- On-chip oscillator circuitry for 76.8kHz X'tal
- 20 pin TSSOP

■ Specifications

Table 1
(Ta=25 °C, 76.8 kHz X'tal used unless otherwise noted)

Characteristic	Value	Condition
Operating Voltage Range	V_{DD1}=0.9~2.2 V V_{DD2}=V_{DD1}~3.6 V	
Average Current Consumption with no page	6 μAtyp. 15 μAtyp.	V_{DD1}=1.5 V V_{DD1}=2.0 V
Average Current Consumption at Stop Mode	5 μAtyp.	V_{DD1}=1.5 V
Operating Temp. Range	-10°C~+50 °C	

■ Dimensions



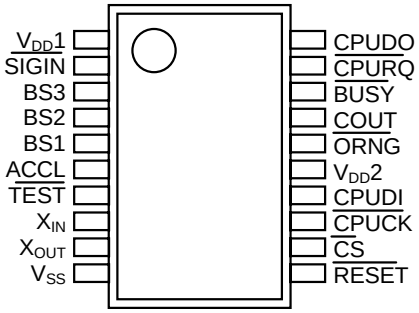
UNIT : mm

■ Absolute Maximum Ratings

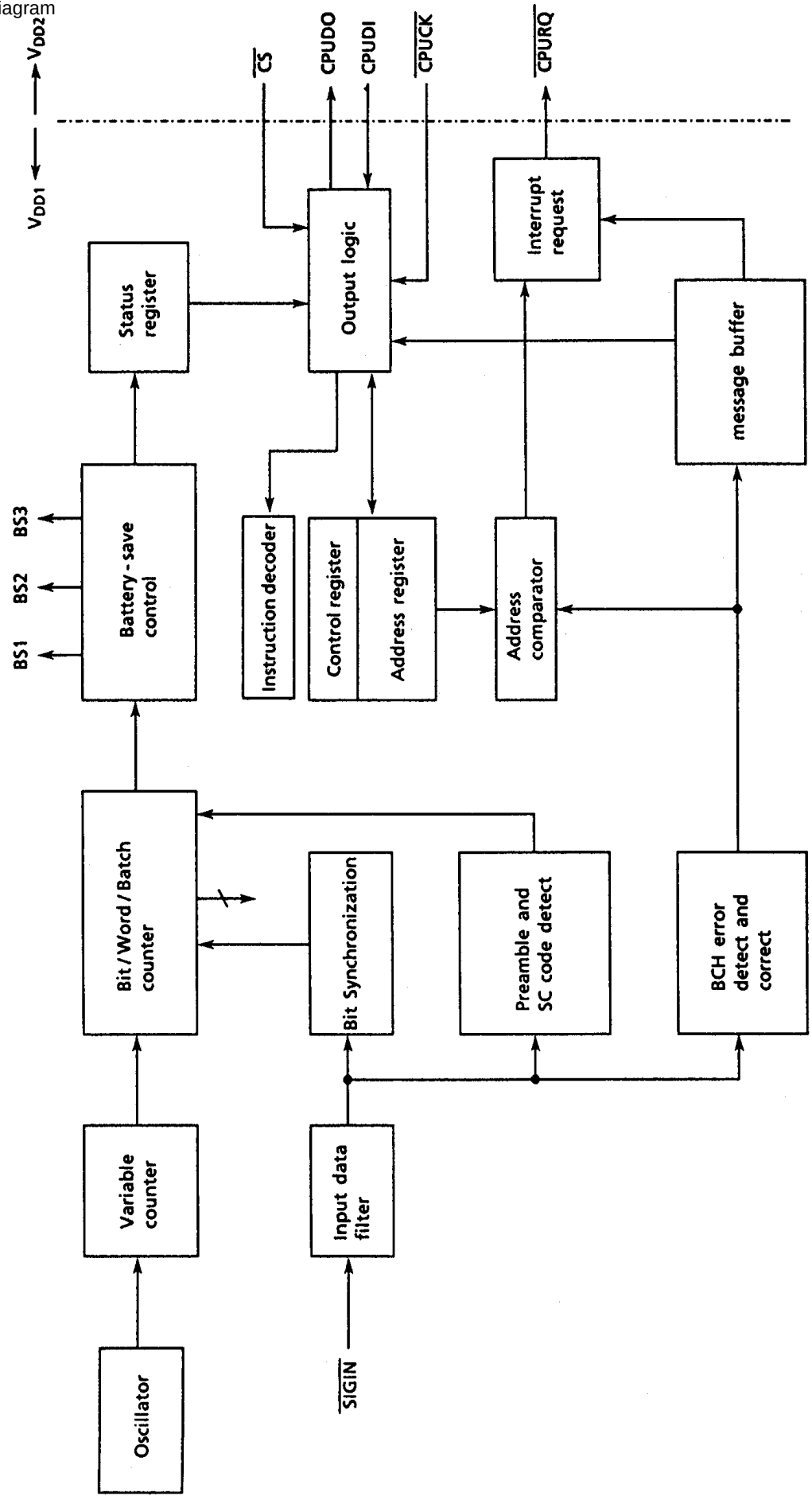
Table 2

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.3 to +4.5	V
Input Voltages	V_{IN}	V_{SS}–0.3 to V_{DD}+0.3	V
Output Voltages	V_{OUT}	V_{SS} to V_{DD}	V
Storage Temperature Range	T_{bias}	–40 to +125	°C
Operating Temperature Range	T_{opr}	–10 to +50	°C

■ Pin Configuration



■ Block Diagram



■ Pin Assignment

Table 3

Pin No	Pin Name	Functions	**L.S.**
1	V_{DD1}	Positive power supply	
2	$\overline{SIGIN}$	Received data input (Inverse or Noninverse register selectable)	No
3	BS3	Batterysaving signal output (for PLL)	No
4	BS2	Same as above (for quick charge)	No
5	BS1	Same as above (for RF and IF)	No
6	ACCL	Test clock input for acceleration	No
7	$\overline{TEST}$	Test input (with pull-up). Sets BS1,2,3 "H" when "L" is input during resetting. Enables test registers to be written by a uP.	No
8	X_{IN}	Oscillator circuit gate input	No
9	X_{OUT}	Oscillator circuit drain output	No
10	V_{SS}	Connects to gnd.	
11	$\overline{RESET}$	Hardware reset input (with pull-up)	No
12	$\overline{CS}$	Chip select input for interfacing with a uP. "L" input to this pin enables CPUDO terminal to indicate the status of the decoder.	Yes
13	$\overline{CPUCK}$	Serial clock input from a uP.	Yes
14	CPUDI	Serial data input from a uP.	Yes
15	V_{DD2}	Positive power supply for the level shifters	
16	$\overline{ORNG}$	Receiver out of range indication output. Goes "L" when a certain amount of time has passed after the SC code loss. The time after missing SC code selectable by internal registers "OR0" and "OR1".	Yes
17	COUT	Oscillator clock output Outputs osc. frequency (76.8kHz) or pseudo 32.768kHz with a duty ratio of 1/3 to 2/3. The frequency selected by the register "CSEL". Pulled down to "L" when clock output is disabledby the "CDIS" register.	Yes
18	$\overline{BUSY}$	Decoder busy indication output. While "L", no commands accepted, no data ready to be output.	Yes
19	$\overline{CPURQ}$	Interrupt request signal output to a uP. Goes "L" on a page reception .	Yes
20	CPUDO	Serial data output to a uP.	Yes

L.S. : Level Shifter

■ Pin Structural Configuration

Table 4

Pin #	Pin Name	I/O	Structure	PU/PD	Reset	Remarks	Circuit
1	V_{DD1}	—					
2	$\overline{SIGIN}$		CMOS				I1
3	BS3	O	CMOS		L	"H" @$\overline{TEST}$="L"	O1
4	BS2	O	CMOS		L	Same as above	O1
5	BS1	O	CMOS		L	Same as above	O1
6	ACCL	I	CMOS				I1
7	$\overline{TEST}$	I	CMOS	PU		Schmitt trigger	I3
8	XIN	I					
9	XOUT	O					
10	V_{SS}	—					
11	$\overline{RESET}$		CMOS	PU		Schmitt trigger	I3
12	$\overline{CS}$	I	CMOS with L.S.				I1
13	$\overline{CPUCK}$	I	CMOS with L.S.				I2
14	CPUDI	I	CMOS with L.S.				I1
15	V_{DD2}	—					
16	$\overline{ORNG}$	O	CMOS with L.S.		L		O2
17	COUT	O	CMOS with L.S.		L		O2
18	$\overline{BUSY}$	O	CMOS with L.S.		H		O2
19	$\overline{CPURQ}$	O	CMOS with L.S.		H		O2
20	CPUDO	O	CMOS with L.S.		OFF		O3

(Notes) PU : Pull-Up Resistor, PD : Pull-Down Resistor, L.S.: Level Shifter

■ Input/Ouput Circuits

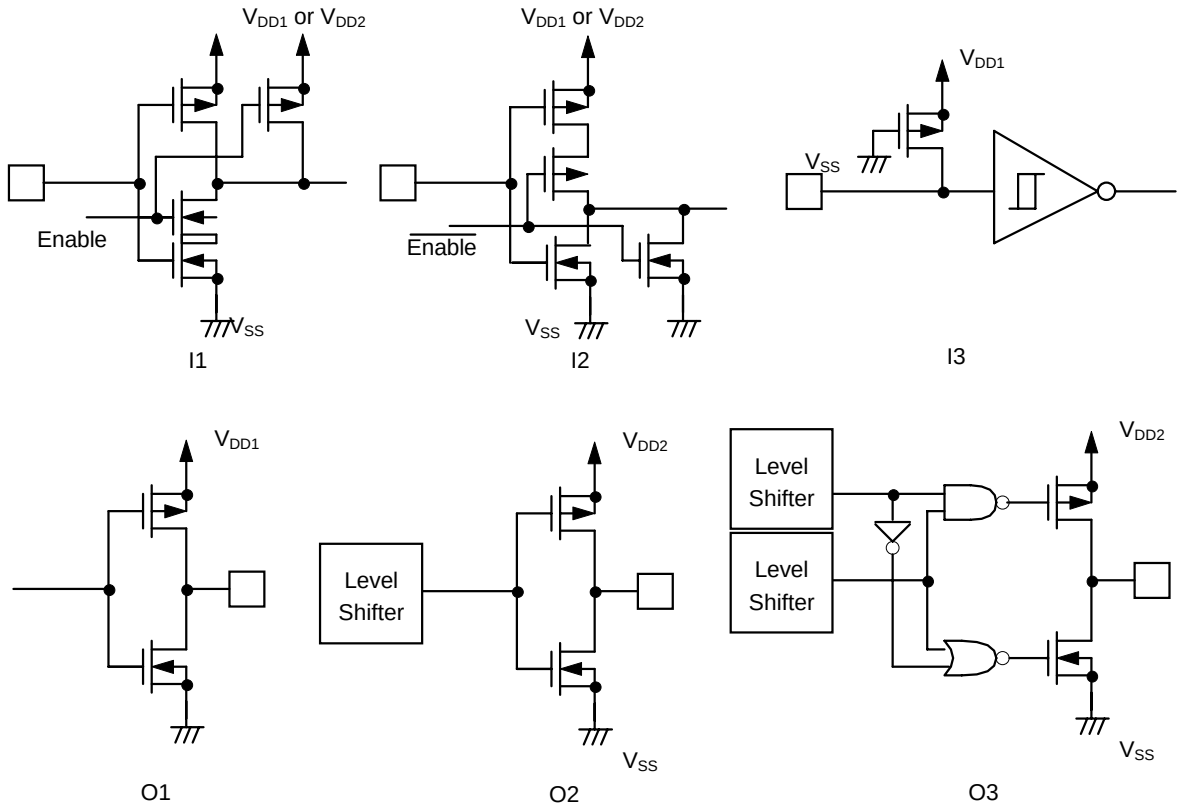


Figure 1

■ Electrical Characteristics

1. DC Electrical Characteristics

Table 5

(V_{DD}=1.5V, V_{SS}=0V, Ta=25 °C Unless otherwise noted)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit	Circuit	Note
Operating Voltage Range	V_{DD}	Ta=–10 to 50°C 76.8kHz	V_{DD1}	0.9	1.5	2.2	V	①	1
			V_{DD2}	V_{DD1}	3.0	3.6			
Oscillator Start-up Voltage	V_{DOB}	Ta=–10 to 50°C 76.8kHz		(1.0)	1.5	2.2	V	①	2
Average Current Consumption with no page	I_N	f0=76800Hz	V_{DD}=1.5V		6.0	25	µA	①	3
			V_{DD}=2.0V		15.0	50			
Output Current	I_{OH1}	V_{DD}=1.5V, V_{OH}=1.2V *1		-700	-350	-180	µA	②	4
	I_{OL1}	V_{DD}=1.5V, V_{OL}=0.3V *1		130	250	500			
	I_{OH2}	V_{DD2}=3.0V, V_{OH}=2.4V *2		-2000	-1000	-500			
	I_{OL2}	V_{DD2}=3.0V, V_{OL}=0.6V *2		430	860	1700			
Input Voltage	V_{IH}	V_{DD1}=1.5V, V_{DD2}=3.0V		0.8×V_{DD}			V	③	
	V_{IL}					0.2×V_{DD}			
Input Current	I_{IN}	V_{IN}=V_{DD} or V_{SS}		–0.1		0.1	µA	④	
Pull-up Current	I_{R1}	V_{IN}=0V *3		–7.2	—	–1.8	µA	⑤	
	I_{R2}	V_{IN}=1.3V *3		–72	—	–18			
Power-on Reset Capacitor	C_{PON}	Tied between $\overline{\text{RESET}}$ and the ground		100	1000	10000	pF		
Reset Pulse Width	t_{RST}	When externally applied		10			µS		

*1 Applied to BS3, BS2, BS1, $\overline{\text{CPURQ}}$
*2 Applied to $\overline{\text{ORNG}}$, $\overline{\text{COUT}}$, BUSY, $\overline{\text{CPURQ}}$, CPUDO
*3 Applied to $\overline{\text{TEST}}$, $\overline{\text{RESET}}$

2. AC Electrical Characteristics

Table 6

(V_{DD}=1.5V, V_{SS}=0V, Ta=25°C Unless otherwise noted)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit	Circuit	Note
Frequency deviation over IC's	Δf / ΔIC				±50	ppm		5
Frequency deviation over Operation Voltage range	Δf / ΔV				±8	ppm		6
Recommended equivalent resistance	CI				45	KΩ		

Notes 1. Insertion of a capacitor of 0.1µF or larger between V_{DD1} and V_{SS} is recommended.
2. The voltage that either 32KHz or 76.8KHz is output from COUT pin within 10 sec. after power-on.
3. Excluding a pull-up current.
4. The current flowing into the IC is considered positive.
5.

$$\Delta f/\Delta IC = \frac{f(V_{DD}=1.5V) - f0}{f0} \times 10^6 \text{ (ppm)} \quad \times \quad f0\text{:Average frequency } @V_{DD}=1.5V$$

6.

$$\Delta f / \Delta V = \frac{f(V_{DD}=1.5V) - f2\ (V_{DD}=1.4V)}{f1\ (V_{DD}=1.5V)} \times 10^6 \text{ (ppm)}$$

■ Circuits For Measurement

①

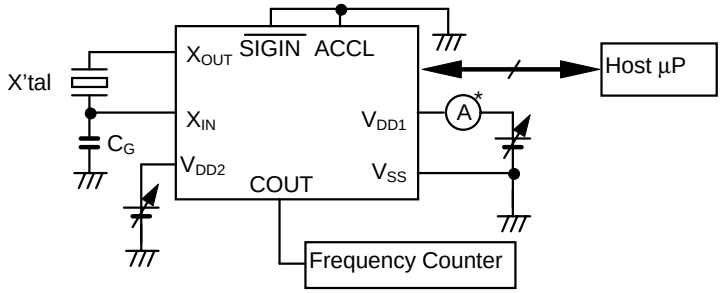
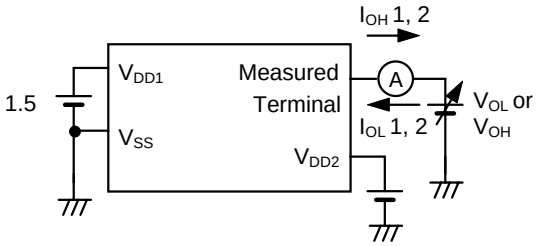


Table 7

Characteristics	Measurement Operation
Current Consumption	Connect $\overline{\text{SIGIN}}$ and ACCL to V_{SS}. Insert ammeter at *.
Oscillator Start-up Voltage	Connect a frequency counter to COUT.
Operating Voltage Range	Interface with a host CPU to confirm the received data. Input NRZ POCSAG data from $\overline{\text{SIGIN}}$.

②



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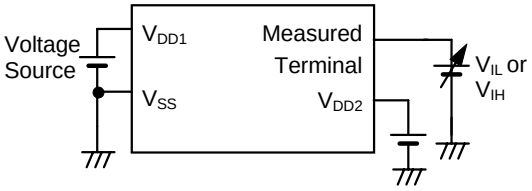

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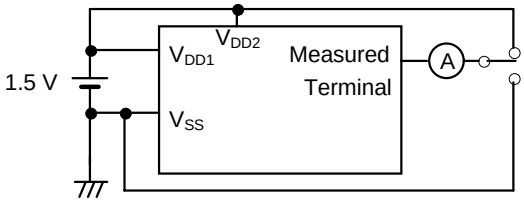

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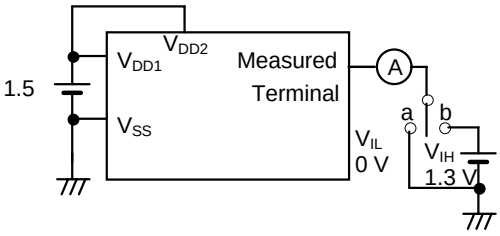


Figure 2

■ Registers

Register Name	Address	B7	B6	B5	B4	B3	B2	B1	B0
Receive Address Receive enable	0 0 0 0 0	a7	a6	a5	a4	a3	a2	a1	a0
	0 0 0 0 1	a15	a14	a13	a12	a11	a10	a9	a8
	0 0 0 1 0						$\overline{aE}$	a17	a16
	0 0 1 0 0	b7	b6	b5	b4	b3	b2	b1	b0
	0 0 1 0 1	b15	b14	b13	b12	b11	b10	b9	b8
	0 0 1 1 0						$\overline{bE}$	b17	b16
	0 1 0 0 0	c7	c6	c5	c4	c3	c2	c1	c0
	0 1 0 0 1	c15	c14	c13	c12	c11	c10	c9	c8
	0 1 0 1 0						$\overline{cE}$	c17	c16
	0 1 1 0 0	d7	d6	d5	d4	d3	d2	d1	d0
	0 1 1 0 1	d15	d14	d13	d12	d11	d10	d9	d8
	0 1 1 1 0						$\overline{dE}$	d17	d16
	1 0 0 0 0	e7	e6	e5	e4	e3	e2	e1	e0
	1 0 0 0 1	e15	e14	e13	e12	e11	e10	e9	e8
	1 0 0 1 0						eE	e17	e16
	1 0 1 0 0	f7	f6	f5	f4	f3	f2	f1	f0
	1 0 1 0 1	f15	f14	f13	f12	f11	$\overline{f10}$	f9	f8
	1 0 1 1 0						fE	f17	f16
Frame select	1 1 0 0 0	FS1	FS0	F22	F21	F20	F12	F11	F10
BS Timing	1 1 0 0 1		BS32	BS31	BS30	BS21	BS20	BS11	BS10
Others	1 1 0 1 0	CDIS	CSEL			DR1	DR0	SGIN	
	1 1 0 1 1			OR1	OR0	ADRS		EE1	EE0
TEST	1 1 1 1 1					T3	T2	T1	T0
Status	0	SC	0	SA1	SA0	OVFL	LAST	E1	E0
	1	SC	0	MD1	MD0	OVFL	Adr2	Adr1	Adr0
DREG	- - - - -	D7	D6	D5	D4	D3	D2	D1	D0

■ Register Functions

1. Control Registers

Name	Function
a0 to a17	Store receiving address No.1
b0 to b17	Store receiving address No.2
c0 to c17	Store receiving address No.3
d0 to d17	Store receiving address No.4
e0 to e17	Store receiving address No.5
f0 to f17	Store receiving address No.6
$\overline{aE}$ to $\overline{fE}$	Receive mode enable for each address
FS1,0	Select frame assignment for receiving addresses FS1, FS0 0,0 0,1 1,0 1,1 frame A none adr.1 adr.1,2 adr.1-3 frame B adr.1-6 adr.2-6 adr.3-6 adr.4-6
F10 to F12	Select frame A
F20 to F22	Select frame B
BS10 to BS11	Select BS1 output timing (1 of 4)
BS20 to BS21	Select BS2 output timing (1 of 4)
BS30 to BS32	Select BS3 output timing (1 of 8)
SGIN	SIGIN input polarity: Inverse when cleared, normal when set.
DR1, 0	Select receiving data rate("00": 512bps, "01": 1200bps, "1*": 2400bps) * : don't care
OR1, 0	Timer select for out of range indication ("00":0sec.,"01":2min.,"10":4min.,"11":8min. approximately)
ADRS	Address search mode select. When set ("1"), decoder keeps searching for its addresses once after SC. loss.
CDIS	Disables clock output from COUT pin when set to "1". COUT pin outputs "L" when disabled.
CSEL	Selects the output clock rate of the COUT pin. "0":pseudo 32kHz ,"1":76.8kHz
EE1,0	Select the max. number of acceptable errors as listed below. When the data length is 4 or 7 bits, the remaining bits on MSB side (Status Reference Flag) are set to indicate the excess of errors or the end of the data. See status 0 to know which of the above cases has occurred. When programmed as "00", the Status Reference Flag is diabled. ("00":BCH or Parity 2bits, "01":0bit, "10": 1bit, "11":2bits)
T0 to 3	Test mode select

2. Status And Data Registers

Name	Function
E1,0	Indicate No. of errors in each received word. "11" for more than or equal to three erroneous bits.
SC	Set when a SC code is detected. Kept at "1" until failing to receive one.
OVFL	Memory overflow indication: Shows the buffer memory has been overflowed.
Adr0~Adr2	Received address indication
SA1,0	Subaddress(function bits) indication
MD1,0	Indicate the operation mode that the decoder is in. ("00":STOP, "01":NULL, "10":PAUSE, "11":RUN)
LAST	Indicates that there are no more messages left in the buffer register.
D7 to D0	Data register that stores received data.

(Notes) All the registers are cleared on initialization.

■ Instruction Codes

Instruction	Instruction code						Operand
NOP	000	×	×	×	×	×	don't care
Write Register	001	a4	a3	a2	a1	a0	b7~b0
Read Status 0	1000		×	×	×	×	don't care
Read DREG	101	L2	L1	L0	×	×	don't care
Read Register	110	a4	a3	a2	a1	a0	don't care
STOP	111	0	0	×	×	×	don't care
PAUSE	111	1	0	×	×	×	
RUN	111	1	1	×	×	×	

(Notes) a4 to a0 : register address
L2 to L0 : data length; Only three are allowed. 100 for 4 bits, 111 for 7 bits and 000 for 8 bits.

■ Operation of Each Instruction

Instruction	Operation	Bytes
NOP	No operation. Used when serial clock input is needed.	1
Write Register	The operand is stored into the register assigned by the command.	2
Read Status 0	The data in the status register 0 are transferred to the output shift register.	1
Read DREG	The received data divided into the data length assigned by L2-L0 are transferred to the output shift register.	1
Read Register	The data in the wanted register are transferred to the output shift register.	1
STOP	Resets the counters related to the decoding function and the BS signals. Registers including the ones that store addresses remain uncleared. Oscillator circuit is held active.	1
PAUSE	OSC., clock function and sync. detection circuit are enabled. Address detection is disabled.	1
RUN	Sets the whole function in motion. Starts with asynchronous mode, then sync. mode to receive the messages.	1

■ Battery Saving

S-70L41 has three battery saving terminals (BS1-3) . Fig.3 shows the output timing of BS1-3.
The BS signal output timing is selected by the BS register as described in Table 8.

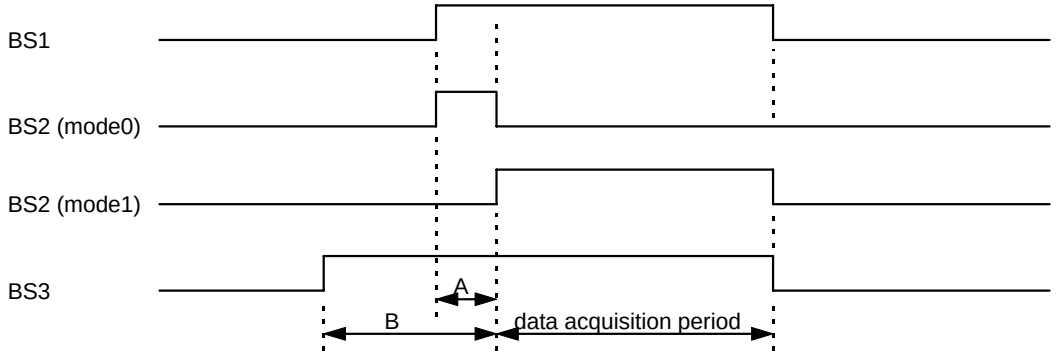


Figure 3

Table 8

BS32	BS31	BS30	BS21	BS20	BS11	BS10	Operation timing (512/1200, 2400bps)
0	0	0					B=11.7 / 11.7ms
0	0	1					B=17.6 / 17.5ms
0	1	0					B=23.4 / 23.3ms
0	1	1					B=29.3 / 29.2ms
1	0	0					B=35.2 / 35.0ms
1	0	1					B=41.0 / 40.8ms
1	1	0					B=46.9 / 46.7ms
1	1	1					B=52.7 / 52.5ms
			0				BS2 output in async. state only. No BS2 output in sync. state.
			1				BS2 output in both async. and sync. state.
				0			Mode 0 output for BS2.
				1			Mode 1 output for BS2.
					0	0	A=3.9 / 4.2ms
					0	1	A=7.8 / 8.3ms
					1	0	A=11.7 / 12.5ms
					1	1	A=15.6 / 16.7ms

(Note) The operation timing listed above is correct only when A<B.

■ Programming and Controlling Each Register

1. Programming the Control Register

When the S-70L41 is initialized, the contents of the control register are completely cleared and it enters Awaiting Command status, where only the oscillating circuit is running (STOP mode). In order to receive data, the control code including addresses from the host CPU has to be written to the control register. This is done by the Write Register command from the host CPU (see Figure 4). The RUN command after completion of writing to the control register allows the S-70L41 to initiate intermittent reception of data.

During initialization, the COUT terminal of the S-70L41 is pulled down. A pseudo 32.768 kHz clock pulses are output soon after initialization. The host CPU can use this clock for its system clock. In this case, AC coupling is recommended to connect the COUT terminal of the S-70L41 and the XIN terminal of the host CPU.

2. Handling the Status and Data Registers and Received Data

There are two types of Status Registers (STATUS 0,1). Information concerning message reception is saved in STATUS 0, and information concerning address reception is saved in STATUS 1. The contents of Status Register 1 are output from the CPUDO terminal whenever the host CPU accesses serial I/O (hereinafter called SIO) by turning the $\overline{CS}$ terminal to "L", responding to the interrupt during address reception. Usually, the host CPU outputs the Read Status 0 command first, retrieving simultaneously the contents of Status Register 1 (see Figure 5).
The contents of Status Register 1 informs the user of whether or not the status is synchronized with the signal transmitted from the station, which operation mode the S-70L41 is in, and whether or not the buffer register has overflowed, etc. This allows the user to confirm the validity of the received address. Information, such as BCH error detection, end of message signals, and subaddresses can be obtained from Status Register 0, which enables users to judge the validity of received messages and completion of message reception.
The Data Register is what you access to get the received data. The received message is usually divided by 8 bits, and readout from the LSB. The Read DREG command includes assignment of the data length, which can divide the message into either 4 bits or 7 bits (see Figure 6). In this case, data are stored on the LSB side, and the Status Reference Flag is assigned to the remaining bit (s) on MSB side. The Status Reference Flag is set when the number of bits assigned by EE bits are detected as BCH error, or when the end of message is detected. When the Status Reference Flag is found to be set, read Status Register 0 for the number of errors (E1, E0) and the LAST bit. When accessing the Data Register, display, dispose of or flicker the data, as required in accordance with the number of error (s) , while confirming the contents of the Status Register.

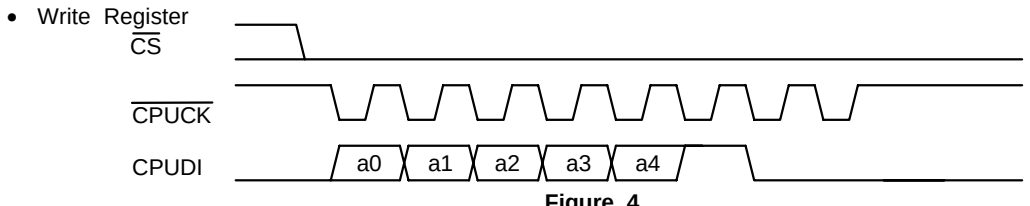


Figure 4

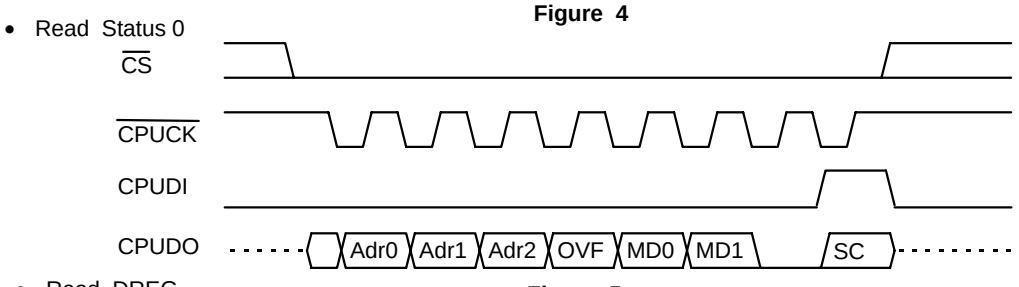


Figure 5

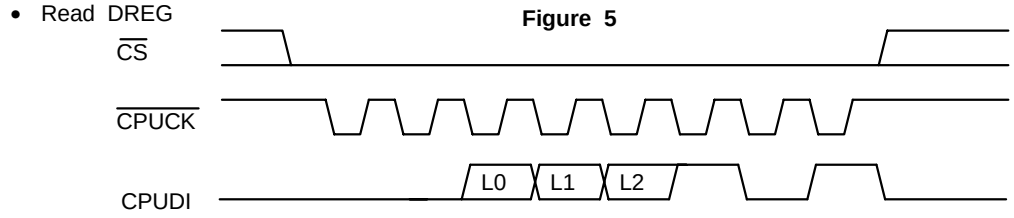


Figure 6

■ Operation Description

1. Initialization

The register and the divider are initialized when the power of the S-70L41 is turned on by insertion of a capacitor of table 5 between $\overline{\text{RESET}}$ terminal and the GND. Driving the $\overline{\text{RESET}}$ terminal to "L" can also initialize the S-70L41. During initialization, the oscillating circuit is held active.
The output status of the terminals during initialization (reset) is shown in Table 4. When initialization is completed (after the $\overline{\text{RESET}}$ terminal is turned back to "H"), pseudo 32.768 kHz clock pulses are output from COUT. It is possible to disable this clock by pulling-down to the ground using the CDIS bit, as well as to change the clock rate from to 76.8 kHz using the CSEL bit. After initialization the S-70L41 enters STOP mode.

2. Decoding the POCSAG Signal

2.1 S-70L41 Operation Mode

The S-70L41 has three operation modes (see Figure 7). The operation mode is shifted to the asynchronous status (ASYNC State) in RUN mode when the RUN command is input from the host CPU while in Stop mode. The S-70L41 begins to perform intermittent reception in this status .
The data received from the SIGIN terminal while BS1 is "H" are sampled, and data retrieval timing is adjusted by the synchronization adjustment circuit with edge detection. When an alternate pattern of 1, 0, 1, 0, ··· is detected in succession, it is recognized as PREAMBLE. A comparison between the received data and the synchronous code is also performed. When the synchronous code is detected, the S-70L41 shifts to the synchronous state (SYNC State) in the RUN mode. Then if no more synchronous code is detected, the S-70L41 returns to the asynchronous state again. Data retrieval is not performed while BS1 is "L."
The PAUSE Command lets the S-70L41 enter PAUSE mode. In PAUSE mode, only the establishment and maintenance of synchronization but address search (programmed frame retrieval) is performed. PAUSE mode, as well as RUN mode, has both asynchronous state (ASYNC State) and synchronous state (SYNC State). The difference is that no frame search is performed in PAUSE Mode.When given the PAUSE Command during message reception, the operation mode is shifted to the PAUSE Mode after completion of the present batch.

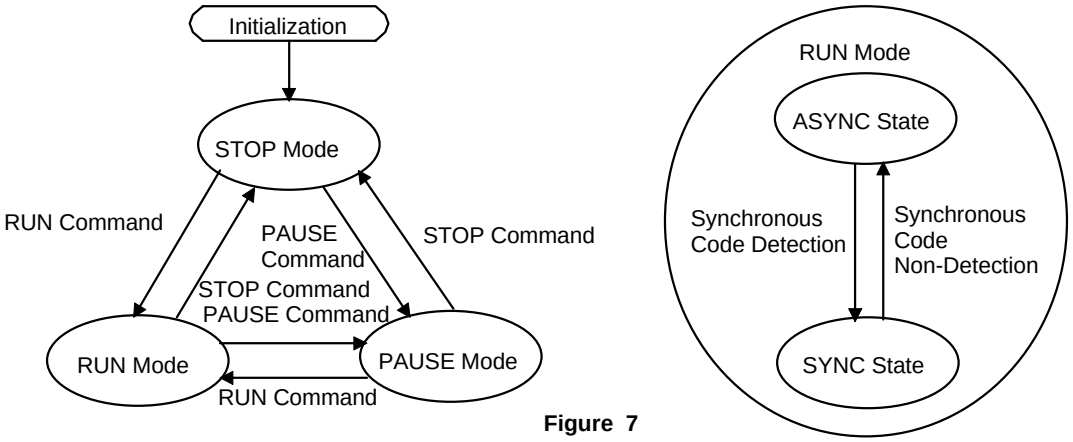


Figure 7

2.2 Establishing the Synchronization and Stopping the Reception

The S-70L41 incorporates an improved synchronous circuit with a digital filter. This allows a quick establishment of bit synchronization and word synchronization. After completion of word synchronization, the S-70L41 shifts to the Frame Search mode. In the Frame Search, the S-70L41 turns the BS1 to "L" up until the programmed frame timing, and only the programmed frame is retrieved. Even when there is no PREAMBLE, the S-70L41 can detect the synchronous code and shift to the Frame Search.
If an error of more than 3 bits occurs in the synchronous code during reception, the operation mode is shifted to the asynchronous state and the Frame Search stops. However, when the ADRS bit is "1", the Frame Search is performed excessively on the batch immediately following the errored synchronous code.

2.3 Detecting the Address

When a programmed address exists in the Frame, the S-70L41 sends an interrupt request to the host CPU and also starts receiving messages. Up to 6 addresses can be programmed into the IDROM. During initialization, addresses are sent from the host CPU to the decoder.
The latter half of the address word contains 11 bits that are check bits to detect errors using the BCH code. When a valid address word is received, it is compared with the six addresses, and if a match is found, the S-70L41 retrieves the message word. Invalid addresses are ignored. Error judgement can be selected by setting the bits of EE1 and EE0. When the same address code is programmed for a plural number of addresses and there is a page calling that address, the smallest number of the addresses is deemed to be received.

2.4 Detecting the Message

When the address word is detected, the S-70L41 receives subsequent message words. When the S-70L41 receives the message word, the LAST bit is cleared until the host CPU finishes reading the message. After reading the message, the host CPU displays it on the panel. The S-70L41 continues to receive the message words until the next address word or the idle word is received. If the S-70L41 fails to detect the synchronous code between message words, it concludes message reception. However, when the ADRS bit is set to “1”, the S-70L41 continues to receive the message words even after failing to receive the sychronous code once. It is after failing to detect the synchronous code twice in succession that the S-70L41 concludes message reception and shifts to the asynchronous mode.
The latter half of the address word contains 11 bits as check bits in order to detect an error using the BCH code. When an error is detected, the error is indicated by setting the flags in Status Register 0. When 4 bit or 7 bit data length is selected, error indication or end of transmission notification is performed by setting the bit(s) on the MSB side of data.

2.5 Buffering the Data

The S-70L41 incorporates a buffer register corresponding to one word. It can retain data of 26.7 msec. (min.) at 1200 bps and 13.3 msec. (min.) at 2400 bps. Therefore, when a twin clock type host CPU is used, it can wait for interrupts in Sub-clock Mode (76.8 kHz), receive the interrupt signal, and retrieve the data. After retrieving the data, the host CPU switches to Main Clock Mode, and continues data processing such as display. This allows current consumption of the user’s system to be significantly reduced.
The quartz crystal of the S-70L41 can be commonly used with the host CPU as a sub-clock by connecting (normally AC couple) the COUT terminal of the S-70L41 to the XIN terminal of the host CPU.

2.6 Reading the Received Data

When the address is detected, the S-70L41 sends an interrupt signal to the host CPU, and also stores the message in the Buffer Register. The host CPU, after receiving the interrupt signal, reads the message from the S-70L41 via the Serial Interface. The standard reading procedure is explained below. Please design accordingly.
First, the host CPU receives the interrupt signal. Next, the host CPU sends a Read Status 0 command to the decoder and simultaneously reads the contents of Status Register 1. The host CPU, then, determines whether or not the reception is valid from the contents of status register 1. If the reception is invalid (i.e. the decoder is not in the synchronous state, the OVFL flag is set, the register is in PAUSE Mode, etc.), it aborts reading the message and waits for the next Interrupt signal. If the reception is deemed valid, it continues to read the message by sending the Read DREG command to the S-70L41 while simultaneously reading the contents of Status Register 0. If there is no further message, a “1” is set as the LAST bit, the CPU stops reading the data, and sends out an alert signal. When a message still exists, it alternates sending between the Read Status 0 and the Read DREG commands (for the 8-bit data length). The $\overline{\text{BUSY}}$ terminal must be “H” before sending any commands.
The S-70L41 is provided with a data length conversion function. It can output the received message on a basis of a 4-bit or 7-bit division unit. In this case, errors or end of message notifications are indicated in the upper Nibble or in the MSB respectively. When 4-bit or 7-bit is the selected data length, the CPU reads only the data register, except for the first command after an interrupt, until it finds a “1” in the MSB telling it to read the contents of Status Register 0. Figure 8 shows the sequence of processing an interrupt .

■ S-70L41 Control Flow by a Host µP

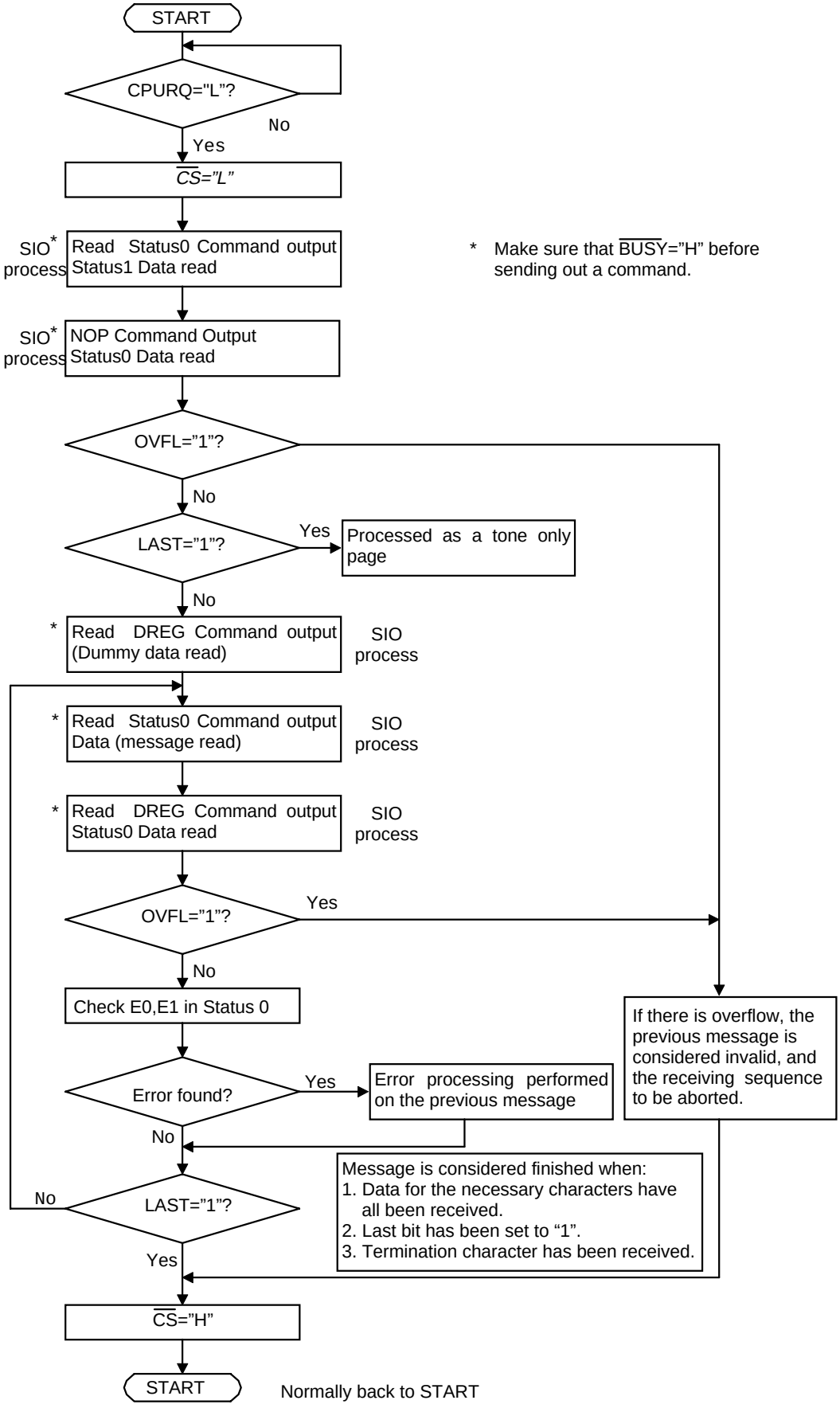


Figure 8

3. Interface to a Host CPU

3.1 Serial Interface Overview

When the control register is programmed during initialization, or an interrupt signal is received during data reception, the host CPU accesses the S-70L41 through the serial interface. The following 6 signal lines are connected between the S-70L41 and the host CPU:

(1) $\overline{CS}$: Signal for Interface Enable Control
When "H", the CPUDO becomes high-impedance, and the $\overline{CPUCK}$ and the CUPDI become invalid.

(2) $\overline{CPUCK}$: Synchronous Clock for Data Transmission to be input from the host CPU to the S-70L41. Data are output from the CPUDO at the falling edge and retrieved from the CPUDI at the rising edge.

(3) CPUDI : Signal for Data Transmission from Host CPU to S-70L41

(4) CPUDO : Signal for Data Transmission from S-70L41 to Host CPU

(5) $\overline{BUSY}$: Signal Showing that an Instruction is being executed inside the S-70L41.
When this signal is "L", the $\overline{CPUCK}$ is not accepted.

(6) $\overline{CPURQ}$: Signal informing CPU of reception of a call
This is usually cleared when setting the $\overline{CS}$ to "L" followed by reading Status1. However, when two or more calls occur, this signal is not cleared even after Status Register 1 is read.

The CPUDI, CPUDO, and $\overline{CPUCK}$ are compatible with a general-purpose SIO. Data are transmitted from the LSB on the basis of an 8-bit unit in succession. Figure 9 shows the timing chart.

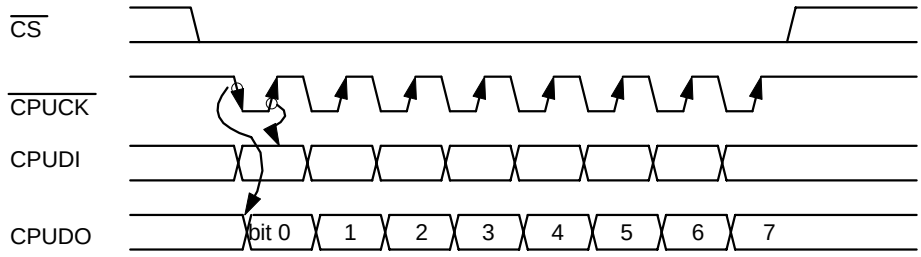


Figure 9

3.2 The code structure of a word and the order of the read-out bits

The code structure of a word

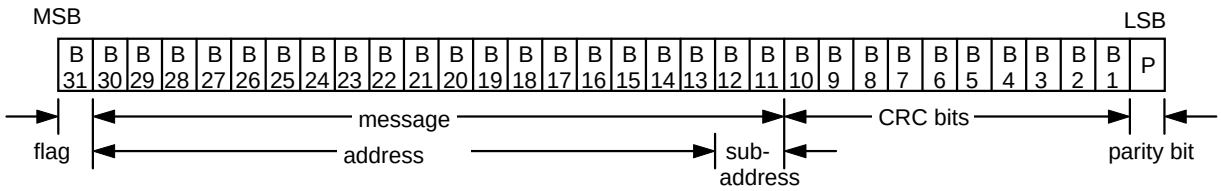
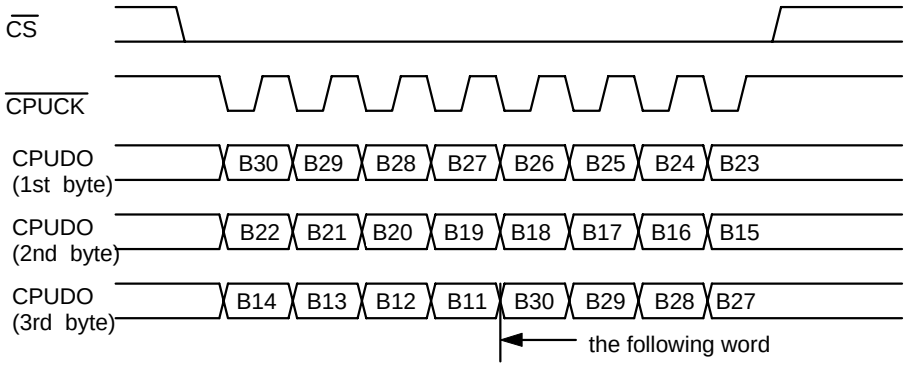
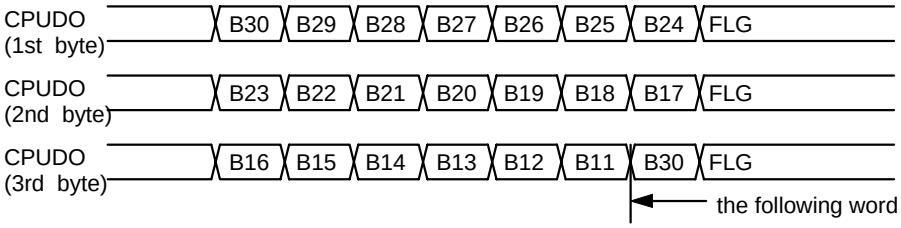


Figure 10

The order of the read-out bits 1 : data length = 8 bits



The order of the read-out bits 2 : data length = 7 bits



The order of the read-out bits 3 : data length = 4 bits

Figure 11

3.3 Relationship between Call Information and $\overline{CS}$

When the call signal is received, the S-70L41 sets the $\overline{CPURQ}$ to “L” and sends the Interrupt signal to the host CPU. The host CPU sets the $\overline{CS}$ to “L” and reads the call information. Please turn the $\overline{CS}$ back to “L” after every call. After reading all of the information in the call, turn the $\overline{CS}$ back to “H”. If the $\overline{CPURQ}$ remains “L” even after turning the $\overline{CS}$ to “H”, it means there is another incoming call. Turn the $\overline{CS}$ “L” again, and have the call information read by the host CPU (see Figure 12).

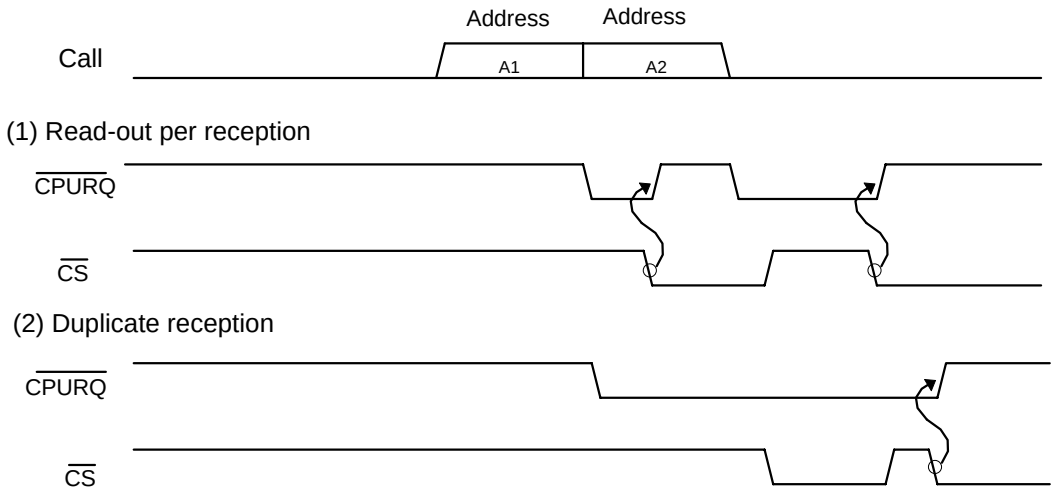


Figure 12

3.4 Serial Interface Timing in Detail

Serial interface timing is described in detail in the following (Fig 13, Table 9):

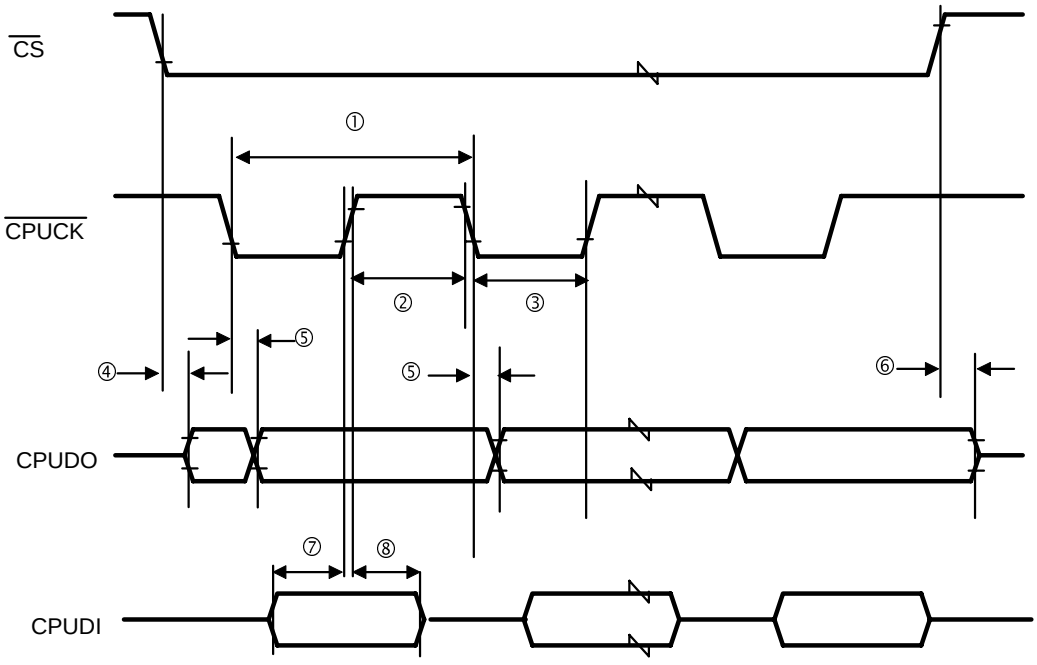


Figure 13 Serial CPU Interface Timing Chart

Table 9
(Unless otherwise stated Ta=25°C V_{DD1}=1.5V Output terminal load Cl=75pF)

No.	Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
①	Serial Clock Cycle Time	Tcy	V_{DD2}=1.5V	5.0			uS
			V_{DD2}=3.0V	2.0			
②	Serial Clock Pulse Width “H”	Tch	V_{DD2}=1.5V	2.5			
			V_{DD2}=3.0V	1.0			
③	Serial Clock Pulse Width “L”	Tcl	V_{DD2}=1.5V	2.5			
			V_{DD2}=3.0V	1.0			
④	Data Output Delay Time	Tdc	V_{DD2}=1.5V			2.0	
			V_{DD2}=3.0V			1.0	
⑤	Data Output Delay Time	Tdk	V_{DD2}=1.5V			2.0	
			V_{DD2}=3.0V			1.0	
⑥	Data Output End Time	Tde	V_{DD2}=1.5V			2.0	
			V_{DD2}=3.0V			1.0	
⑦	Data Set-up Time	Tds	V_{DD2}=1.5V	0.1			
			V_{DD2}=3.0V	0.1			
⑧	Data Hold Time	Tdh	V_{DD2}=1.5V	0.1			
			V_{DD2}=3.0V	0.1			

3.5 Reading SC in the Status register

The end of the message is recognized by the LAST flag being set. In order to know if the LAST flag was set due to the SC. loss the following operation is necessary. When the host μP finds that the message is over, turn the $\overline{CS}$ back to “H” and then again drive it down to “L” to read status 1. If the SC. bit is “0”, the loss of SC. is the cause of the set of the LAST flag. On the other hand, if the SC. bit is found to be “1”, the detection of an unmatched address or an idle code is regarded as the trigger to indicate the end of the message setting the LAST flag.

4. ERROR CORRECTION

4.1 Number of Bits for Error Correction

Error correction of up to 2 bits is available. The number of bits to be corrected is assigned via the EE bits as shown below in Table 10. If the number of error bits in a received address exceeds the number shown in Table 10, S-70L41 will ignore the address.

Table 10

EE1, EE0	Number of Correctable Error Bits	Status Reference Flag
0, 0	BCH Error of 2 Bits or Less "2"	Prohibited
0, 1	Error Correction Prohibited "0"	Set for 1 or more error bits
1, 0	BCH Error of 1 Bit "1"	Set for 2 or more error bits
1, 1	BCH Error of 2 Bits or Less "2"	Set for 3 or more error bits

4.2 Annotation of the Number of Error Bits

After error detection is performed, the S-70L41 saves the number of error bits in the E1 and E0 bits of the Status Register as shown below.

Table 11

BCH Error	Parity Error	E1, E0
None	No	0, 0
None	Yes	0, 1
1 bit	No	0, 1
1 bit	Yes	1, 0
2 bits	No	1, 0
2 bits	Yes	1, 1
3 bits or more	Does not matter	1, 1

4.3 Error Update Information

When a message is received, the BCH error is detected for every word. Information about the error is stored in the Status Register. When 4-bit or 7-bit data length is selected, the Status Reference Flag is selected at the same time.
The above error information is updated each time a new word is stored in the Buffer Register. Consequently, it is necessary to take into account the number of errors detected in the previous word when a set of data bits, representing a character, etc., is placed across two words. For example, assume that the first word has two errors and the second has none, and there are a number of bits representing a character starting in the first word and ending in the second. When this happens, the host CPU can display the character only after reading the second word and finding no errors in the Status Register. Thus, the CPU may ignore the error bits that might have existed in the character. Therefore, it is recommend for users to buffer the error information in the host CPU.

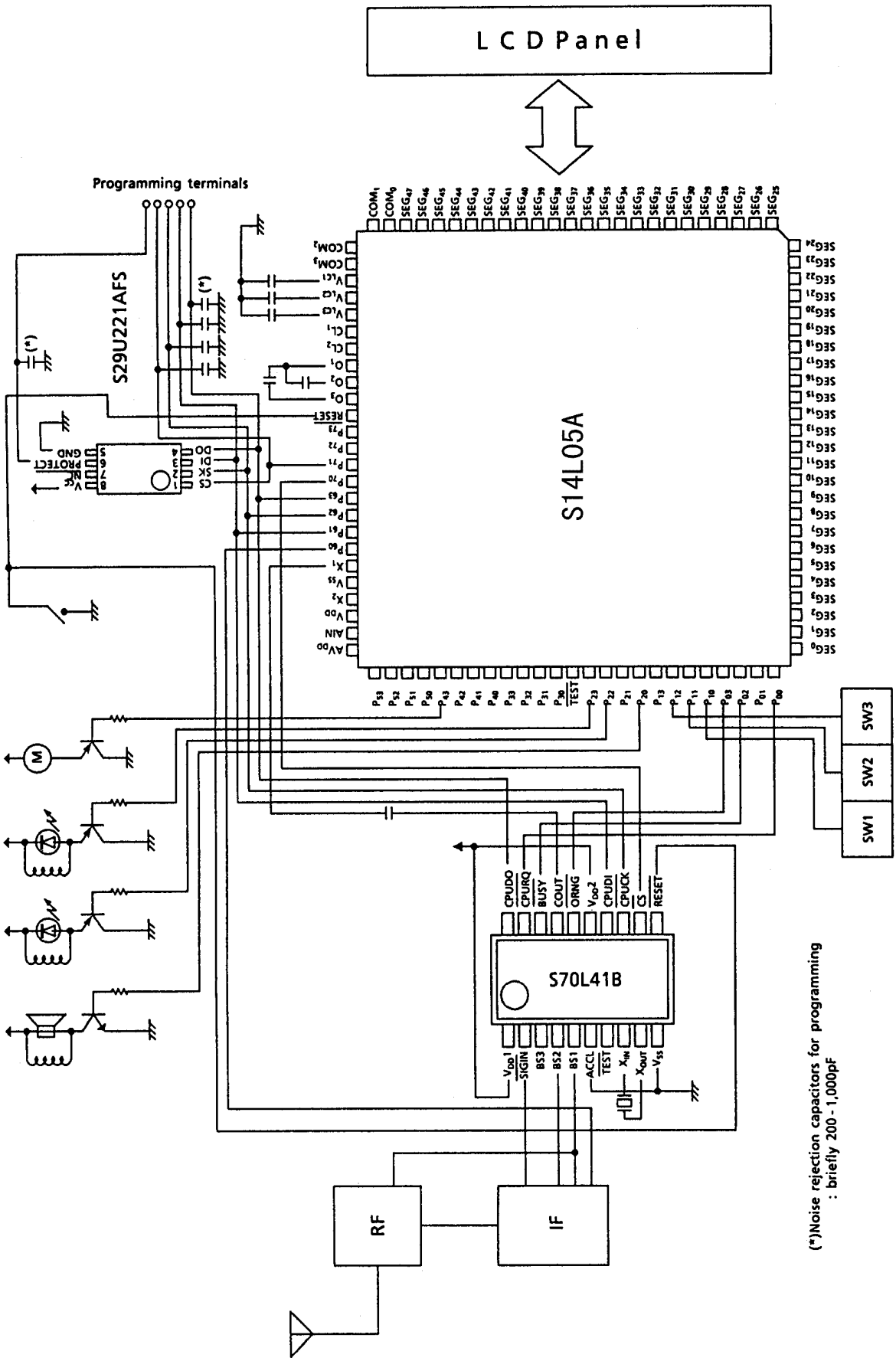


Figure 14. Application circuit example

Notes for the Paging Decoder ICs

- Please note that the products incorporating these ICs may infringe a patent depending upon applications, including the one in this document, the specifications of the products, and countries to which they are supplied.
- In the event that the aforesaid products including these ICs infringe a patent, Seiko Instruments Inc. shall not bear any responsibility for any matters with regard to and arising from such patent infringement.

Collection of Product FAQs

Author: Shirai Masaaki Date: 99/01/12 (Tuesday) 17:09 (modified: 99/01/12(Tuesday))

<Information level>

A: Public (Printing O.K.)

Index: B: Technical

<Product>

Division name: 01 IC

Category 1: 17 ASSP

Category 2: 1. paging decoder

Cal No.: S70L41B

Related documents:

Question:

What are the recommended quartz resonator and external Cg values?

Answer:

Recommended quartz resonator: VTC-200 (76.8 kHz) manufactured by SII

Load capacity: 12 PF

Recommended Cg value: 15 PF

<Remarks>

FAQ No.: 17S70L4001