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# HA11575F

## Satellite Broadcast Tuner

### FM Demodulator IC

Rev. 0  
Feb. 1994

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#### Functions

- IF amplifier (with built-in IF AGC)
- PLL FM detection
- AGC detection
- First AGC output
- AFC (supports keyed AFC)
- Digital AFC output
- Video amplifier
- Supports both the Japanese reception specifications (an IF frequency of 403 MHz) and the European reception specifications (an IF frequency of 480 MHz).
- Provides digital AFC outputs. Digital AFC output polarity: (H, H) when tuned.
- Provides a keyed AFC pulse input pin to support MUSE reception.
- The video output level can be adjusted with an external resistor up to a maximum output of 1 Vp-p.

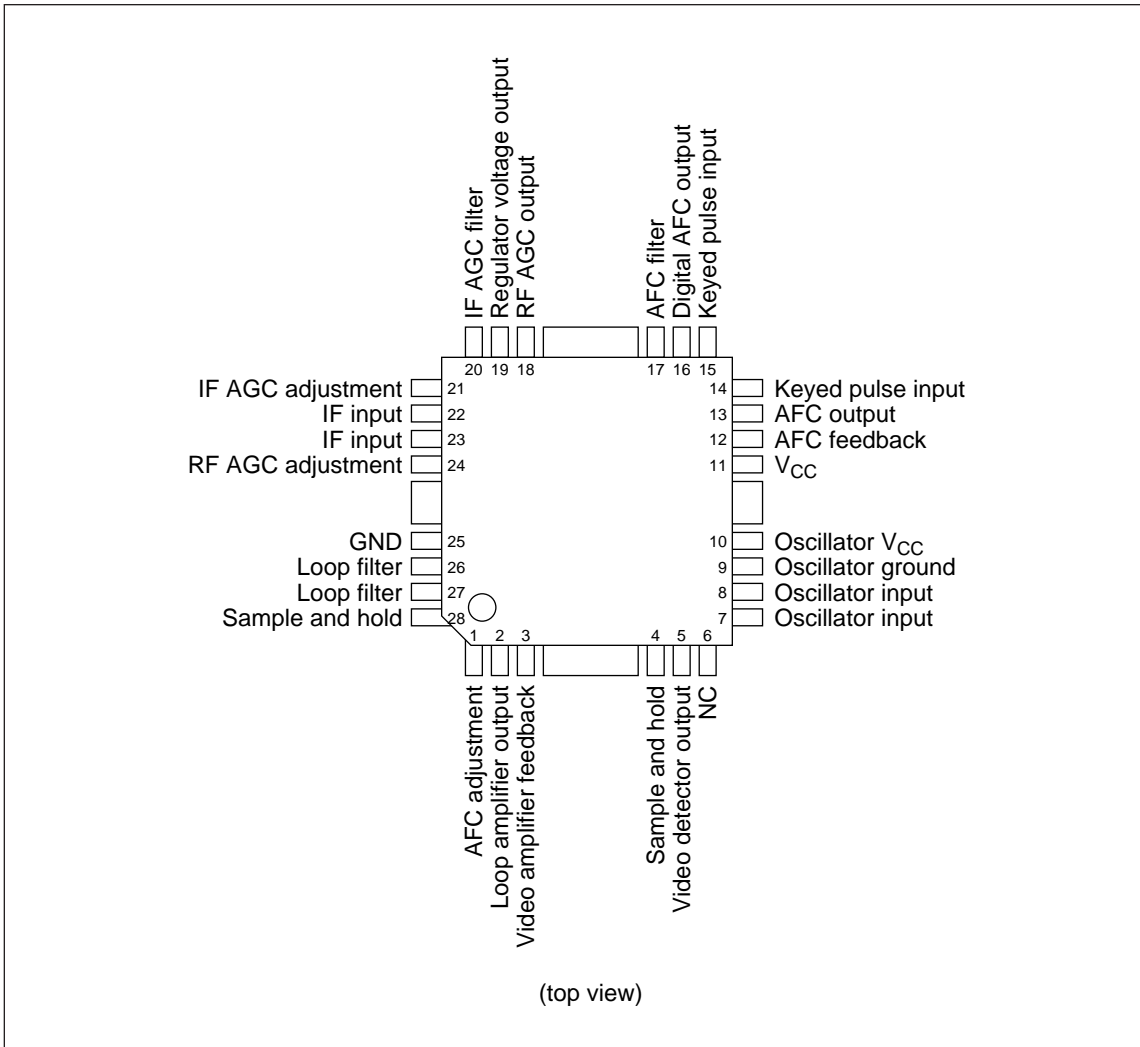
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#### Features

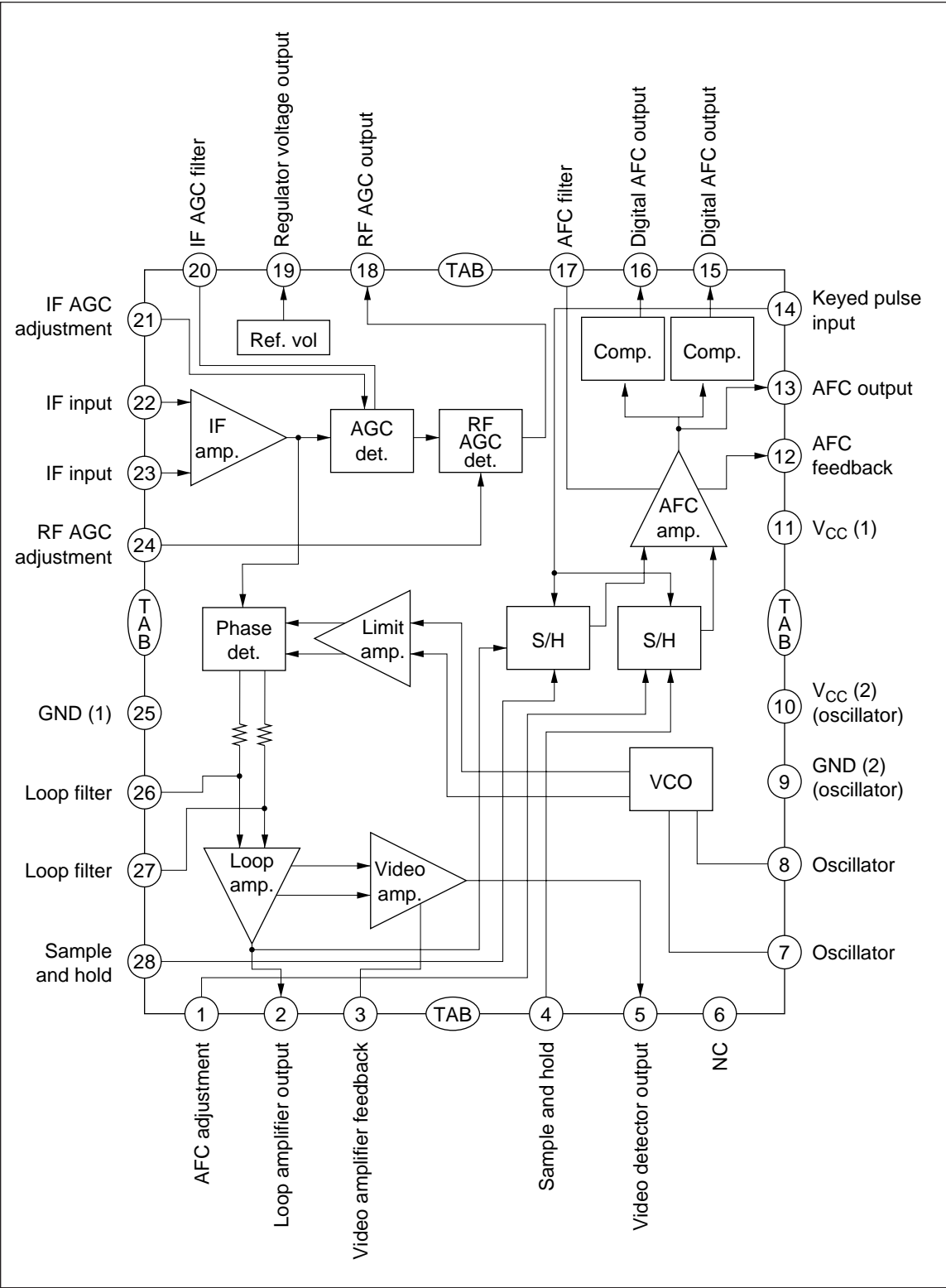
- Can be used with a single voltage 5 V power supply.
- Uses an averaging VCO to provide stable characteristics.
- Includes a built-in IF AGC to provide stable PLL demodulation characteristics.
- The AFC sensitivity can be set with external components.
- The first AGC output voltage gain has been improved over that of earlier products.

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## Pin Arrangement

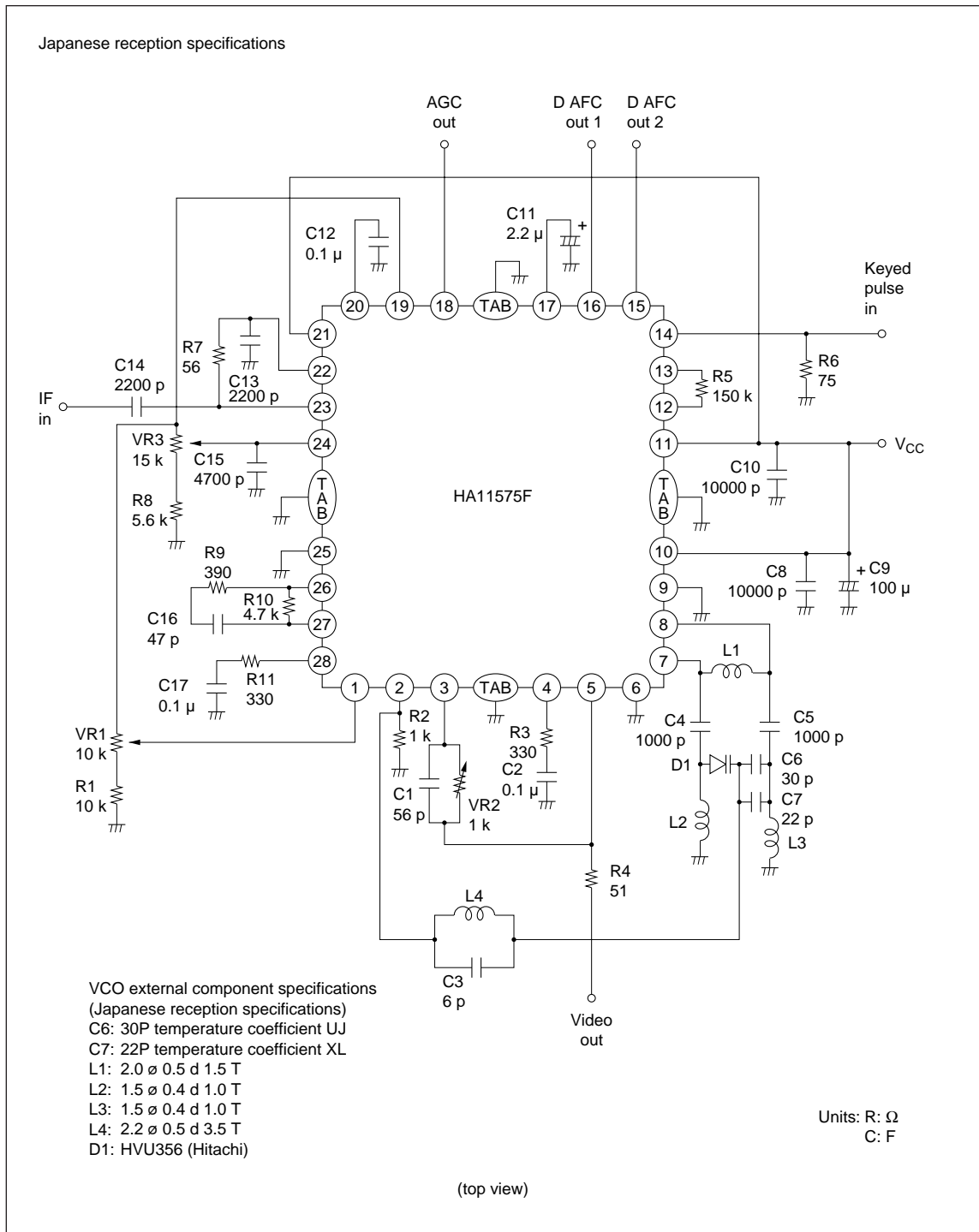


Block Diagram



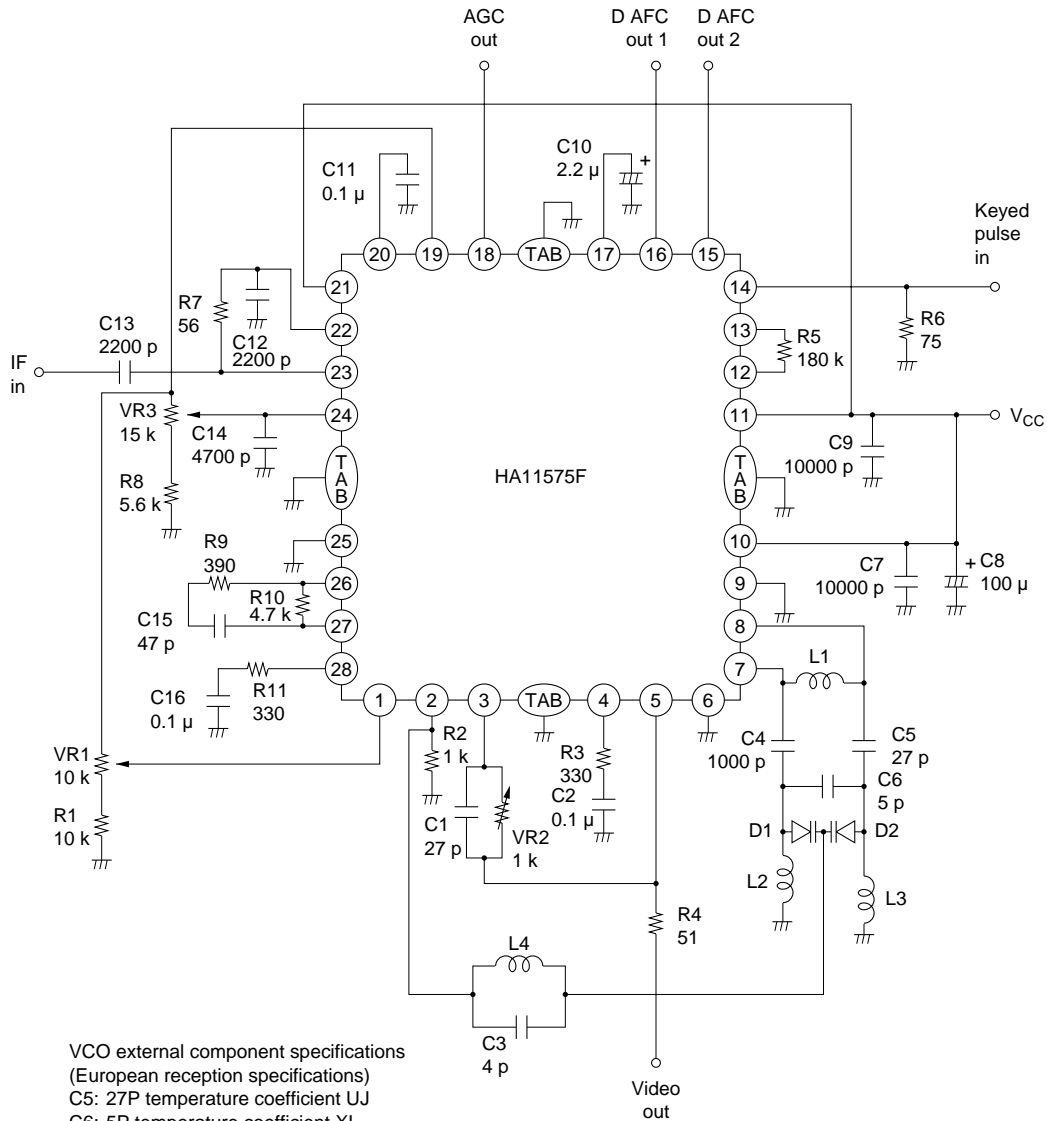
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## Standard External Circuits



Standard External Circuits

European reception specifications



- VCO external component specifications  
(European reception specifications)
- C5: 27P temperature coefficient UJ
  - C6: 5P temperature coefficient XL
  - L1: 1.5 ∅ 0.5 d 1.5 T
  - L2: 2.6 ∅ 0.5 d 2.0 T
  - L3: 2.6 ∅ 0.5 d 2.0 T
  - L4: 2.2 ∅ 0.5 d 3.5 T
  - D1: HVU356 (Hitachi)
  - D2: HVU356 (Hitachi)

Units: R: Ω  
C: F

(top view)



**IC Mounted Characteristics**

| Item                                | Symbol | Min | Typ  | Max | Unit |
|-------------------------------------|--------|-----|------|-----|------|
| Signal to noise ratio at CN = 14 dB | SN1    | —   | 38.5 | —   | dB   |
| Signal to noise ratio at CN = ∞     | SN2    | —   | 50   | —   | dB   |
| Threshold C/N                       | CN     | —   | 7.3  | —   | dB   |
| Differential gain                   | DG     | —   | 2    | —   | %    |
| Differential phase                  | DP     | —   | 2    | —   | deg  |
| CS mode                             | IM2    | —   | 50   | —   | dB   |
|                                     | IM3    | —   | 50   | —   | dB   |

**Absolute Maximum Ratings (Ta = 25°C)**

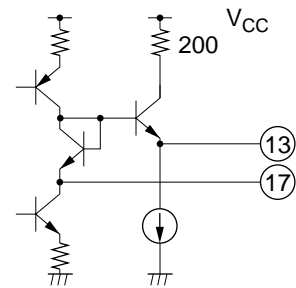
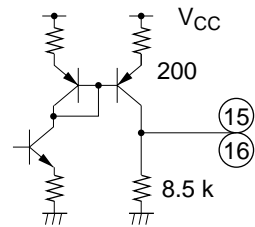
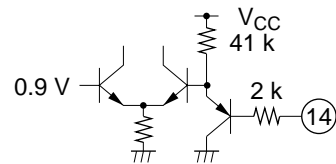
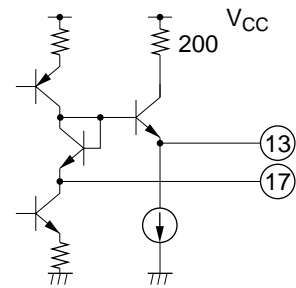
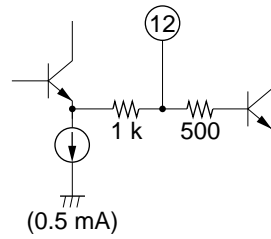
| Item                        | Symbol          | Rated Value | Unit |
|-----------------------------|-----------------|-------------|------|
| Power supply voltage        | V <sub>CC</sub> | 6.0         | V    |
| Allowable power dissipation | P <sub>T</sub>  | 630         | mW   |
| Operating temperature       | Topr            | -10 to +80  | °C   |
| Storage temperature         | Tstg            | -55 to +125 | °C   |

**Electrical Characteristics (Ta = 25°C)**

| Item                                      | Symbol            | Min  | Typ  | Max  | Unit | Test Conditions                                | Pins   |
|---|-------------------|------|------|------|------|--|--------|
| Current drain                             | I <sub>CC</sub>   | 58   | 83   | 100  | mA   | Pins 10 and 11, V <sub>CC</sub> = 5 V (1.6 mA) | 10, 11 |
| IF input maximum sensitivity              | V <sub>is</sub>   | -60  | -52  | -46  | dBm  |  | 22, 23 |
| PLL pull-in range (+)                     | f <sub>CRH</sub>  | 15   | 23   | —    | MHz  | V <sub>CC</sub>                                | 5      |
| PLL pull-in range (-)                     | f <sub>CRL</sub>  | —    | -23  | -15  | MHz  |  |        |
| Video amplifier frequency characteristics | B <sub>V</sub> A  | -0.6 | 0    | 0.6  | dB   | f = 500 kHz to 8.1 MHz                         |        |
| First AGC output voltage high level       | V <sub>2AGH</sub> | 3.9  | 4.2  | 4.6  | V    | (3 mA)   | 18     |
| First AGC output voltage low level        | V <sub>2AGL</sub> | 0    | 0    | 0.5  | V    |  |        |
| Second AGC output voltage high level      | V <sub>1AGH</sub> | 4.2  | 4.6  | 4.9  | V    | With the VCO oscillator stopped                | 20     |
| Second AGC output voltage low level       | V <sub>1AGL</sub> | 0    | 0.2  | 0.7  | V    | V <sub>CC</sub>                                |        |
| Analog AFC output voltage high level      | V <sub>AFH</sub>  | 3.25 | 3.45 | 3.65 | V    | 400 ohm resistors                              | 13     |
| Analog AFC output voltage low level       | V <sub>AFL</sub>  | 1.25 | 1.45 | 1.65 | V    |  |        |
| Digital AFC output voltage high level     | V <sub>DFH</sub>  | 4.0  | 4.6  | —    | V    |  | 15, 16 |
| Digital AFC output voltage low level      | V <sub>DFL</sub>  | —    | 0    | 0.5  | V    |  |        |

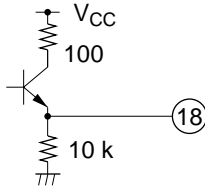
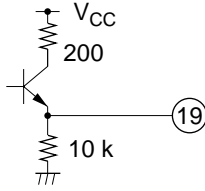
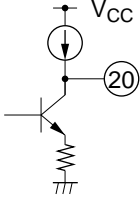
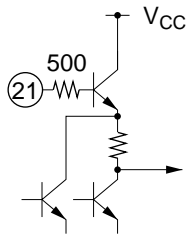
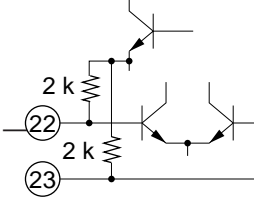
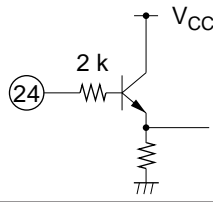
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|                       |       |     |   |      |   |    |
|-----------------------|-------|-----|---|------|---|----|
| Keyed AFC on voltage  | Vkon  | 0.4 | — | —    | V | 14 |
| Keyed AFC off voltage | Vkoff | —   | — | 0.05 | V |    |





**Pin Interface**

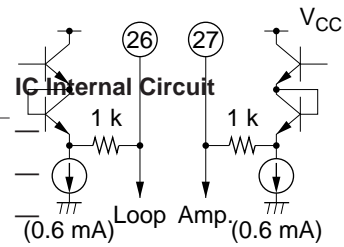
| Pin No. | Function                                    | Average DC Voltage * (V)                                      | IC Internal Circuit  |
|---------|---|---|--|
| 1       | AFC adjustment                              | —<br>(Adjust to 2.5 V when measuring voltages on other pins.) |   |
| 2       | Loop amplifier output                       | 2.4   |  |
| 3       | Video amplifier feedback                    | 2.3   |   |
| 4       | Sample and hold<br>(reference voltage side) | 3.2   |  |
| 5       | Video detector output                       | 2.3   |  |
| 6       | NC pin                                      | —   |  |
| 7       | Oscillator                                  | 4.4   |  |
| 8       | Oscillator                                  | 4.4   |  |

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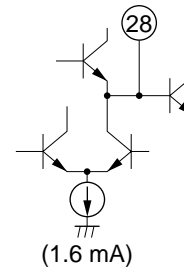
Note: \* When the input is  $V_{in} = -35$  dBm.

## Pin Interface (cont)

| Pin No. | Function                  | Average DC Voltage * (V) |
|---------|---------------------------|--------------------------|
| 9       | GND (2) (oscillator)      | —                        |
| 10      | $V_{CC}$ (2) (oscillator) | —                        |
| 11      | $V_{CC}$ (1)              | —                        |
| 12      | AFC feedback              | 1.9                      |



|    |            |     |
|----|------------|-----|
| 13 | AFC output | 2.5 |
|----|------------|-----|



|    |                   |   |
|----|-------------------|---|
| 14 | Keyed pulse input | — |
|----|-------------------|---|

|    |                    |     |
|----|--------------------|-----|
| 15 | Digital AFC output | 4.6 |
|----|--------------------|-----|

16

|    |            |     |
|----|------------|-----|
| 17 | AFC filter | 2.5 |
|----|------------|-----|

22 IF input 2.5

23 2.5

Note: \* When the input is  $V_{in} = -35$  dBm.

**Pin Interface (cont)**

| Pin No. | Function      | Average DC IC Internal |
|---------|---------------|------------------------|
| 18      | RF AGC output | 2.0                    |

|    |   |                   |
|----|---|-------------------|
| 24 | RF AGC adjustment                       | —                 |
|    | when measuring voltages on other pins.) | (Adjust to 2.2 V) |

Note: \* When the input is  $V_{in} = -35$  dBm.

**Pin Interface (cont)**

|    |                          |     |
|----|--------------------------|-----|
| 19 | Regulator voltage output | 2.9 |
|----|--------------------------|-----|

|    |               |     |
|----|---------------|-----|
| 20 | IF AGC filter | 2.4 |
|----|---------------|-----|

|    |   |                 |
|----|---|-----------------|
| 21 | IF AGC adjustment                       | —               |
|    | when measuring voltages on other pins.) | (Adjust to 5 V) |

| Pin No. | Function | Average DC IC Internal |
|---------|----------|------------------------|
|---------|----------|------------------------|

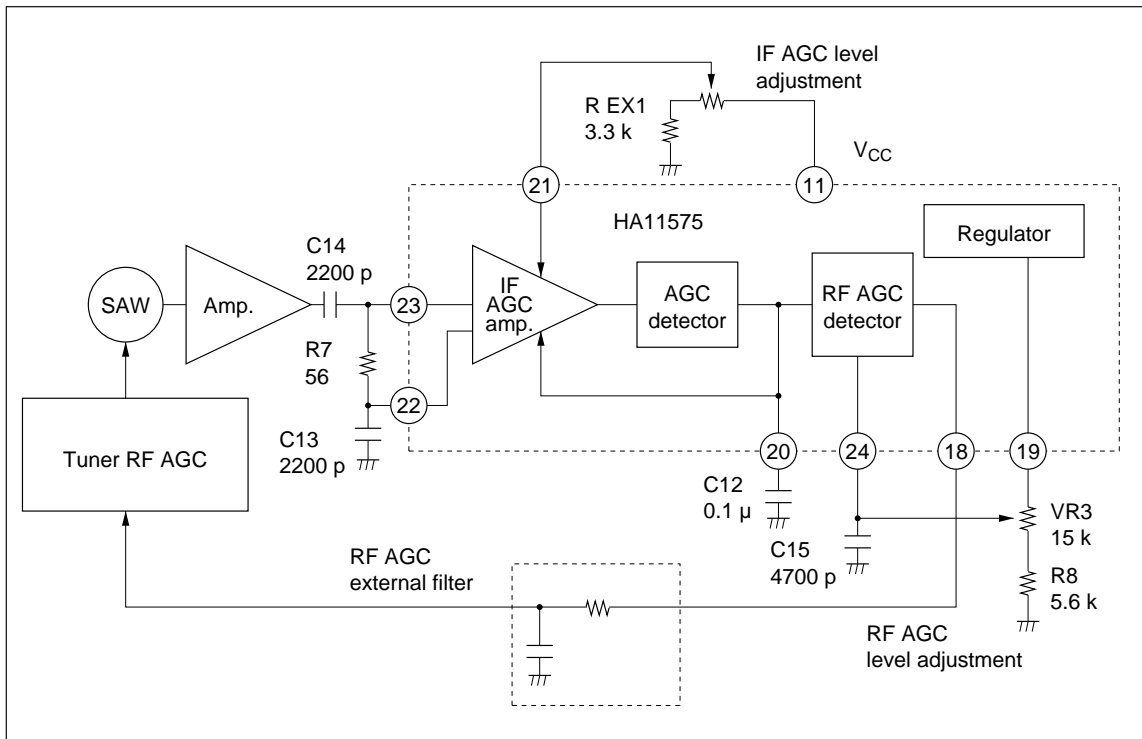
|    |     |   |
|----|-----|---|
| 25 | GND | — |
|----|-----|---|

|    |                                     |     |
|----|-------------------------------------|-----|
| 26 | Loop filter (phase detector output) | 3.0 |
|----|-------------------------------------|-----|

|    |  |     |
|----|--|-----|
| 27 |  | 3.0 |
|----|--|-----|

|    |                               |     |
|----|-------------------------------|-----|
| 28 | Sample and hold (signal side) | 3.2 |
|----|-------------------------------|-----|

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Note: \* When the input is  $V_{in} = -35$  dBm.

**Block Functional Descriptions**

**IF Amplifier and AGC Circuit**

Figure 1 shows the block diagram of the AGC circuit.

This IC includes a built-in RF AGC control circuit that controls the gains of the IF AGC circuit and the external RF amplifier so that the IC maintains a fixed signal processing level and performs stable signal processing.

The AGC circuit can be adjusted using pin 21 (IF AGC adjustment) and pin 24 (RF AGC adjustment).

**AGC Adjustment:** When adjusting the AGC settings, first adjust the IF AGC and then adjust the RF AGC. If the RF AGC is adjusted first, its setting will be changed by changes made in adjusting the IF AGC. On the other hand, adjustments to the RF AGC have no influence on the IF AGC and do not change the IF AGC setting.

- IF AGC adjustment procedure  
The IF AGC is normally used without adjustment. The standard setting for the IF AGC adjustment is to connect pin 21 to the power supply.  
If the IF AGC adjustment voltage (pin 21) is set to a voltage lower than the power supply voltage, use a resistor voltage divider to create the setting voltage using the power supply as the reference voltage.  
If the pin 21 voltage is to be adjusted on every circuit board, construct the adjustment voltage circuit taking the power supply as the reference. (See figure 1.)  
The voltage range for the IF AGC adjustment is about 3.8 V to 5.0 V when a 5.0 V power supply is used. As the adjustment voltage is lowered, the phase detector input signal level is reduced and the PLL loop gain is also reduced. As a result, changing the pin 21 voltage changes the video detector output S/N characteristics and the PLL loop response characteristics.

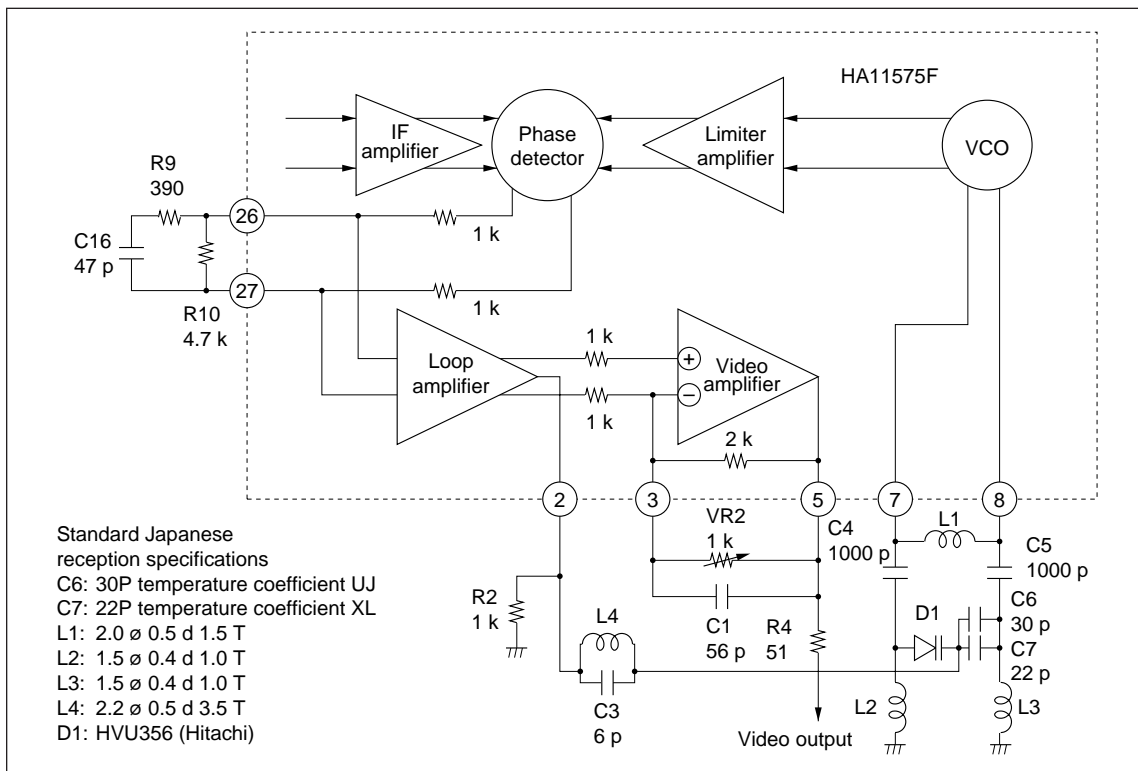
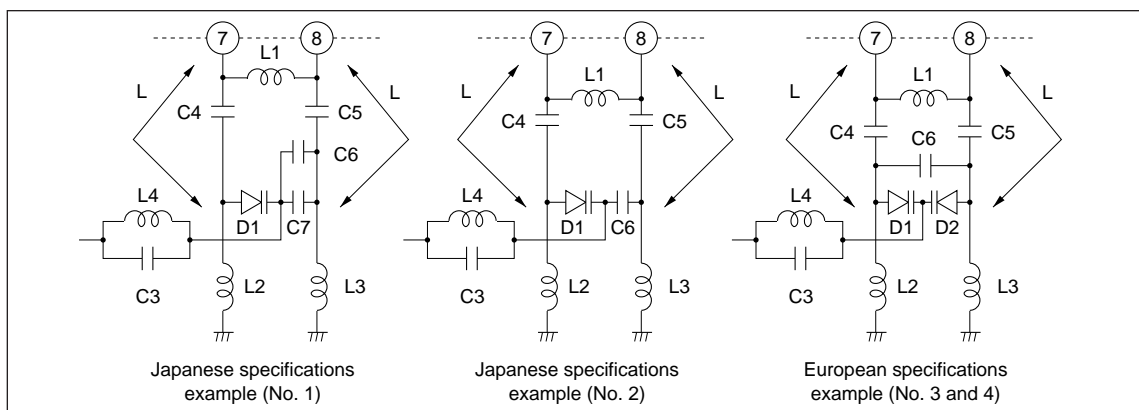


Figure 2 FM Demodulator Circuit

- RF AGC adjustment procedure**  
 The RF AGC adjustment should be set so that the IC input signal level is in the range  $-27$  dBm to  $-35$  dBm. Furthermore, the IC input level should be set to the same level for all units produced to reduce variations in characteristics between units.  
 The RF AGC adjustment voltage should be generated using a resistor voltage divider including a variable resistor (trimmer) and the regulator power supply (pin 19). (See figure 1.)  
 The main characteristics of the RF AGC circuit (when a 5 V power supply voltage is used) are as follows:

**Table 1 VCO External Circuit Component Value Examples**

| Specification    | External Circuit Component Values |                                   |                                   |                                   |     |        |              |              |              |                         |                         | VCO Control Sensitivity | VCO Temperature Characteristics, $-10^{\circ}\text{C}$ to $70^{\circ}\text{C}$ |
|------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----|--------|--------------|--------------|--------------|-------------------------|-------------------------|-------------------------|--|
|                  | No.                               | L1                                | L2, 3                             | L4                                | C3  | C4     | C5           | C6           | C7           | D1                      | D2                      |                         |  |
| 403 MHz (Japan)  | 1                                 | 2.0 $\emptyset$<br>0.5 d<br>1.5 T | 1.5 $\emptyset$<br>0.4 d<br>1.0 T | 2.2 $\emptyset$<br>0.5 d<br>3.5 T | 6 p | 1000 p | 1000 p       | 30 p<br>(UJ) | 22 p<br>(XL) | HVU<br>356<br>(Hitachi) | —                       | About 31 MHz/V          | $\pm 0.5$ MHz  |
|                  | 2                                 | 2.0 $\emptyset$<br>0.5 d<br>1.5 T | 1.5 $\emptyset$<br>0.4 d<br>1.0 T | 2.2 $\emptyset$<br>0.5 d<br>3.5 T | 6 p | 1000 p | 1000 p       | 51 p<br>(UJ) | —            | HVU<br>356<br>(Hitachi) | —                       | About 31 MHz/V          | $\pm 2.5$ MHz  |
| 480 MHz (Europe) | 3                                 | 1.5 $\emptyset$<br>0.5 d<br>1.5 T | 2.6 $\emptyset$<br>0.5 d<br>2.0 T | 2.2 $\emptyset$<br>0.5 d<br>3.5 T | 4 p | 1000 p | 27 p<br>(UJ) | 5 p<br>(XL)  | —            | HVU<br>356<br>(Hitachi) | HVU<br>356<br>(Hitachi) | About 34 MHz/V          | $\pm 0.5$ MHz  |
|                  | 4                                 | 1.5 $\emptyset$<br>0.5 d<br>1.5 T | 2.6 $\emptyset$<br>0.5 d<br>2.0 T | 2.2 $\emptyset$<br>0.5 d<br>3.5 T | 4 p | 1000 p | 27 p<br>(UJ) | 5 p<br>(UJ)  | —            | HVU<br>356<br>(Hitachi) | HVU<br>356<br>(Hitachi) | About 34 MHz/V          | $\pm 2.5$ MHz  |



**Figure 3 VCO External Circuit Examples**

Adjustment voltage range (pin 24):  
 About 1.5 V to 3.0 V  
 (for an IC input range of  
 -27 dBm to -35 dBm.  
 See figure 6.)

Control output voltage (pin 18):  
 0 V to 4 V  
 (See figure 5.)

Control sensitivity: About 2 V/dB

Output drive current (pin 18):  
 1 mA (maximum)

Polarity: Reverse polarity

Since the RF AGC circuit is a reverse polarity circuit, an external inverter must be provided if a forward type RF AGC circuit is used.

If a signal with residual AM components enters the IC, it is possible for an AM detected voltage to appear on the RF AGC output and for sag to occur in the detector output. If this is a problem, the sag can be corrected by adding the RF AGC external filter on pin 18 as shown in figure 1. However, since the RF AGC response is slowed by the time constant of the filter, be sure to check the response characteristics.

**Figure 1 AGC Circuit Block Diagram**

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**Table 2 AFC Polarities**

| AFC Type | Corresponding Pin | Input Frequency               |        |                                |
|----------|-------------------|-------------------------------|--------|--------------------------------|
|          |                   | Detuned (low frequency input) | Tuned  | Detuned (high frequency input) |
| Analog   | 13                | High                          | Middle | Low                            |
| Digital  | 15                | Low                           | High   | High                           |
|          | 16                | High                          | High   | Low                            |

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## FM Demodulator Circuit

Figure 2 shows the block diagram of the FM demodulator circuit.

The FM demodulator circuit consists of five blocks, a phase detector, a loop amplifier, a VCO, a video amplifier and a limiter amplifier. Structurally, the FM demodulator outputs the control voltage of the PLL circuit synchronized with the IC's input signal frequency as the demodulated signal.

**Loop Amplifier:** The loop amplifier amplifies the phase detector output. The loop amplifier output (from pin 2) drives the VCO's variable capacitance diode. The loop filter is formed on pins 26 and 27.

This loop filter determines the PLL loop frequency response characteristics. The loop filter consists of the two IC internal 1 kΩ phase detector output resistors and the external filter circuit connected to pins 26 and 27.

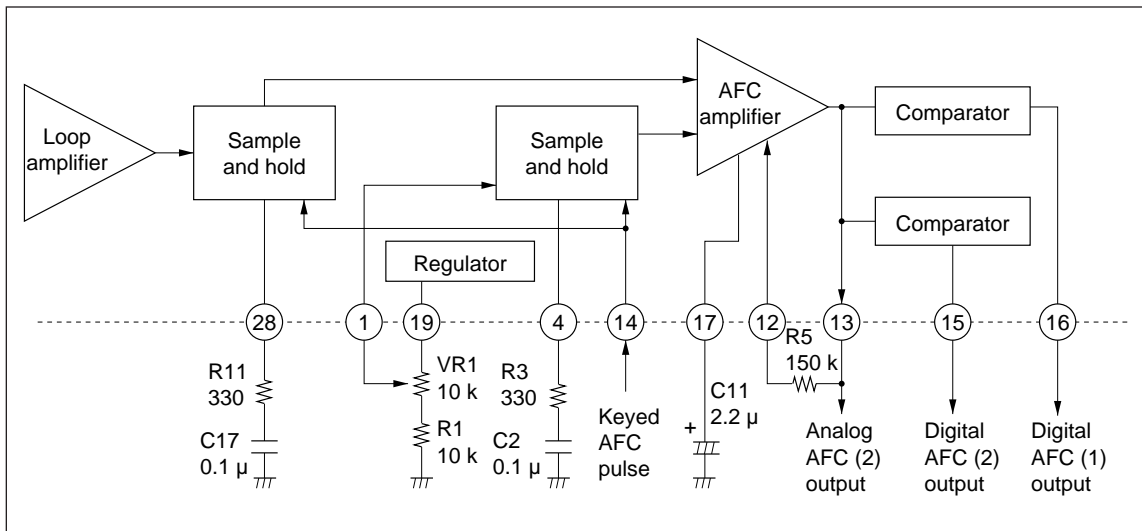
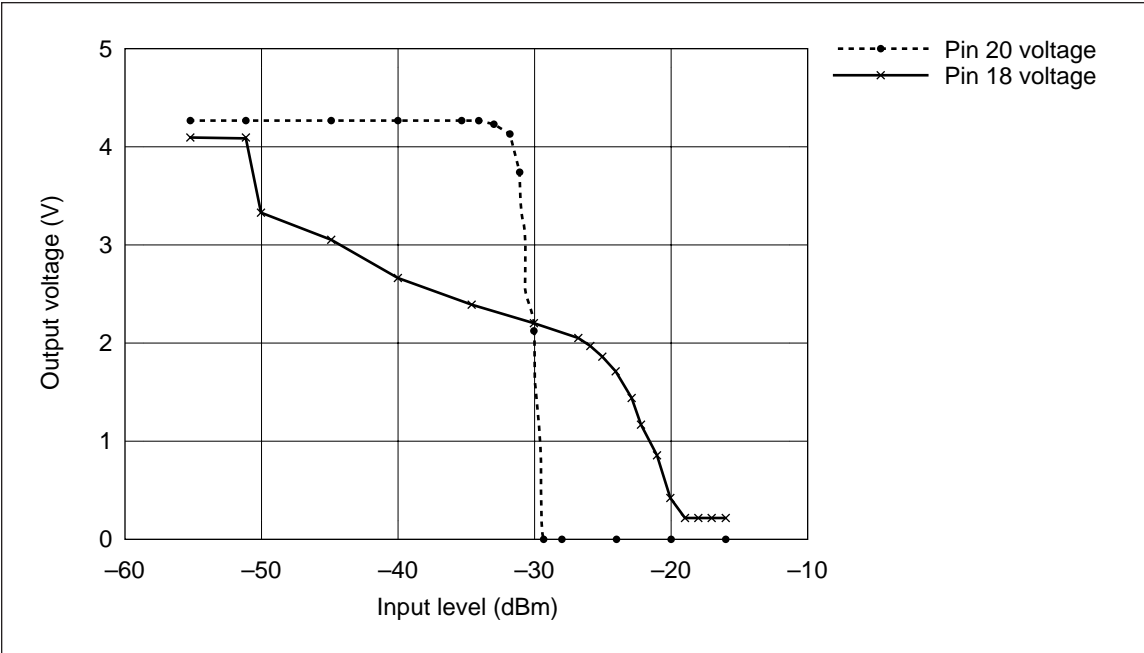
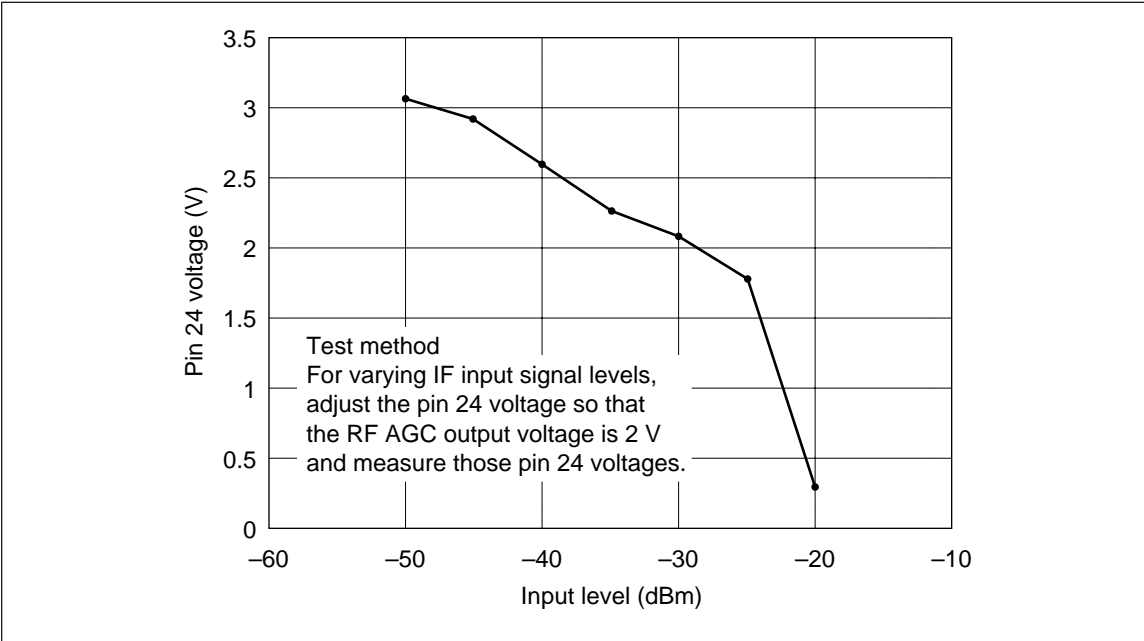


Figure 4 AFC Block Diagram





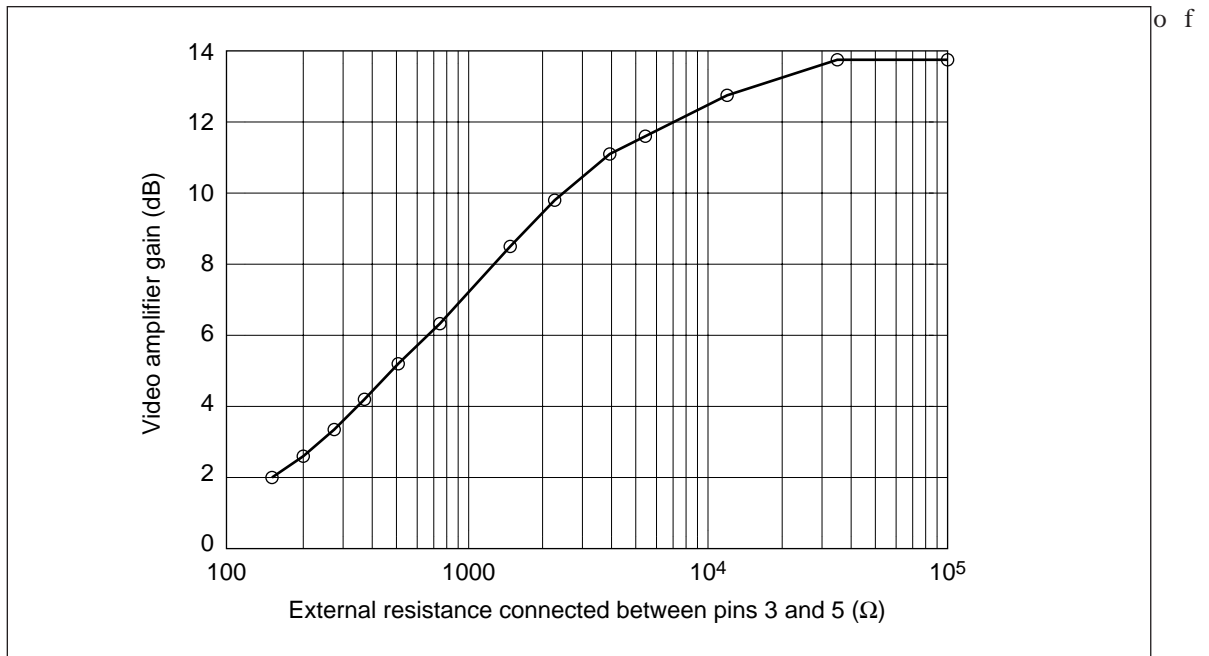
The resistor R10 connected between pins 26 and 27 (see figure 2) lowers the loop gain of the PLL loop and improves the signal to noise ratio characteristics. However, if a resistor of under



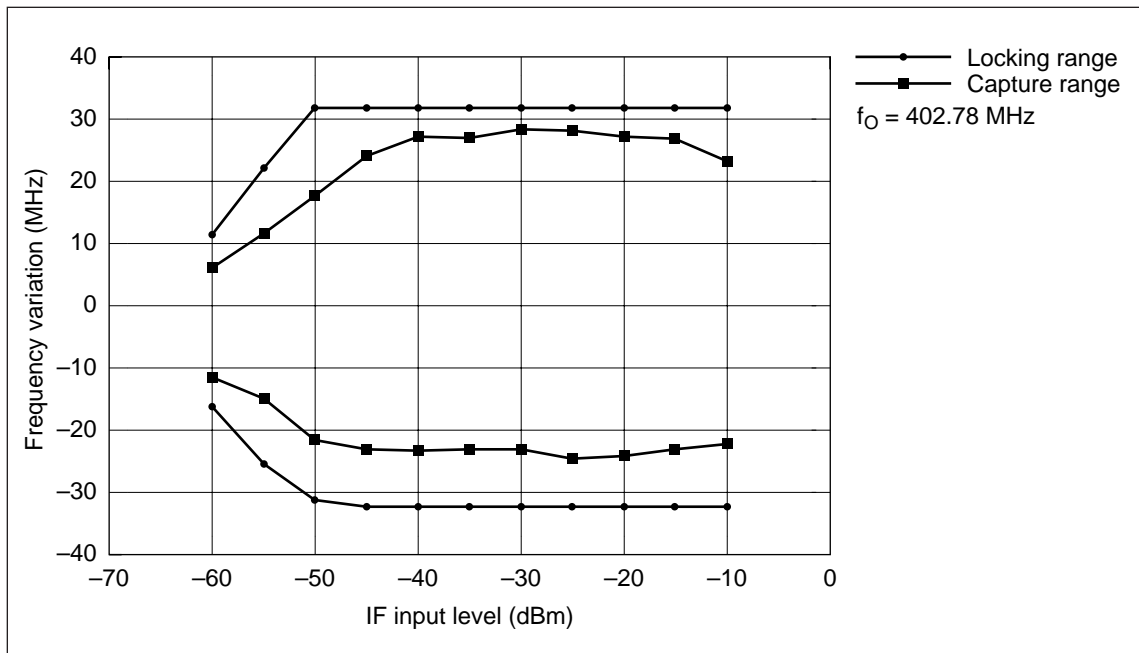
3.0  
 kΩ  
 is

used, the loop gain will be reduced excessively, and sparkle noise degradation may occur. Therefore, a resistor

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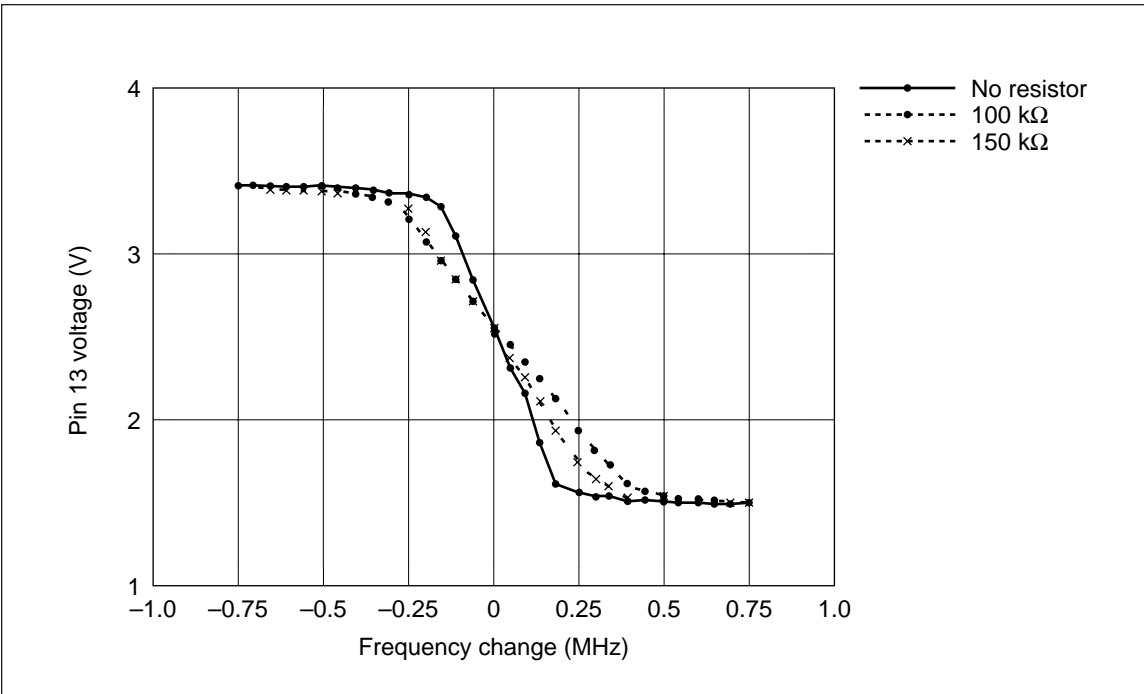


over 3.0 kΩ should be used.

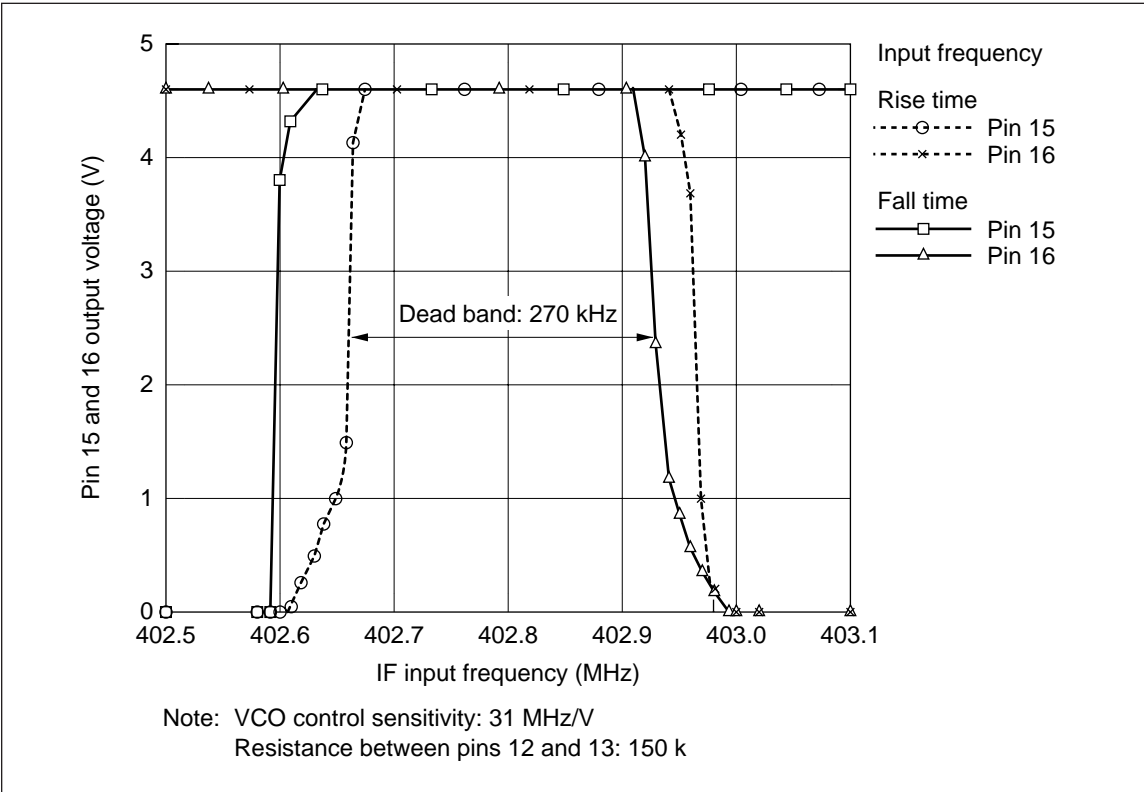


**Video Amplifier:** The video amplifier outputs the video output signal. This amplifier uses a feedback structure that allows the video output amplitude and frequency characteristics to be adjusted.

The video output will have an amplitude of



V<sub>p-p</sub> under the following conditions.  
 VCO control sensitivity: 31 MHz/V



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Resistance between pins 3 and 5: 560  $\Omega$

Input signal frequency variation: 17 MHz

The output amplitude can be adjusted by changing the value of the resistor (VR2) between pins 3 and 5. (See



FP-28T

figure 7.)

The video amplifier frequency characteristics can be adjusted by changing the value of the external capacitor (C1) connected between pins 3 and 5. The video output frequency characteristics are determined by the video amplifier frequency characteristics and the overall characteristics of the loop amplifier.

The signal to noise ratio characteristics may be degraded if a capacitive load is connected to pin 5. This problem can be ameliorated by connected a series resistance (R4) of between 50  $\Omega$  and 100  $\Omega$  to pin 5. The IC internal drive current for the video output (pin 5) is 3 mA. A video output buffer circuit should be added if the load capacitance is over 30 pF or if a larger drive current is needed.

**VCO Circuit:** This IC uses a horizontal VCO. The external resonator circuit is constructed as a parallel resonator type.

- VCO external circuit constant examples

Figure 3 shows three VCO external circuit examples, and table 1 lists examples of component values for Japanese domestic reception and European reception specifications.