SIEMENS

ICs for Communications

ATM Switching Matrix

PXB 4310 Version 1.1

Preliminary Data Sheet 12.97

DS 2

PXB 4310		
Revision History:	**Current Version: 12.97**	Functional Update
Previous Version:	Preliminary Data Sheet 08.95 (V 1.1)	
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
23	30	VBIAS has no built-in bandgap reference
91	97	Note 17 changed to comment, new note 17 added
52-55	59-62	Register ISR some descriptions changed
57	66	Note to ILA register added Bit LSE added, description of LSYNC refined
57	66	Additional bit in LFR register
58-63	67-73	All register addresses changed
58	68	Bit RXof COR inverted
62	72	Register PQLR added
63	74	Bit IVINP added to MR register
47-50	53-56	Section about cell sequence simplified

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1 Introduction

The second generation of the Siemens ATM layer chip set consists of the six chips

- PXB 4310 ATM Switching Matrix ASM
- PXB 4325 ATM Switching Preprocessor ASP
- PXB 4330 ATM Buffer Manager ABM
- PXB 4340 ATM OAM Processor AOP
- PXB 4350 ATM Layer Processor ALP.
- PXB 4360 Content Addressable Memory Element CAME

These chips form a complete chip set to build an ATM switch. A generic ATM switch consists of a switching fabric and switch ports as shown in **Figure 1**.

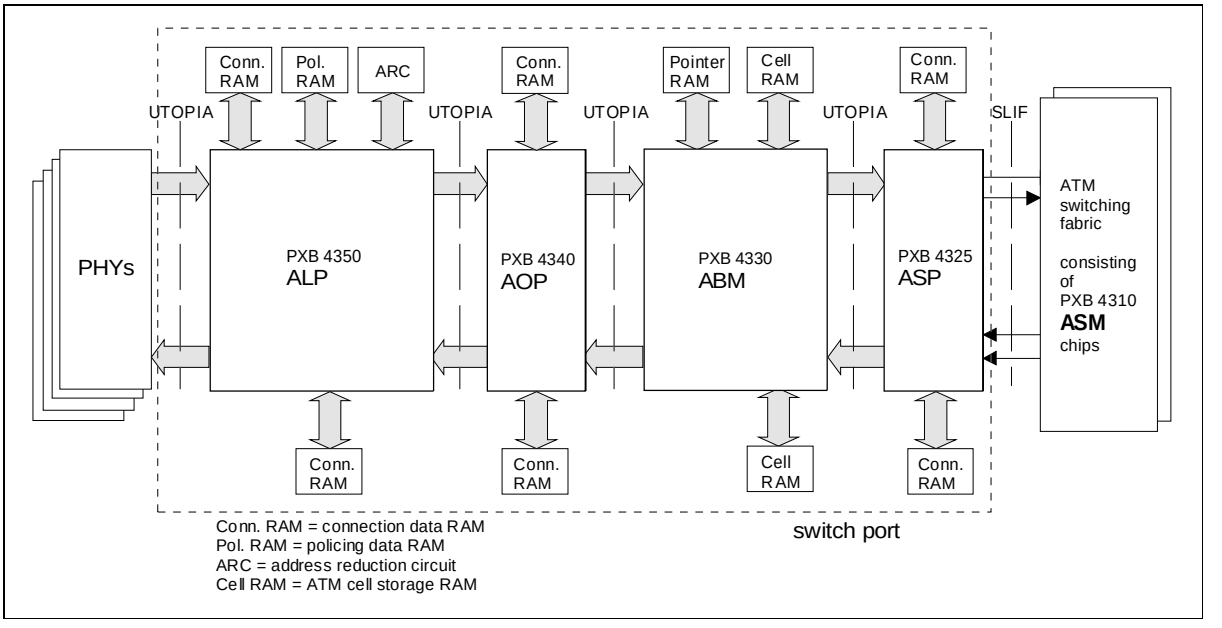


Figure 1 ATM Switch Basic Configuration

In the Siemens ATM layer chip set the switching fabric only does cell routing using the PXB 4310 ASM, which can be used stand alone or in arrays to scale switching network throughput from 2.5 Gbit/s up to more than 40 Gbit/s. All other ATM layer functions are performed on the switch ports: policing, header translation and cell counting by the PXB 4350 ALP and the PXB 4360 CAME, OAM functions by the PXB 4340 AOP and traffic management by the PXB 4330 ABM. The PXB 4325 ASP is the access device to the switching fabric and adds/removes the routing header. It also supports redundant switching fabrics and does multicast.

Only two interfaces are used for data transfer: the industry standard UTOPIA [1, 2] Level 2 multi-PHY interfaces and the proprietary Switch Link InterFace SLIF. This is a serial, differential high speed link using LVDS [3] levels.

For low end applications a single board switch with 622 Mbit/s throughput can be built with only one PXB 4350 ALP and one PXB 4330 ABM. Such a mini-switch is basically one switch port stand alone, without switching network access via the PXB 4325 ASP. If the full OAM functionality is not needed the PXB 4340 AOP chip can be omitted as shown in **Figure 2**. Minimum OAM and multicast functionality is also built into the PXB 4350 ALP. The external Address Reduction Circuit (CAME) is not required if the built-in address reduction is used.

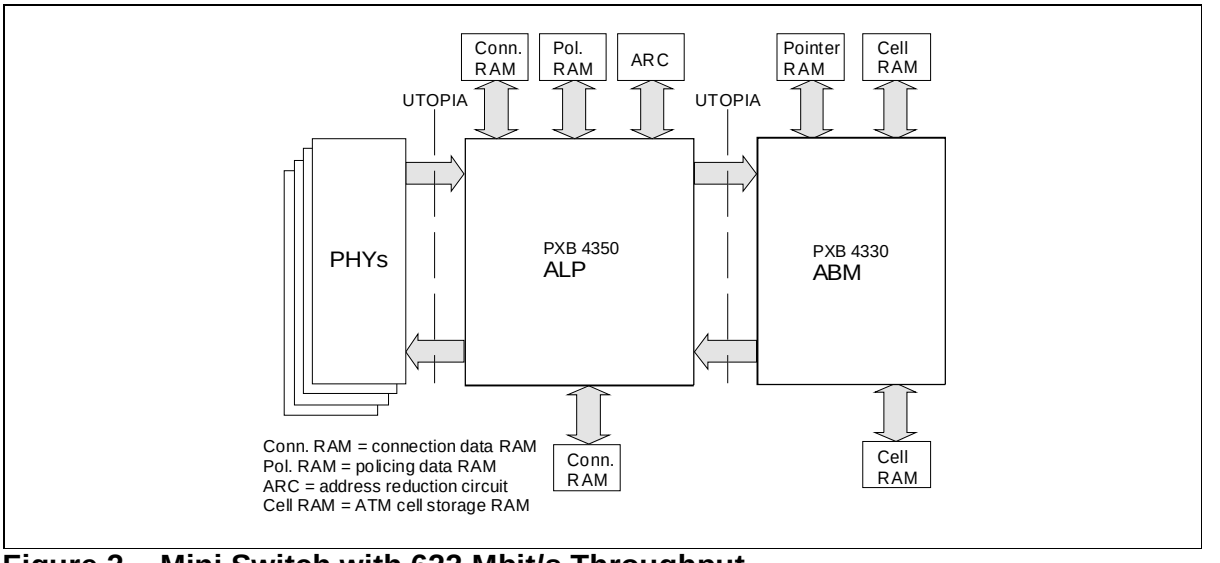


Figure 2 Mini Switch with 622 Mbit/s Throughput

Apart from the two applications of **Figure 1** and **2**, many other combinations of the chip set are possible in designing ATM switches. Functionality is selectable in many combinations due to the modular function split of the chip set. Address reduction, multicast, policing, redundant switching network and other functions can be implemented by appropriate chip combinations. The number of supported connections scales with the size of the external connection RAMs. The policing data RAM can be omitted if this function is not required.Thus functionality and size of an ATM switch can be tailored exactly to what the respective application requires, without carrying the overhead of unnecessary functions.

2 Overview

The ATM Switching Matrix is a member of the Siemens ATM integrated Chip Set. It is a true ATM cell switch with 32 inputs and 16 outputs each of which can transport a STM-1 equivalent load. Total maximum throughput is 2.5 Gbit/s. A shared buffer architecture with individual output queues allows ATM cell loads of 95 % of a STM-1 payload for each output. An adjustable buffer limit is provided to account for low priority cells.

The ASM supports both self-routing (with the output port address contained in the cell header) and multicast (using an external look-up table). The chip can be used stand-alone or in a networked configuration. It can be configured in various operating modes.

Multiple ASMs can be connected to build switching networks of arbitrary size. A continuous growth from small to very large switching networks is possible.

Inputs and outputs are realized as serial, differential transmission lines, defined as Switch Link Interface (SLIF). The serial interface allows a lower pin count and less power dissipation compared to chips with parallel I/Os. Both features result in a smaller and cheaper chip. The low pin count is an important feature if larger switching networks are built which extend over multiple boards via backplane. No clock line is necessary to transmit data, as each input of the ASM has an individual bit phase adaptation.

The ASM has the capability of bundling 2, 4, 8 or 16 lines to form pipes of higher bit rates up to 2.5 Gbit/s. In these cases the transmitting ASM distributes the cells cyclically on the lines of the bundle, so that the receiving ASM can reconstruct the correct sequence. This feature facilitates the bandwidth management for the interconnection lines of a switching network and allows the later support of 622 Mbit/s and 2.5 Gbit/s line interfaces.

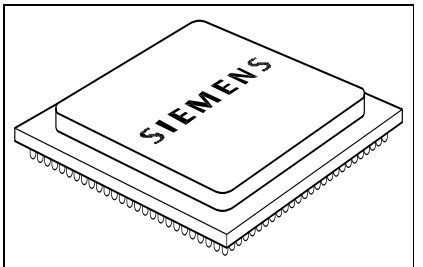
Electrical characteristics of the SLIF are according to the LVDS standard defined by IEEE **[7]**. The LVDS signals have low voltage swing and use 50 Ω terminated transmission lines. The low impedance and the differential signal guarantee a secure data transmission, even via connectors, backplanes and twisted or coaxial cable pairs of up to some meters length. This simplifies the construction of large switching networks.

The data format is the Siemens proprietary 64 byte ATM cell which contains the standardized 53 byte ATM cell extended by routing and housekeeping informations.

The conversion from standardized 53 byte cell format to SLIF format is done by the PXB 4325 ATM Switching Preprocessor ASP which connects to one, two or four lines of the switching network. The ASP frees the user to cope with the data format inside the switch; simply writing the desired output port of the switch into the upstream translation RAM of the ASP defines the path through the network. The ASP does all the necessary conversions in both directions, i.e. at the switch input port and at the switch output port. It has a bidirectional throughput of one, two or four STM-1 equivalents.

The ASM is controlled via a generic 8-bit microprocessor interface with 8-bit address bus.

2.1 Features



P-BGA-352

- Self-routing switching matrix with built-in multicast function and redundant switching architecture support.
- High performance: 10^{-10} cell loss probability with 87 % Bernoulli type traffic (corresponds to 96 % load on a STM-1/OC-3 link).
- Internal speed-up concept reduces cell load inside the switching network.
- Central buffer architecture provides minimum cell delay variation at high data throughput.
- Routing Header provides 32-bit routing address, freely configurable.
- Expandable up to 256 $\times$ 256 non-blocking switching network core.
- Blocking switching networks up to 32768 $\times$ 32768 ports.
- Free programmable input filter function.
- Configurable as single chip multiplexer/demultiplexer.
- Prepared for 622-Mbit/s and 2.5-Gbit/s ports.
- Uses 200-Mbit/s serial, differential data link lines, the Switch Link Interface.
- Switch Link Interface uses LVDS levels for low crosstalk, less interference and low power consumption.
- Individual phase adaptation per input; no separate clock required.
- Static output multiplexer allows flexible assignment of output queues to outputs e.g. for protection switching support.
- Intel compatible 8-bit microprocessor interface for chip control.
- 3.3-V 0.5-µ-CMOS technology.
- Power dissipation below 3 W.
- 352-pin ball-grid array.

Type	Ordering Code	Package
PXB 4310	Q67101-H6587	P-BGA-352

2.2 Logic Symbol

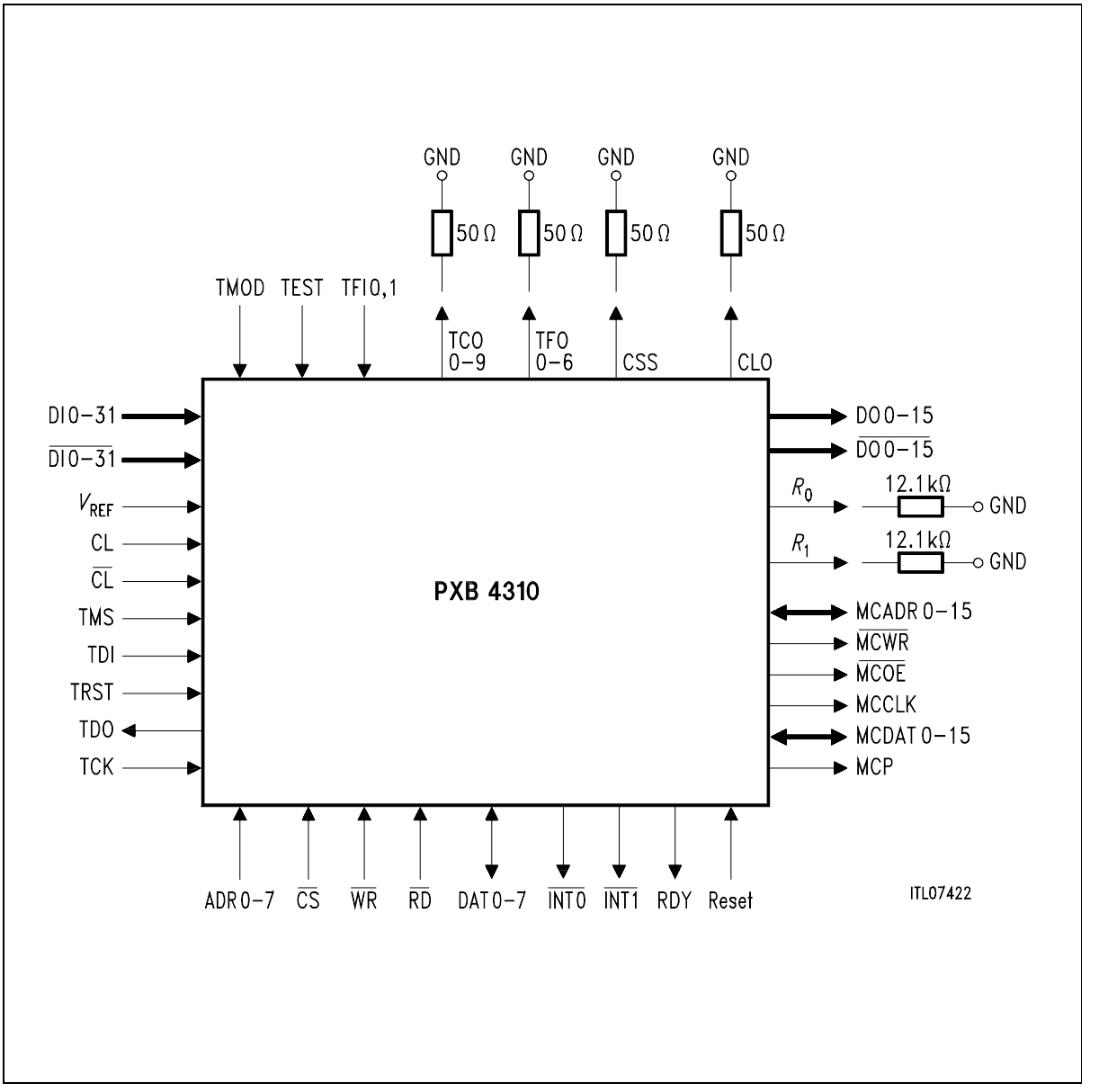


Figure 3 ASM Logic Symbol

2.3 Pin Configuration

(bottom view)

A1	B1	C1	D1	E1	F1	G1	H1	J1	K1	L1	M1	N1	P1	R1	T1	U1	V1	W1	Y1	AA1	AB1	AC1	AD1	AE1	AF1
A2	B2	C2	D2	E2	F2	G2	H2	J2	K2	L2	M2	N2	P2	R2	T2	U2	V2	W2	Y2	AA2	AB2	AC2	AD2	AE2	AF2
A3	B3	C3	D3	E3	F3	G3	H3	J3	K3	L3	M3	N3	P3	R3	T3	U3	V3	W3	Y3	AA3	AB3	AC3	AD3	AE3	AF3
A4	B4	C4	D4	E4	F4	G4	H4	J4	K4	L4	M4	N4	P4	R4	T4	U4	V4	W4	Y4	AA4	AB4	AC4	AD4	AE4	AF4
A5	B5	C5	D5																			AC5	AD5	AE5	AF5
A6	B6	C6	D6																			AC6	AD6	AE6	AF6
A7	B7	C7	D7																			AC7	AD7	AE7	AF7
A8	B8	C8	D8																			AC8	AD8	AE8	AF8
A9	B9	C9	D9																			AC9	AD9	AE9	AF9
A10	B10	C10	D10																			AC10	AD10	AE10	AF10
A11	B11	C11	D11																			AC11	AD11	AE11	AF11
A12	B12	C12	D12																			AC12	AD12	AE12	AF12
A13	B13	C13	D13																			AC13	AD13	AE13	AF13
A14	B14	C14	D14																			AC14	AD14	AE14	AF14
A15	B15	C15	D15																			AC15	AD15	AE15	AF15
A16	B16	C16	D16																			AC16	AD16	AE16	AF16
A17	B17	C17	D17																			AC17	AD17	AE17	AF17
A18	B18	C18	D18																			AC18	AD18	AE18	AF18
A19	B19	C19	D19																			AC19	AD19	AE19	AF19
A20	B20	C20	D20																			AC20	AD20	AE20	AF20
A21	B21	C21	D21																			AC21	AD21	AE21	AF21
A22	B22	C22	D22																			AC22	AD22	AE22	AF22
A23	B23	C23	D23	E23	F23	G23	H23	J23	K23	L23	M23	N23	P23	R23	T23	U23	V23	W23	Y23	AA23	AB23	AC23	AD23	AE23	AF23
A24	B24	C24	D24	E24	F24	G24	H24	J24	K24	L24	M24	N24	P24	R24	T24	U24	V24	W24	Y24	AA24	AB24	AC24	AD24	AE24	AF24
A25	B25	C25	D25	E25	F25	G25	H25	J25	K25	L25	M25	N25	P25	R25	T25	U25	V25	W25	Y25	AA25	AB25	AC25	AD25	AE25	AF25
A26	B26	C26	D26	E26	F26	G26	H26	J26	K26	L26	M26	N26	P26	R26	T26	U26	V26	W26	Y26	AA26	AB26	AC26	AD26	AE26	AF26

Figure 4 Ball Configuration - The Index Mark is at Ball A1

2.4 Pin Definitions and Functions

Pin No.	Symbol	Function
Inputs		
AD15, AC15	DI0, $\overline{DI0}$	Differential data inputs.
AE15, AE14	DI1, $\overline{DI1}$	Data rate up to 208 Mbit/s.
AC14, AD14	DI2, $\overline{DI2}$	
AD13, AC13	DI3, $\overline{DI3}$	
AC12, AD12	DI4, $\overline{DI4}$	
AD11, AC11	DI5, $\overline{DI5}$	
AE11, AE10	DI6, $\overline{DI6}$	
AC10, AD10	DI7, $\overline{DI7}$	
AD9, AC9	DI8, $\overline{DI8}$	
AC8, AD8	DI9, $\overline{DI9}$	
AD7, AC7	DI10, $\overline{DI10}$	
AE7, AE6	DI11, $\overline{DI11}$	
AC6, AD6	DI12, $\overline{DI12}$	
AD5, AC5	DI13, $\overline{DI13}$	
AC3, AC4	DI14, $\overline{DI14}$	
AC2, AB2	DI15, $\overline{DI15}$	
AB4, AB3	DI16, $\overline{DI16}$	
AA3, AA4	DI17, $\overline{DI17}$	
Y4, Y3	DI18, $\overline{DI18}$	
W3, W4	DI19, $\overline{DI19}$	
W2, V2	DI20, $\overline{DI20}$	
V4, V3	DI21, $\overline{DI21}$	
U3, U4	DI22, $\overline{DI22}$	
T4, T3	DI23, $\overline{DI23}$	
R3, R4	DI24, $\overline{DI24}$	
R2, P2	DI25, $\overline{DI25}$	
P4, P3	DI26, $\overline{DI26}$	

Pin No.	Symbol	Function
N3, N4	DI27, $\overline{DI27}$	
M4, M3	DI28, $\overline{DI28}$	
L3, L4	DI29, $\overline{DI29}$	
L2, K2	DI30, $\overline{DI30}$	
K4, K3	DI31, $\overline{DI31}$	
G3	VREF	Analog reference voltage input, used for a precise adjustment of the internal current sources. VREF-value: (1.2 ± 0.1)V
C22, D22, B22, D23, D25, E25, E23, E24	ADR0 … 7	Address bus of the µP-interface.
K23	$\overline{CS}$	Chip select signal of the µP-interface (low active).
L23	$\overline{WR}$	Write enable signal of the µP-interface (low active).
L26	$\overline{RD}$	Read enable signal of the µP-interface (low active).
F2	$\overline{RESET}$	Hardware reset, blocks all cell output data (DO) while ‘0’; starts internal reset procedure with the low to high level transition.
D20	TMS	Boundary Scan Test Mode Select.
B20	TDI	Boundary Scan Test Data Input.
B21	TRST	Boundary Scan Test Reset.
G2	TMOD	Device test mode status signal, controls the chip-internal generation of the phase-alignment clocks. During normal operation, TMOD must be kept at ‘0’ in normal operation.
AC21	TEST	Test mode signal, for device test only. Must be kept at ‘1’ in normal operation.

Outputs

D19, C19	DO0, $\overline{DO0}$	Differential data outputs. The outputs operate into a 50 Ω line terminated by a 50 Ω resistor.
C18, D18	DO1, $\overline{DO1}$	
D17, C17	DO2, $\overline{DO2}$	
C16, D16	DO3, $\overline{DO3}$	
D15, C15	DO4, $\overline{DO4}$	

Pin No.	Symbol	Function
C14, D14	DO5, $\overline{DO5}$	
D13, C13	DO6, $\overline{DO6}$	
C12, D12	DO7, $\overline{DO7}$	
D11, C11	DO8, $\overline{DO8}$	
C10, D10	DO9, $\overline{DO9}$	
D9, C9	DO10, $\overline{DO10}$	
C8, D8	DO11, $\overline{DO11}$	
D7, C7	DO12, $\overline{DO12}$	
C6, D6	DO13, $\overline{DO13}$	
D5, C5	DO14, $\overline{DO14}$	
C4, D4	DO15, $\overline{DO15}$	
G4	R0	Calibration output, used for an external resistor between R0 pin and ground. Resistor value 12.1 k$\Omega \pm 1$ %.
C20	R1	Calibration output, used for an external resistor between R1 pin and ground. Resistor value 12.1 k$\Omega \pm 1$ %.
J23	$\overline{INT0}$	Interrupt 0 of the µP-interface, open drain output (low active).
J24	$\overline{INT1}$	Interrupt 1 of the µP-interface, open drain output (low active).
K24	RDY	Ready signal of the µP-interface, open drain output (high active).
W24, Y24, Y23, Y25, AA25, AA23, AA24, AB24, AB25, AD23, AC23, AE23, AE22, AC22, AD22, AD21	MCADR0 … 15	Address bus for Multicast RAM.
L24	$\overline{MCWR}$	Write signal for Multicast RAM (low active).
M24	$\overline{MCOE}$	Output enable signal for Multicast RAM (low active).
C21	TDO	Boundary Scan Test Data Output.

Pin No.	Symbol	Function
AE21, AE20, AC20, AD20, AD19, AC19, AE19, AE18, AC18, AD18	TCO0 … 9	Test control outputs, for device test purpose only.
AD17, AC17, AE17, AC16, E3, E4, E2	TFO0 … 6	Analog test outputs, for device test only. Must be left open.
F4	CSS	Analog device test output, source follower; indicates the cell starts, i.e. the 1st octet of the cells clocked out at the data output DO0. Must be terminated with 50 Ω when used, otherwise open.

Bidirectional Pins

F24, F23, G25, G23, G24, H24, H23, J25	DAT0 … 7	Data bus of the µP-interface.
N25, N23, N24, P24, P23, R25, R23, R24, T24, T23, U25, U23, U24, V24, V23, W25	MCDAT0 … 15	Data bus for the Multicast RAM.
W23	MCP	Parity bit for the Multicast RAM.

Clock Inputs and Outputs

J2	CL	I	Operating clock input with a frequency of up to 208 MHz.
H2	$\overline{CL}$	I	Complementary clock input.
D21	TCK	I	Boundary Scan Test Clock Input.

Pin No.	Symbol		Function
M23	MCCLK	O	Clock output for Multicast RAM, frequency is 1/8 of the operating clock.
F3	CLO	O	Analog device test clock output, source follower, operates at a frequency of up to 208 MHz; the positive edge clocks the output data and can be used to strobe them. Must be terminated with 50 Ω.

Pin No.	Symbol
Power Supply	
A1, B1, E1, F1, J1, K1, N1, P1, U1, V1, AA1, AB1, AE1, AF1, A2, C2, N2, U2, AA2, AD2, AF2, B3, D3, H3, J3, AE3, B4, AD4, A5, AF5, A6, B6, AF6, B8, AE8, A9, AF9, A10, B10, AF10, B12, AE12, A13, AF13, A14, B14, AF14, B16, AE16, A17, AF17, A18, B18, AF18, A21, AF21, A22, AF22, C23, B24, AC24, AE24, A25, C25, AD25, AF25, A26, B26, E26, F26, J26, K26, N26, P26, U26, V26, AA26, AB26, AE26, AF26	V_{CC}
C1, D1, G1, H1, L1, M1, R1, T1, W1, Y1, AC1, AD1, B2, D2, M2, T2, Y2, AE2, A3, C3, AD3, AF3, A4, H4, J4, AE4, AF4, B5, AE5, A7, B7, AF7, A8, AF8, B9, AE9, A11, B11, AF11, A12, AF12, B13, AE13, A15, B15, AF15, A16, AD16, AF16, B17, A19, B19, AF19, A20, AF20, A23, B23, AB23, AF23, A24, C24, AD24, AF24, B25, AC25, AE25, C26, D26, G26, H26, L26, M26, R26, T26, W26, Y26, AC26, AD26	GND
D24, F25, H25, K25, M25, P25, T25, V25	not connected

2.5 Functional Block Diagram

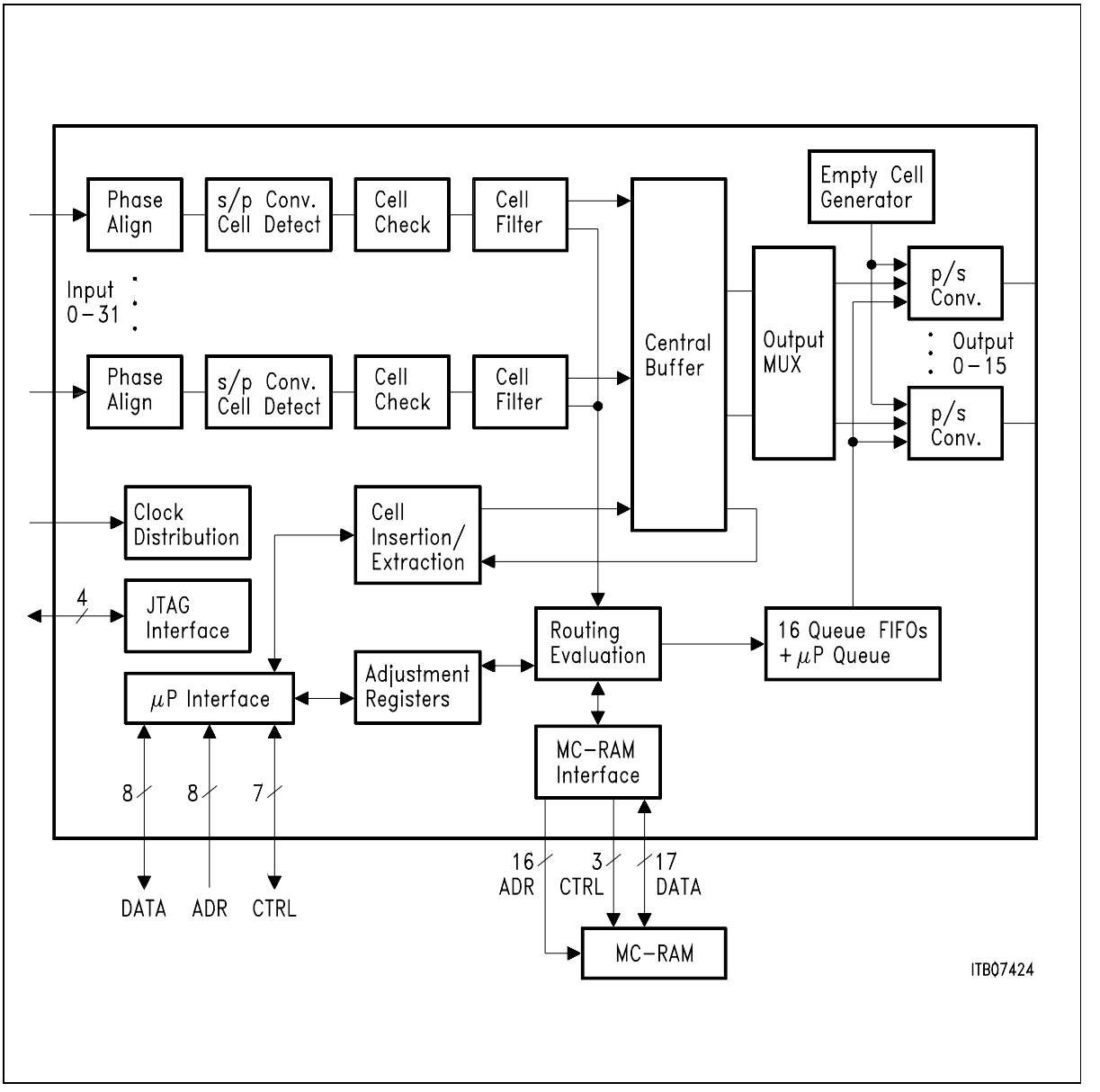


Figure 5 Block Diagram of ASM

2.6 System Integration

The ASM needs the PXB 4325 ATM Switching Preprocessor ASP as access device. A generic circuit is shown in **Figure 6**. It shows the path of ATM cells through a switch. ATM cells with standardized 53-octet cell format are input at the UTOPIA receive interface of the ASP which expands the cells to 64-octet format by adding routing and housekeeping octets. The cells are output at the serial SLIF interface which is connected to the ATM switching network ASN. The ASN may be of arbitrary size, consisting from one stand-alone ASM up to an array of many ASM chips. In any case the routing header of the cells defines a unique path through the ASN to the desired output port, which is connected to an ASP. This chip does the necessary post-processing and reduces the cell to standardized 53-octet format, which is output at the UTOPIA transmit interface.

The operating clock of up to 208 MHz is supplied to all ASM and ASP chips in the system. It needs not necessarily come from the same clock source, but the frequencies must be within a certain range (refer to **Section 7.2**, page 107).

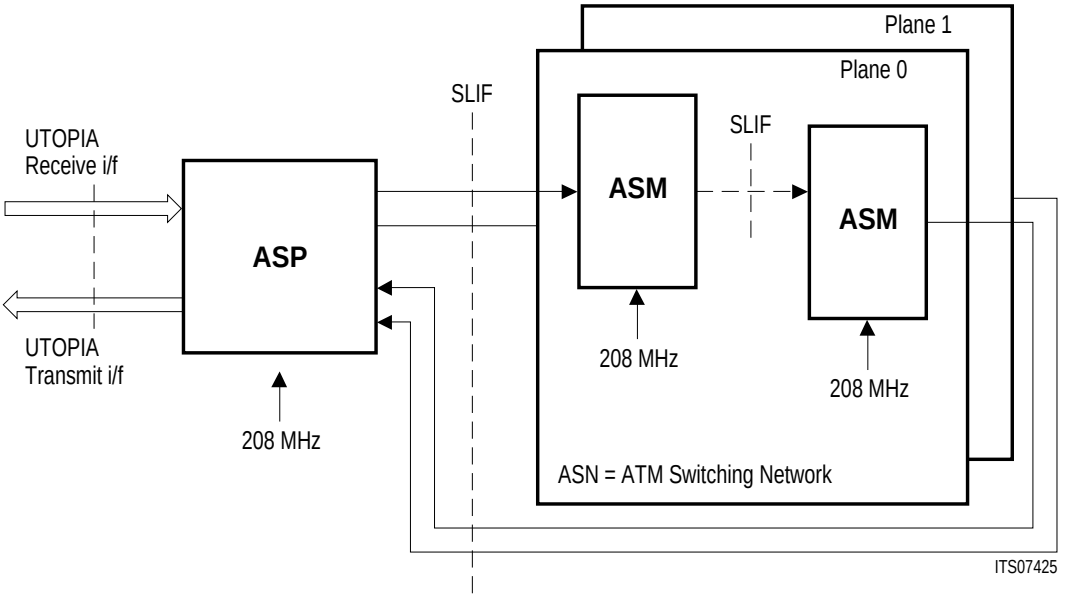


Figure 6 ATM Cell Path through a Switch

Figure 6 shows that the ASP chips allow the connection of two switching network planes for redundancy or load sharing purposes.

3 Functional Description

The ASM has two main functions, routing and queuing.

Routing is the true switching function of forwarding ATM cells from any input to a desired output. The routing information is contained in the header of the ATM cells. The ASM evaluates the routing header information with respect to its configuration.

Queuing occurs due to the asynchronous nature of ATM. For a short time more cells may arrive at the ASM inputs than can be forwarded by the outputs and thus accumulate in the internal buffer. Queuing thus means for the ASM to store cells and queue them to the respective output(s) by preserving the cell sequence from the inputs.

3.1 Routing

The ASM is capable to route ATM cells received at any input to one or more desired outputs. It can switch two types of cells, point-to-point and point-to-multipoint (=multicast) cells. For point-to-point cells the self routing principle is used, i.e. the cell carries the information of the desired output directly in its own routing header.

Figure 7 shows the self routing principle. In this example the cell comes in at input line 6 of a switching element. It has a prepended routing header carrying the pattern $101_{bin} = 5_{dec}$. and a bit identifying the cell as self-routing cell. The switching element uses the pattern as encoded output number and programs the output multiplexer accordingly. The cell is thus forwarded to output 5.

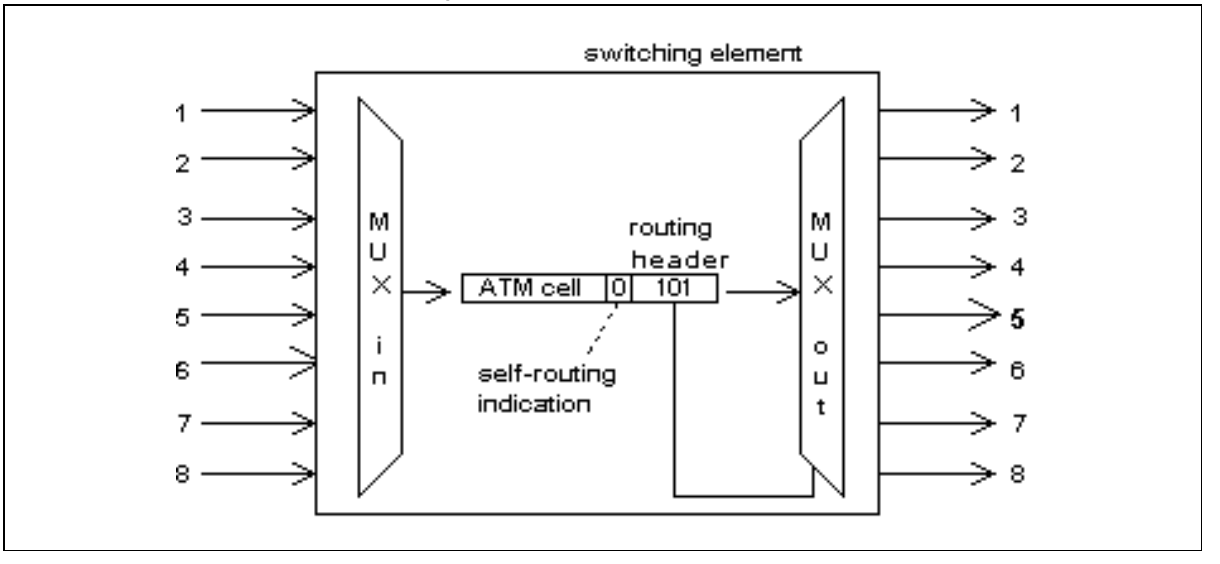


Figure 7 Self-routing Principle for Point-to-Point Connections

For multicast cells the table routing method is used, where a part of the cell header is used as address to a routing table. Each entry of this table defines the outputs of the (multicast) connection.

Figure 8 shows the table routing principle. The cell comes in at input line 6 of a switching element. The prepended routing header has the same pattern as in the self-routing

example with the exception that the cell is identified as table routing cell. The switching element in this case uses the pattern 101_{bin} as address to a table where the output(s) of the switching element are represented by a 8-bit pattern. A „one“ means that the cells of this connection are to be forwarded to the corresponding output. In the example of **Figure 8** bit the bit positions 2 and 3 are denoted at the table location 5 and hence the cell is output at outputs 2 and 3.

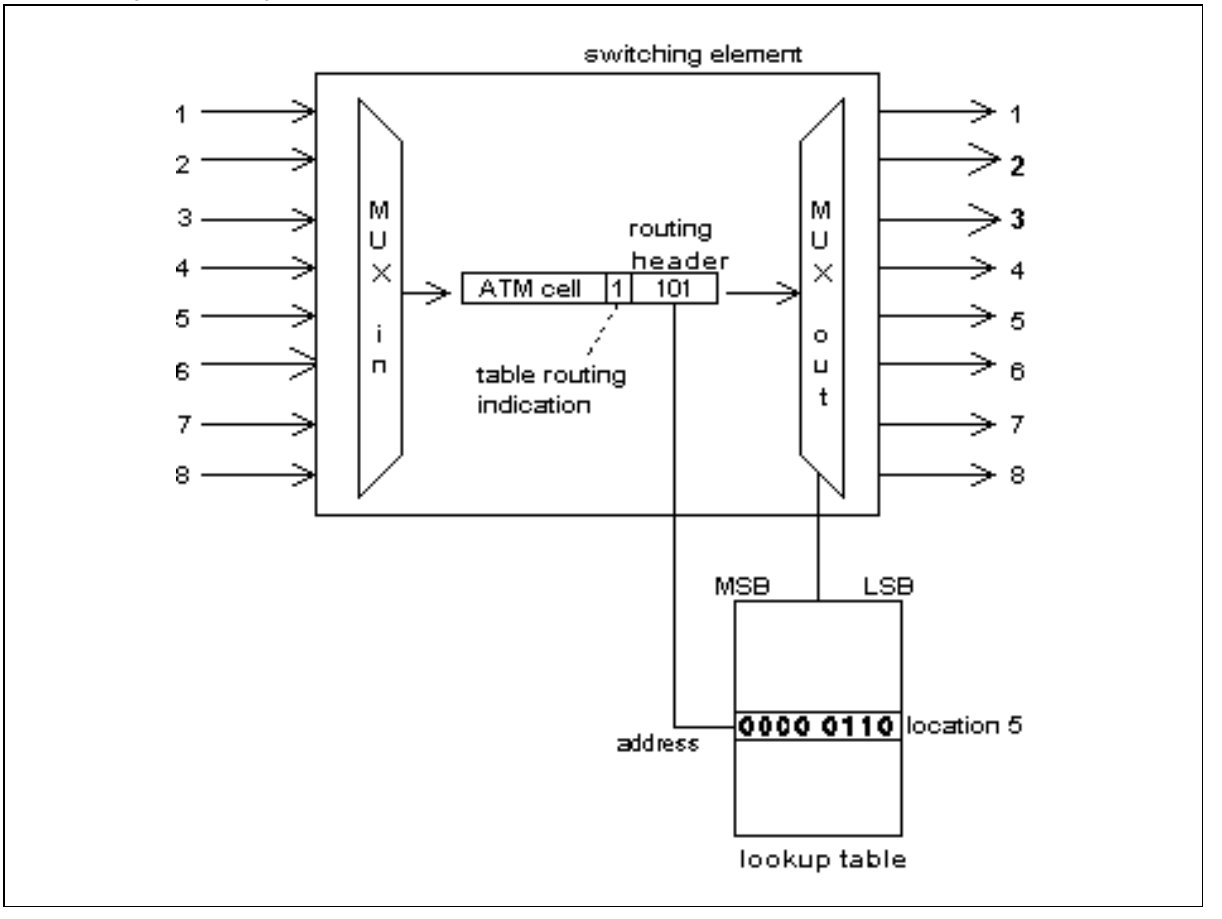


Figure 8 Table Routing Principle for Multicast Connections

Note that table routing could be used for point-to-point and point-to-multipoint connections. However, it is recommended to use table routing only for multicast connections, as self-routing does not require to handle table entries.

The lookup table for multicast is realized in the ASM as external RAM (MC-RAM). The size of the table determines the total number of multicast connections in the switch. A maximum of 65536 multicast connections are supported by the ASM, limited by the address bus width of the MC-RAM interface. If less multicast connections are needed in a switch a smaller MC-RAM can be connected. It can be omitted if the multicast functionality is not required at all.

Self routing

For self routing up to four bit are required to determine the output of an ASM. The four bits must be contiguous. Their location within the 32-bit routing tag is programmable. This offers maximum flexibility in the design of switching networks.

If a switching network consists of several stages as shown e.g. in **Figure 25**, the ASM chips of each stage are programmed to 'look' at a different four bit group. A three stage switching network would require three groups of four routing bits. If outputs are bundled (see below) less than four bits are needed for routing.

Each of the switching elements shown in **Figure 25** could be built with two ASMs connected in parallel. To support such a configuration the ASM has the input filter function.

Input filtering

The input filter function allows to connect the inputs of multiple ASMs in parallel. This allows to build switching networks as shown e.g. in **Figure 22**, where the right hand ASM filters out (accepts) only the cells destined to outputs 0..15 and the left hand ASM accepts only the cells for outputs 16..31.

The filter function also uses the 32-bit routing tag. The 32-bit filter mask register defines an arbitrary part of the routing tag as filter field as shown in the example of **Figure 9**. The content of this field of each cell is compared to the respective part of the 32-bit identification register. The cell is only accepted if the two pattern match. Masked bits always match, so that when all bits are masked the cell is accepted anyway.

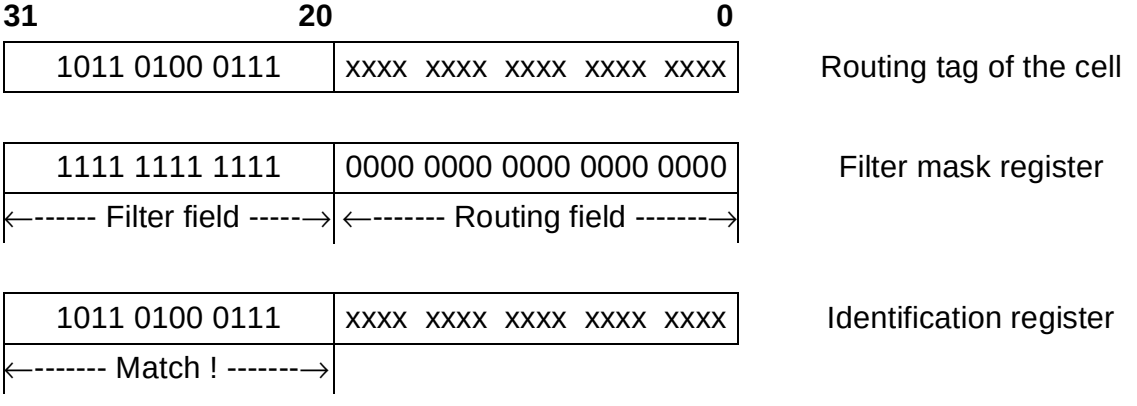


Figure 9 Definition of Filter Field and Routing Field

In the example of **Figure 9** the filter field of the cell matches the content of the identification register and the cell is accepted.

Separation of filter field and routing field is completely arbitrary. Both may even be non-contiguous and spread over the whole 32-bit range. This arbitrary definition

possibility gives maximum flexibility for the design of switching networks. There are, however, some restrictions which should be taken into account:

- Routing and filter fields should not overlap.
- In split mode the 6 LSBs of the routing tag are reserved (see below).
- It may be useful to restrict the multicast function to some of the ASMs in a switching network (see **Figure 32**).This avoids the MC-RAM at some of the ASMs. These ASMs may be programmed to ignore multicast cells and treat them as self routing cells. The filter and routing fields interpreted by these ASMs must use the part of the routing tag which is **not** used as multicast address (AUX-bits of **Figure 19**).

Special routing functions

- Depending on the configuration of the output multiplexer (see **Figure 10**) the physical output can be different to the specified output number. It may also be configured that the same cell is forwarded to several outputs, a function which is independent of the multicast function.
- If SLIF bundles are declared (see below) the cell is output at any output within the bundle. If e.g. the 4 routing bits specify output 2, and a 4-bundle is declared for outputs 0 … 3, the cell may be output at any output of this bundle, but not necessarily at output 2.
- For the special case that all outputs form one 16-bundle the output number is meaningless. If additionally the filter function is switched off (by masking all 32 routing bits) the ASM works as a simple multiplexer. This mode is used in the middle stage of **Figure 24**.

Split Mode

This is an additional feature to the self-routing mode. Normally the cells from all inputs are treated identically. In split mode, the 32 inputs can be split into two groups with the cells input at different groups routed according to different routing bits. The two input groups can be defined by programming a value n between 0 and 30 to the mode register of the ASM. The respective routing is as follows:

- inputs 0..(n-1), lower part: fixed routing according to the 4 LSBs of the routing tag (bits 0..3) with a small, fixed, 2-bit filter field (bits 4 and 5). Unlike the normal filter function this filter field is not maskable.
- inputs n..31, higher part: normal routing tag evaluation with filter option as described above.

Split mode is used for single chip multiplexers with concentrating upstream traffic and distributing downstream traffic (see e.g. **Figure 28**).

Communication and test cell routing

The ASM has the capability to insert cells from the microprocessor interface into the cell stream and to extract cells from the cell stream and direct them to the microprocessor interface. There are two applications for these features, system test and internal communication.

System tests can be done in-service e.g. to check the availability of all interconnection lines between the ASMs of a switching network and between ASM and ASP devices. For this purpose test cells can be inserted at specified outputs, even in bundle mode. It also is not influenced by the setting of the output multiplexer, but uses always the default path.

Communication cells could be used in large switches, where the switching network consists of several boards. A dedicated µP could be used to control the ASM chips e.g. on a switch board. A communication channel to this µP can be set-up via the data lines to the system controller. One ASM will be selected to drop the communication cells.

To support this feature the ASM provides two transmit buffers of one cell size and a receive buffer queue. To detect incoming test or communication cells the switching stage number (SSN) field of the prepended routing header is used. A cell is extracted if the SSN is non-zero and matches the SSN assigned to the respective ASM chip.

Some features of this function are:

- The filter function is applied normally before comparing the SSN.
- The non-zero SSN field overrides the multicast indication bit of the cell, i.e. these cells are never treated as multicast cells.
- The acceptance of all other cells than communication or test cells can be disabled. This is especially useful during the initialization phase of a chip.

3.2 Queuing

Queuing occurs due to the asynchronous nature of ATM. As the arrival of ATM cells of a given connection is not in a fixed time slot, it may happen that simultaneously two or more cells destined to the same output may arrive at the inputs. As the output can forward only one cell at a time, the other cell(s) have to be stored intermediately. If at a later time no cells are destined to this output the ASM can work off the stored cells and empty the buffer. The maximum number of cells which has to be stored for a given output load can be derived using statistical methods (see appendix).

Throughput

The ASM is able to switch ATM cells with a data rate of up to 208 Mbit/s from up to 32 high speed inputs ports to 16 high speed output ports. 208 Mbit/s is the data rate of one SLIF line. As the SLIF cell format is 64 octet, the effective data rate with reference to standard, 53-octet ATM cells is 208 Mbit/s x 53/64 = 172.25 Mbit/s.

Its total effective throughput is thus 16 x 172.25 Mbit/s = 2.756 Gbit/s.

Fairness Management

The fairness management determines the maximum number of queue entries for each output queue. It is recommended to specify a maximum queue length if more than one output queue are configured. Otherwise one output queue - e.g. in an overload situation - could occupy the whole buffer, so that all cells destined to any other output are discarded.

The maximum queue sizes for a given load and for a cell loss probability of 10^{-11} can be obtained from **Figure 40**. If as an example the ASM operates with a load of 90 % the required total buffer size is 270 cells. The buffer limit for the single queue can be obtained from the curve 'X|1-Multiplexer', which amounts to 128 cells approximately.

For bundles of 4 or 8 the maximum queue size is obtained from the curves 'X|4-Multiplexer' and 'X|8-Multiplexer', respectively. For the above example the values are 160 and 202, respectively. For bundles of 2 the value can be extrapolated from curves 'X|1-Multiplexer' and 'X|4-Multiplexer'.

For each sort of bundle group (also for single ports) the maximum number of queue entries can be specified by a threshold defined via the µP-interface.

Output Grouping

The ASM is able to route ATM cells to a specified output or to a bundle of outputs. The bundle size can be 2, 4, 8, or 16.

The input and output sections of the ASM are able to handle data streams of up to 16×155 Mbit/s = 2.5 Gbit/s without violating cell sequence integrity (see **Section 4.7**).

Priority Handling

A control feature incorporated within the chip-internal logic enables the device to handle cells of two different priorities (high and low) by permanently evaluating the **c**ell **l**oss **p**riority bit CLP.

For low priority cells (CLP = 1, **Figure 18** and **19**) a threshold for the total buffer fill can be programmed. There is no individual queue limit for low priority cells.

3.3 Other Functions

Cell check

All incoming cells are checked for correct header parity. Cells with false parity bit are discarded. Empty[1)] cells defined by a special housekeeping pattern are discarded. The ASM generates new empty cells at the output ports if necessary (cell rate decoupling).

[1)] The term 'empty cell' is used to denote stuffing cells inside the switching network. These are proprietary cells and must not be mixed up with the standardized unassigned or idle cells. Empty cells never leave the switching network.

High Speed Input/Output Operation

The data inputs/outputs work with LVDS-compatible signal levels. The appropriate data rate is common for all the I/Os and amounts to 208 Mbit/s.

The LVDS-compatible system clock inputs operate with the single frequency clock of 208 MHz.

Bit Phase Alignment

In order to enable an asynchronous clock/data operation the switch is equipped with 32 internal phase-aligning circuits, each processing one of the data inputs.

Cell Start Detection

The ASM detects cell start using Sync byte with the MSB toggeling to prevent mis-synchronization to possible payload pattern. Hence the Sync byte alternates between $E8_H$ and 68_H.

Output Multiplexer

A static multiplexer located between output queues and parallel-to-serial converters allows the arbitrary assignment of each output to any output queue, i.e. each output can be programmed to get the cells from an arbitrary output queue. Several outputs can be assigned to one output queue. This means that multiple outputs get the (identical) cell stream from the same output queue.

Applications for this feature are 1:1 or n:1 redundancy schemes as shown in **Figure 10** showing two applications. Outputs 0 and 1 are both connected to the same queue 0. Hence both have the identical cell stream. This can be used to have two transmission lines with 1:1 redundancy. The other outputs are configured as a 13:1 redundant system. Outputs 2 … 14 are active, output 15 is redundant. If any of the transmission lines connected to the active outputs fails output 15 can be switched to this output to take over. In the example of **Figure 10** the transmission line of output 2 has failed.

The feature is effectively a protection of the line card or LIC and is therefore referenced in this document as ‘LIC Protection Switch LPS’.

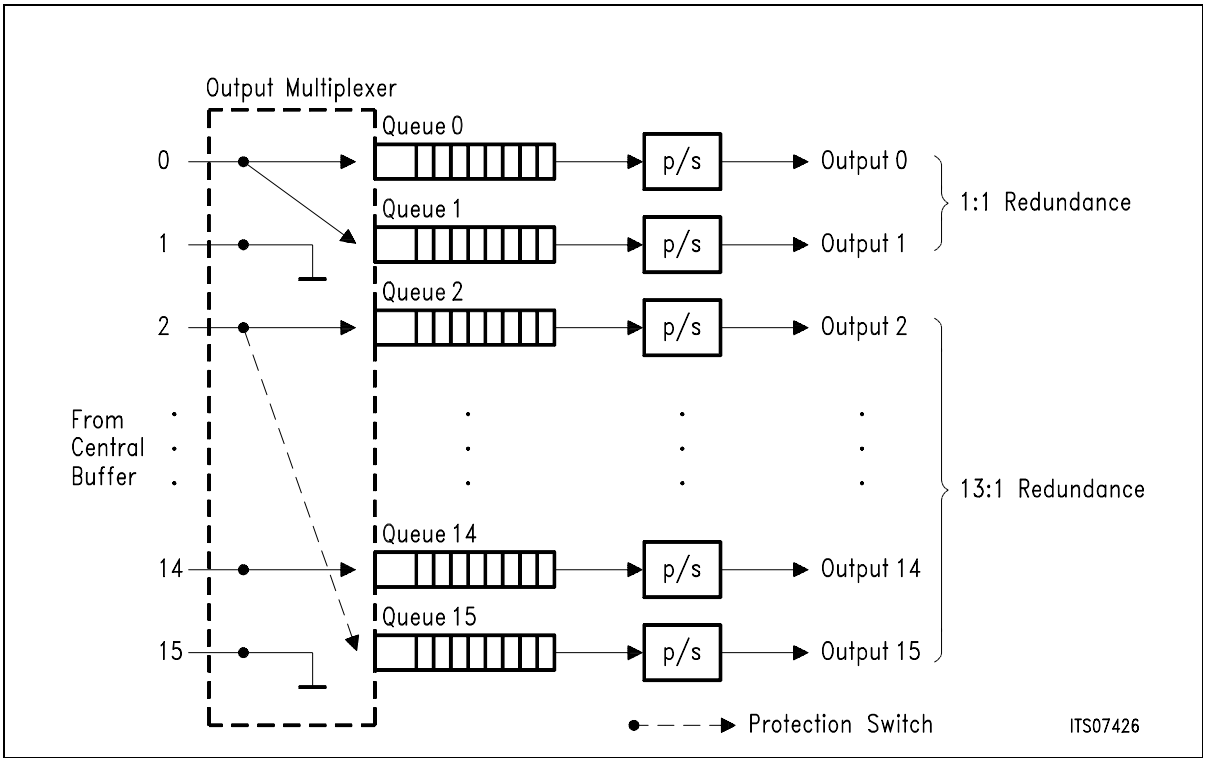


Figure 10 Applications for the Output Multiplexer

Cells which are addressed to an output queue which is not connected to any output are discarded. In the example of **Figure 10** the cells of queues 1 and 15 are discarded.

The change of queue to output assignment can be done in-service. To identify the switch-over of any output queue, the ASM inserts a Protection Switch Identifier cell (PSI-cell) between the last cell of the ‘old’ central buffer output and the first cell of the ‘new’ central buffer output. E.g. in case of the above example before the switchover queue 15 would receive no cells and thus only empty cells are produced at the output. After the queue change command the PSI-cell would be inserted at output 15 before the first cell coming from central buffer output 2.

Immediately after the switchover command for a queue this queue could contain some cells from the ‘old’ central buffer output, then a PSI-cell, and then the first cells from the ‘new’ central buffer output.

Logic Control

Control functions are implemented, to permanently supervise the HW inside and outside the chip:

– Check of synchronization state (SYNC/ASYNC state) for each input port,
– Parity check of the internal header octets used by the ASM (external parity),
– Byte-interleaved parity check made on the whole cell itself (chip internal parity),

– Check of the correct chip-internal queue handling by parity protected multicast entries, cell location data and cell entry usage count,
– Check of the actual buffer occupation (buffer overflow, queue overflow).

Test of Control Functions

The control functions can be separately tested via the µP-interface of the ASM. This can be done during normal operation, i.e. without any need for disconnecting or even removing the device, a fact that drastically relieves the supervision of the system and the localization of potential failures.

Device Test Functions

The ASM offers boundary scan for all inputs and outputs with the following restrictions:

– No self test and
– High speed input/output ports can only be monitored and not disconnected.

3.4 Interfaces Description

3.4.1 High Speed Data Interface

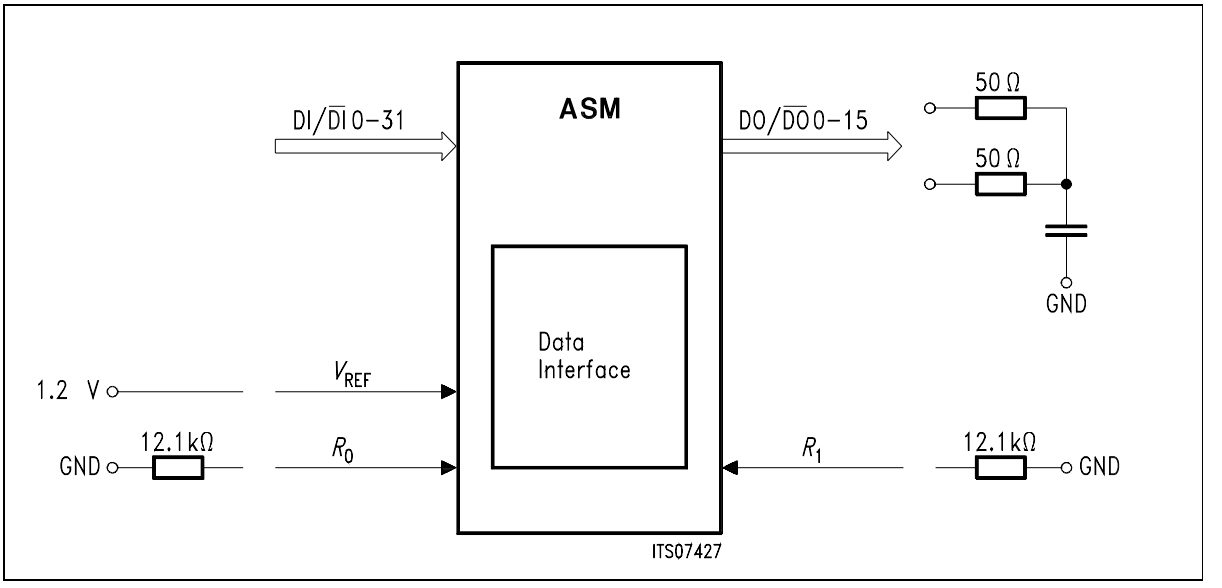


Figure 11 High Speed Data Interface

– **Data Inputs (DI/$\overline{DI}$)**
There are 32 separate pairs of complementary (‘differential’), high speed data inputs DI0/$\overline{DI0}$ … DI31/$\overline{DI31}$. Each of these is a serial NRZ input, operating at up to 208 Mbit/s and at LVDS levels.

Note: Open data inputs should be hold at defined and complementary levels or should be disabled in the Input Online Register IOR.

– **Data Outputs (DO, $\overline{DO}$)**
There are 16 separate pairs of complementary (‘differential’), high-speed data outputs DO0/$\overline{DO0}$ … DO15/$\overline{DO15}$. Each of these is a serial non-return to zero (NRZ) output, operating at up to 208 Mbit/s and at LVDS-levels. A termination resistor of 50 Ω has to be connected to each output line. Every two matching resistors belonging to one output pair are connected via a capacitor to the ground level.

Note: To avoid any improper high voltage operation potentially occurring with unconnected outputs, it is strictly recommended to terminate them always by a 50 Ω resistor.

– **Precision Reference Voltage (**VREF**)**
The precision reference voltage VREF [value: (1.2 ± 0.1)V] is used to define properly the internal current source of the input-/output-circuits together with the precision resistors R0 / R1.

VREF is connected directly to standard voltage generators. The current drawn by the VREF pin is less than 1 A (diode current).

– **Resistor Pin** R0
The external resistor R0, connecting the appropriate R0 pin and ground, is necessary to define the internal current sources of e.g. the data and clock inputs to the required current conditions.

Present value: R0 = 12.1 kΩ ± 1 % (precision resistor).

– **Resistor Pin** R1
The external resistor R1, connecting the appropriate R1 pin and ground, is necessary to define the internal current source of the data outputs to the required current conditions.

Present value: R1 = 12.1 kΩ ± 1 % (precision resistor).

3.4.2 Multicast RAM Interface

This interface (**Figure 12**) is used for the connection of an external synchronous SRAM (64 k × 18 bit) containing the multicast look-up table. It can be omitted if the multicast function is not desired.

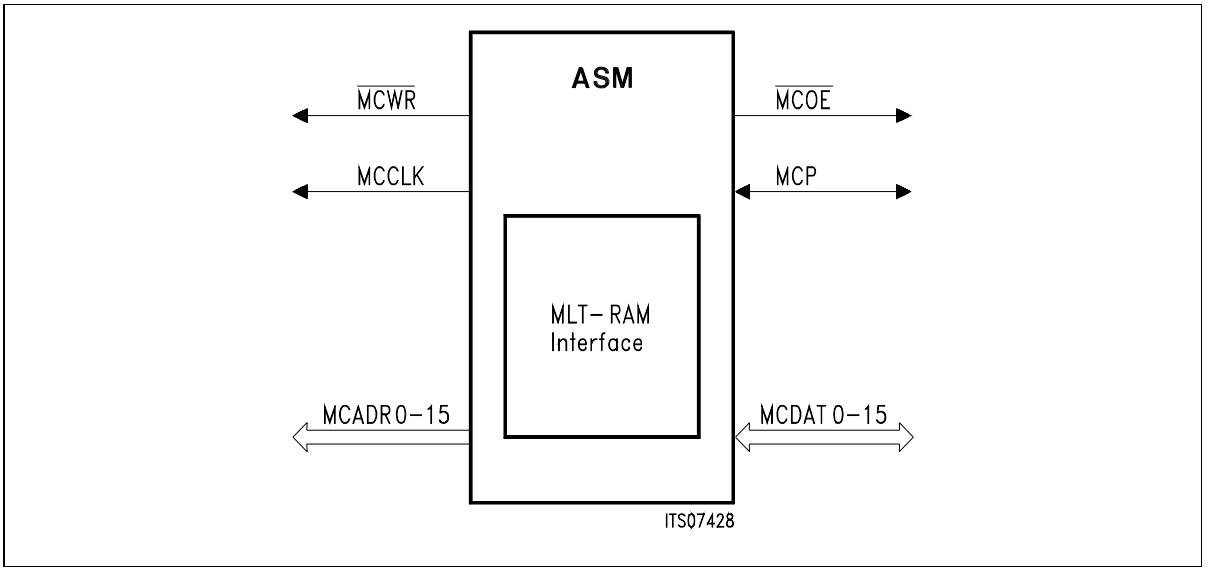


Figure 12 MC-RAM Interface

The interface consists of a sixteen-bit wide non multiplexed address bus (MCADR), a sixteen-bit wide bidirectional data bus (MCDAT), 1 data parity line (MCP), 1 clock signal (MCCLK) and two control lines ($\overline{\text{MCWR}}$, $\overline{\text{MCOE}}$) for the flow control. The clock line supplies the RAM with the ASM-internal octet clock (1/8 of the operating clock of up to 208 MHz). All the signals work with LVCMOS logic levels.

3.4.3 Device Test Interface

The Device Test Interface (see **Figure 13**) is used for production test only. During normal operation TMOD and TEST must always be connected to '0' (GND potential), the two test inputs TFI0,1 have to be held open or at '1'.

The Test Control outputs TCO0 … 9 and TFO0 … 6 should be left open.

Only the CLO and CSS outputs may be used for test purposes.

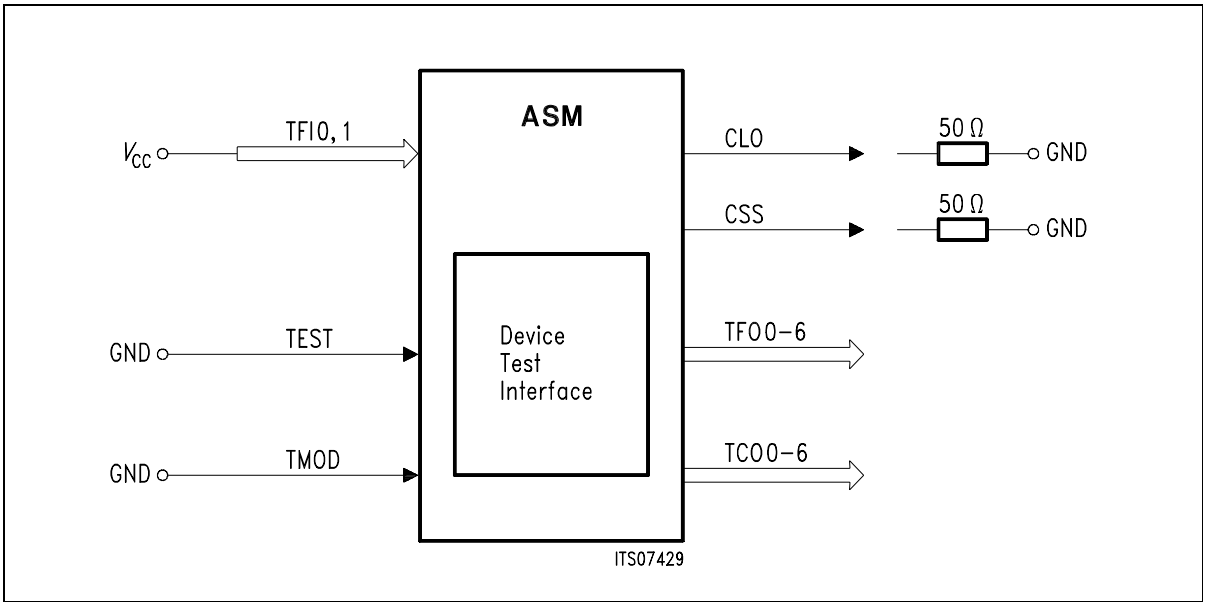


Figure 13 Device Test Interface

– **Clock Output Signal (CLO)**
The clock output signal CLO given out via a source follower output allows the observation of the operating clock of the ASM (frequency: up to 208 MHz) with an oscilloscope. Its positive edge clocks out the data and can be used to strobe the data output signals.

Since the output buffer employed is pulling up actively towards the supply voltage V_{CC} only, it has to be provided externally with a pull-down resistor of the recommended value of 50 Ω, to achieve a voltage swing of about 490 mV typical.

– **Cell Start Signal (CSS)**
The cell start signal CSS given out via an source follower output defines the 1st octet of the cells clocked out via the data outputs DO0/$\overline{DO0}$.

Therefore it can be used as a cell trigger signal.

For a proper operation the output employed has to be provided externally with a pull-down resistor of the recommended value of 50 Ω, to achieve a voltage swing of about 490 mV typical.

3.4.4 Boundary Scan

The boundary scan of the ASM complies the standard requirements according to JTAG with the following restrictions:

- High speed data inputs and outputs can only be observed
- No self test possibility

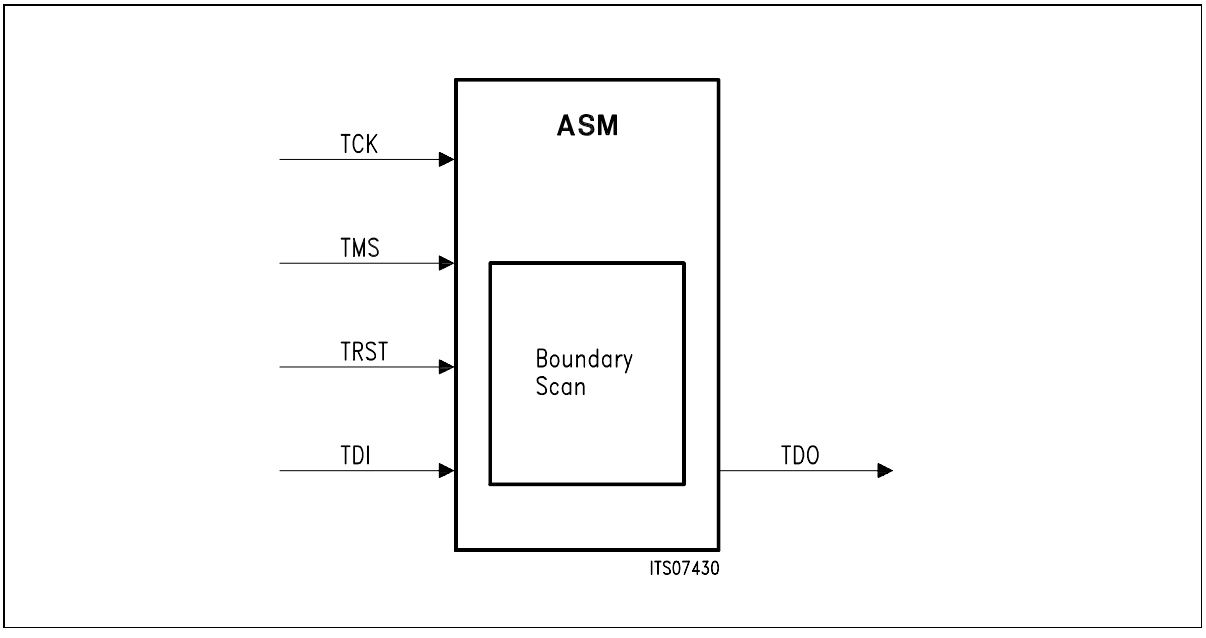


Figure 14 Test Interface (Signals, Loading)

– **Test Clock Input (TCK)**
This control input needs a system-independent test clock.

– **Test Mode Select (TMS)**
This control input is used for the initialization of the Test-Access-Port controller (TAP controller).

– **Test Data Input (TDI)**
All test information is serially loaded into the ASM via this data input. The data are taken over with the rising edge of TCK.

– **Test Data Output (TDO)**
All test information left the ASM via this data output with the falling edge of TCK.

– **Test Reset (TRST)**
Asynchronous reset for the TAP controller (low active). The state of the TAP controller is not influenced by the system reset (RESET pin) of the ASM.

3.4.5 Microprocessor-Interface

This interface consists of an eight bit wide, generic, non multiplexed microprocessor bus as required for interfacing of 80x86 processors, and of additional control lines as shown in **Figure 15**. All the signals work with LVCMOS logic levels.

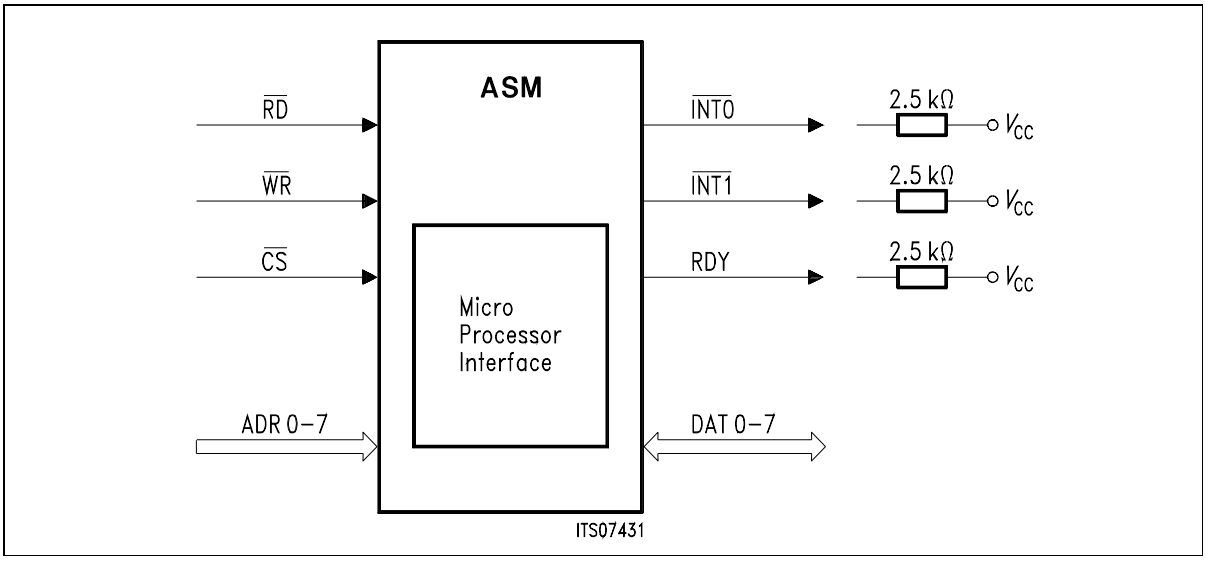


Figure 15 µP-Interface

– **Data Signals (DAT0 … DAT7)**
There is a 8-bit wide bidirectional data interface between the µP and the ASM to gain access to the different internal register sets inside the ASM. It is controlled by the chip-select- ($\overline{CS}$), read- ($\overline{RD}$), and write-signals ($\overline{WR}$). During the non-selecting phase ($\overline{CS}$ inactive) the port is switched into the inactive high impedance state. With $\overline{CS}$ active ($\overline{CS}$ = '0'), the data bus is configured as an input port during a write cycle and as an output port during a read cycle.

– **Address Signals (ADR0 … ADR7)**
The 8-bit wide common unidirectional address bus performs the selection of the ASM internal registers for the read or write cycles.

– **Bus Control Input Signals ($\overline{CS}$, $\overline{RD}$, $\overline{WR}$)**
There are three control inputs with common low active signals to select the chip ($\overline{CS}$) and to determine the data direction for the proper read ($\overline{RD}$) or write ($\overline{WR}$) operation from or to the selected register inside the ASM.

– **Ready Output Signal (RDY)**
The active high ready signal realized as an open drain output supports the interfaces under different speed requirements. During a bus cycle with a control line $\overline{RD}$ or $\overline{WR}$ becoming active (High to Low transition) the ready signal will be forced low to indicate that this access to an internal register may have to insert wait states (not ready state). After the necessary reaction time of the ASM, it returns to a high level indicating that

the data are stable and that the bus cycle can be finished by the microprocessor with $\overline{WR}$ or $\overline{RD}$ returning to a high level.

Since the output is only pulling down actively to GND an external pull-up resistor has to be provided with the recommended value of 2.5 kΩ.

– **Interrupt Output Signal ($\overline{INT0}$)**
The active low interrupt ($\overline{INT0}$), realized as an open drain output is provided to indicate that a µP-cell was received or that an error has been detected by the ASM. After reading the RCR register (at least octet 63) or resetting the RX-bit (RX = '0', bit 7) in the command register COR respectively after reading the interrupt status register ISR, this signal will become high. Since the output is only pulling down actively to GND an external pull-up resistor has to be provided with the recommended value of 2.5 kΩ.

– **Interrupt Output Signal ($\overline{INT1}$)**
The active low interrupt ($\overline{INT1}$), realized as an open drain output is provided to indicate that a communication cell (HK = 110 and MODR:EINT1 = 1) was received by the ASM. After reading the RCR register (at least octet 63) or resetting the RX-bit (RX = '0', bit 7) in the command register COR this signal will become high. Since the output is only pulling down actively to GND an external pull-up resistor has to be provided with the recommended value of 2.5 kΩ.

3.4.6 Clock and Reset

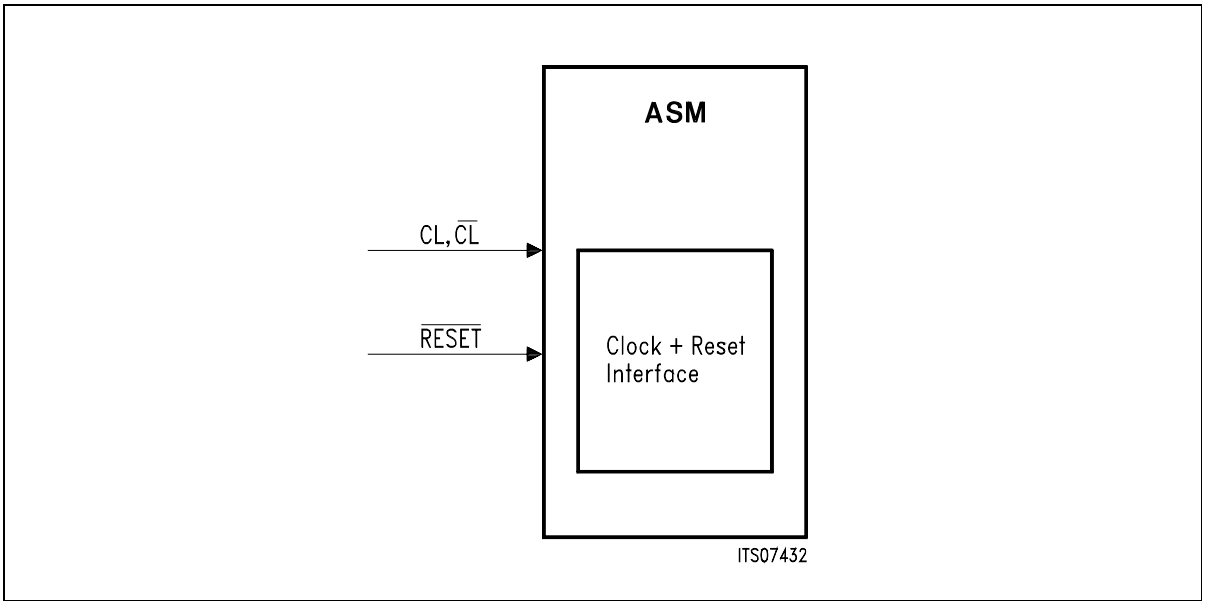


Figure 16 Clock and Reset Interface

– **Clock Inputs (CL/$\overline{CL}$)**
The central operating clock is running at up to 208 MHz, which is identical to the system frequency. It is complementarily fed in via the clock inputs CL and $\overline{CL}$ (differential inputs).

Level: Both inputs work at the LVDS levels.

Note: The loss of the operating clock may cause an increase of the power dissipation. In order to hold this increase low, it is strictly recommended, to supervise the board clock operation: If the clock fails, an active Hardware Reset (RES = 0) should be delivered to the ASM devices concerned.

– **Reset Input Signal (RESET)**
The RESET-signal is fed in via a LVCMOS-compatible input. Whenever it is at the low state '0' (GND) and then switched from the low state '0' to the high state '1', it causes a reset of the switch internal circuitry:

RESET = '0' active (reset of the converter circuits)

RESET = '0' → '1' active (general reset of the control and clock circuitry)

RESET = '1' inactive (no influence)

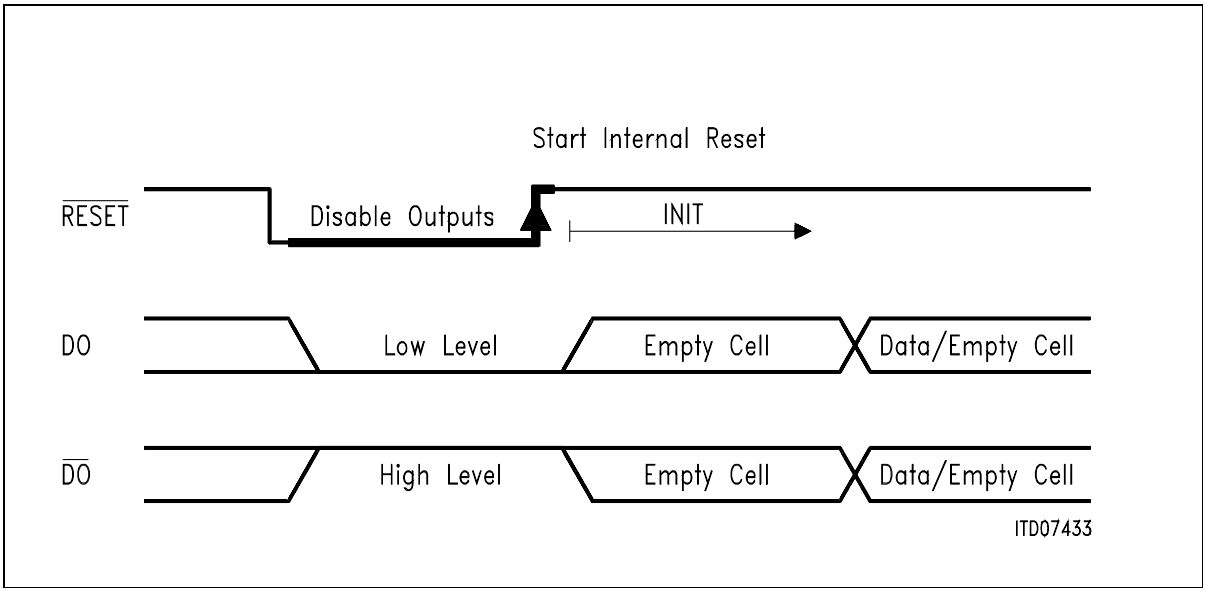


Figure 17 RESET Signal

An active HW-reset causes an initialization of the whole ASM, including all the registers. The influence of the RESET signal to the serial outputs is shown in **Figure 17**. During the active RESET signal the differential outputs are held at constant values. After the RESET signal becoming inactive an empty cell is sent out at each of the 16 outputs. During that time the initialization of some internal circuits occurs. In the second cell slot the first data cells may be transmitted, if any.

– **Software Reset**
A Software reset is activated by the µP by setting the SRES-bit of COR to ‘1’. This action causes the reinitialization of all the queues, of the FCL-RAM, MCC-RAM and the maintenance register MR.

The phase-alignment circuitry of the input lines and the cell synchronism of the outputs remain unaffected by this operation, as the empty cell generator is activated to permanently transmit empty cells as long as the software reset is kept active.

As soon as the reinitialization procedure is completed, the software reset is deactivated by the ASM by setting SRES to ‘0’.

3.5 ATM Cell Format

The ASM uses a proprietary 64-octet ATM cell format. It is shown in **Figure 18** for self-routing and in **Figure 19** for multicast cells.

The shaded areas represent bit fields, which are transparent to the ASM, while the ‘open’ fields will be evaluated by the ASM (routing information).

The term ‘external header’ denotes the standardized, 5-octet header of the ATM cell. The internal header is added by the ASP and comprises 10 octets. A one octet trailer is appended at the end of the internal cell and carries a checksum. It is not evaluated by the ASM, but only by the ASP at the outgoing side.

Table 1 explains the used header bytes.

The MCRA 19 … 16 bits are not evaluated by the ASM. They are reserved for further expansion of the number multicast connections.

The auxiliary bits AUX 20 … 31 can be used for routing information in multicast cells. As some ASMs in the switching network may be programmed to treat the multicast cells as self-routing cells, these ASMs would be programmed to ‘look’ for routing bits within this field.

The following two figures show the structure of empty cell (**Figure 20**) and Protection Switch Identifier PSI cell (**Figure 21**).

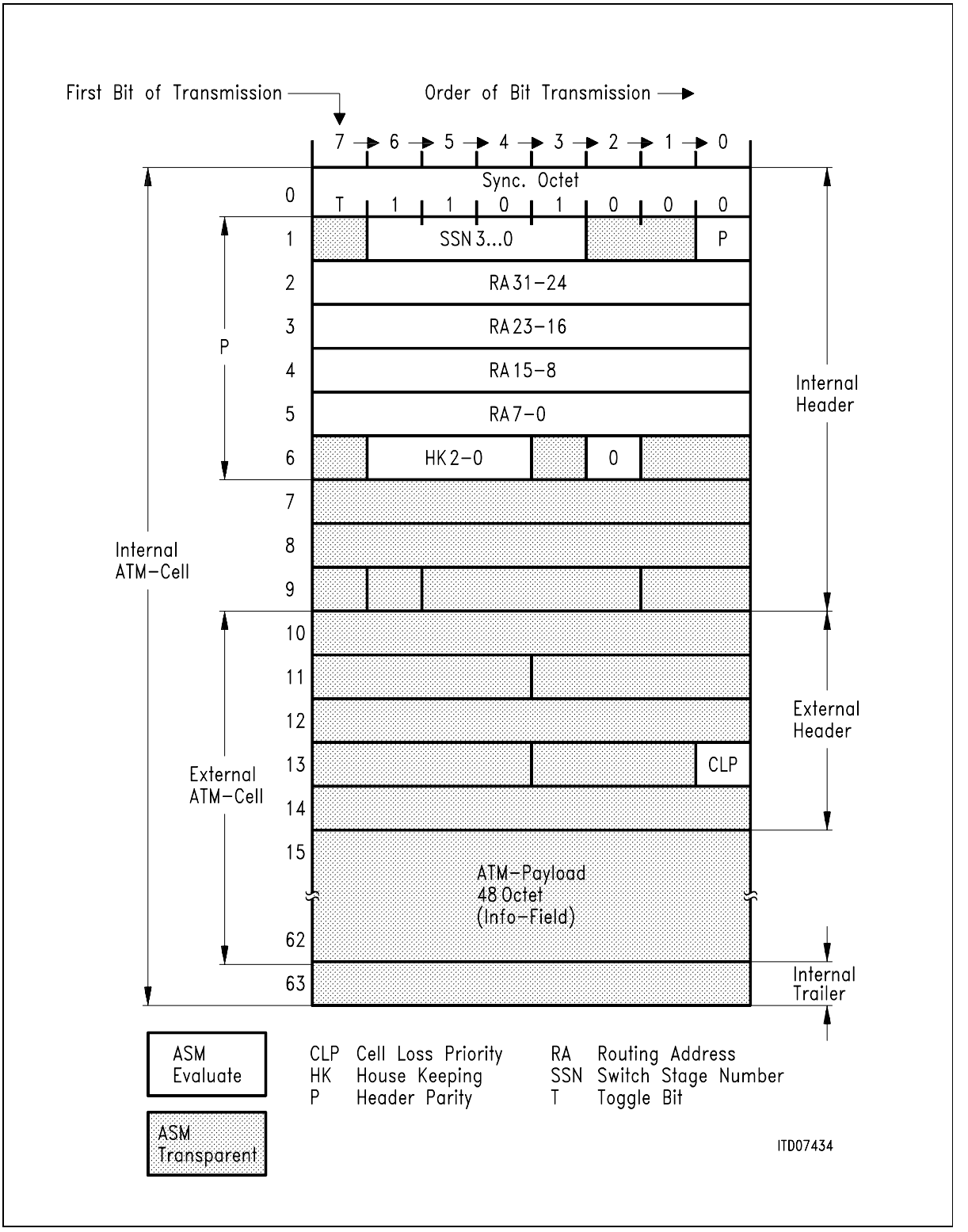


Figure 18 Format of Self-routing ATM Cell

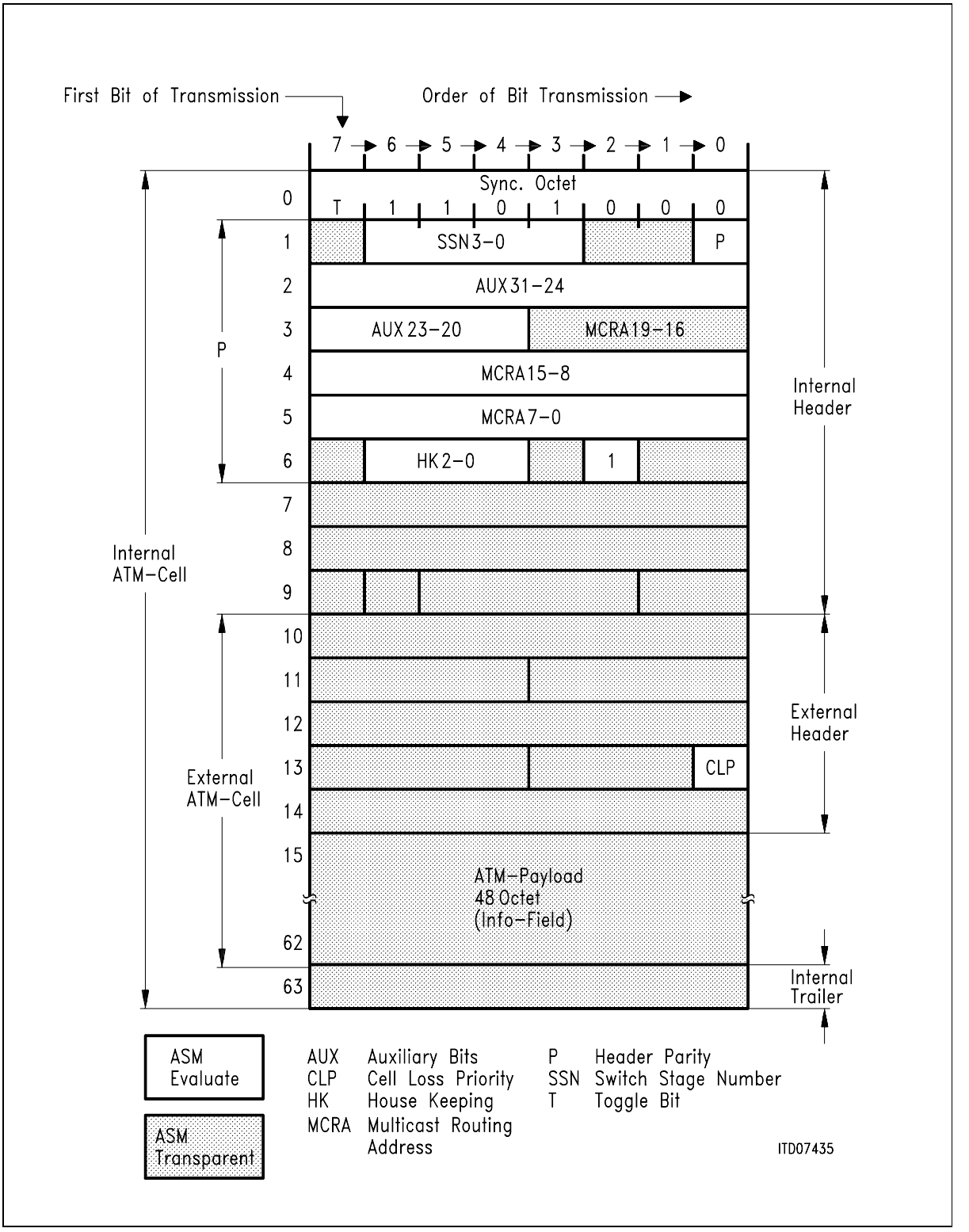


Figure 19 Format of Multicast ATM Cell

Table 1 Description of Used Header Fields

Abbr.	Bits	Meaning	Comment	
ADI	2	Address identifier	To identify the RA type:	
			ADI	RA field
			X0	Routing address
			X1	Multicast routing address
AUX	12	Auxiliary bits	In case of DCMC = '1' and EVMCI = '0' in the MODR-register, the AUX-bits can be used as routing address	
CLP	1	Cell loss priority	1 = low priority cell; 0 = high priority cell	
HK	3	House keeping	Cell type identifier	
			HK	Cell type
			000	Empty cell
			011	Maintenance control cell; not influenced by output multiplexer
			110	Control cell; cause a $\overline{INT1}$-request instead of an interrupt $\overline{INT0}$
			other	Standard operation
MCRA	20	Multicast routing address	MCRA 19 … 16: Not evaluated by the ASM.MCRA 15 … 0: Address used for the multicast lookup table (MLT, external sync. SCRAM)	
P	1	Header parity	For internal header (octet 1 … 6), odd parity	
RA	32	Routing address	Variable, depending on the initialization of the ASM	
Res	2	Reserved		
SSN	4	Switch stage number	To mark the ASM in the different stages; for normal routing, not using the µP-output of the ASM, the SSN has to be set to SSN = 0000_B	
Sync.	8	Synchronization octet	Cell start identifier with toggle bit (first bit of transmission), hex-value: $68_H/E8_H$	

Octet	7	6	5	4	3	2	1	0	Hex-val.
0	T	1	1	0	1	0	0	0	68/E8
1	0	0	0	0	0	0	0	1	01
2	0	0	0	0	0	0	0	0	00
3	0	0	0	0	0	0	0	0	00
4	0	0	0	0	0	0	0	0	00
5	0	0	0	0	0	0	0	0	00
6	0	0	0	0	0	0	0	0	00
7	0	0	0	0	0	0	0	0	00
8	0	0	0	0	0	0	0	0	00
9	0	0	0	0	0	0	0	0	00
10	0	0	0	0	0	0	0	0	00
11	0	0	0	0	0	0	0	0	00
12	0	0	0	0	0	0	0	0	00
13	0	0	0	0	0	0	0	1	01
14	0	0	0	1	1	0	0	1	19
15	0	1	1	0	1	0	1	0	6A
:									:
61	0	1	1	0	1	0	1	0	:
62	0	1	1	0	1	0	1	0	6A
63	1	1	1	1	1	0	0	1	F9

Figure 20 Format of Empty Cell

Octet	7	6	5	4	3	2	1	0	Hex-val.
0	T	1	1	0	1	0	0	0	68/E8
1	0	0	0	0	0	0	0	1	01
2	0	0	0	0	0	0	0	0	00
3	0	0	0	0	0	0	0	0	00
4	0	0	0	0	0	0	0	0	00
5	0	0	0	0	0	0	0	0	00
6	0	0	0	0	1	0	1	0	00
7	0	0	0	0	0	0	0	0	00
8	0	0	0	0	0	0	0	0	00
9	0	0	0	0	0	0	0	0	00
10	0	0	0	0	0	0	0	0	00
11	0	0	0	0	0	0	0	0	00
12	0	0	0	0	0	0	0	0	00
13	0	0	0	0	0	0	0	1	01
14	0	1	0	1	1	0	0	0	19
15	0	1	1	0	1	0	1	0	6A
:									:
61	0	1	1	0	1	0	1	0	:
62	0	1	1	0	1	0	1	0	6A
63	1	1	1	1	1	0	0	1	F9

Figure 21 Structure of Protection Switch Identifier Cell

3.6 Examples for System Integration

The ASM can be operated stand-alone as a 16×16 switch of 2.5 Gbit/s throughput by just leaving 16 inputs open. Larger switching networks can be built by interconnecting several ASMs in arrays. Two possible expansion schemes are described in the following, funnel-type and Banyan networks. Note, however, that many more options exist to build switching networks using other network types and/or combinations of them (see e.g. the book of **Händel, Schröder, Huber [5]** for further study). Due to the flexible routing header concept the switching network can be optimized for each application.

3.6.1 Funnel-Type Switching Networks

The simplest funnel-type switching network is obtained by connecting two ASMs in parallel as shown in **Figure 22** They constitute a 32×32 switching network. Each incoming cell is input at both ASMs and each ASM filters out those cells which are destined for its outputs and discards the other cells. Each line in **Figure 22** stands for 16 parallel SLIF lines.

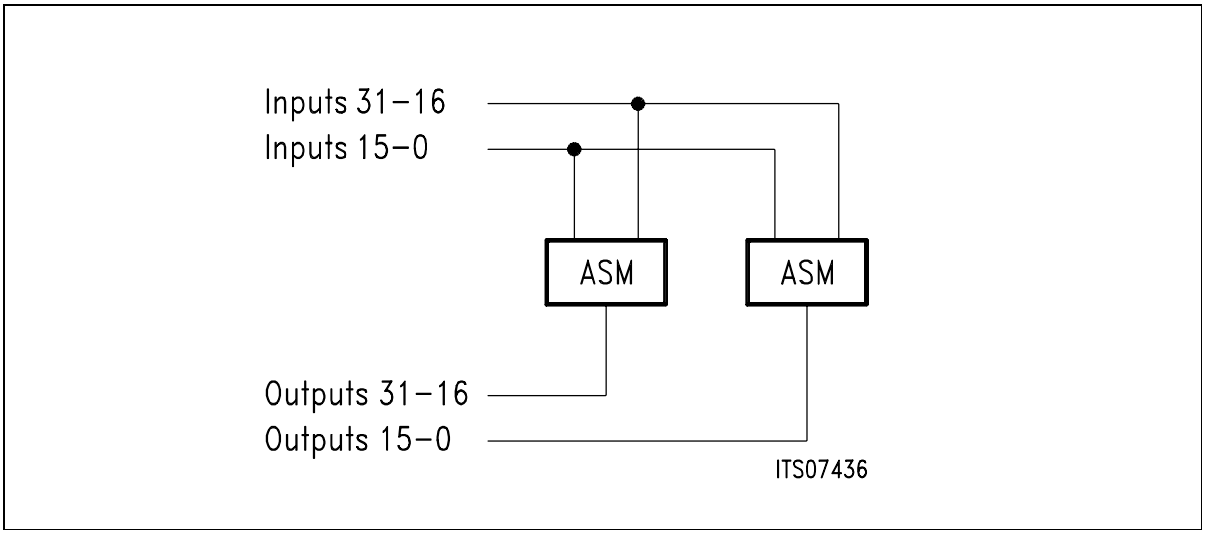


Figure 22 5 Gbit/s Switching Network

The next size of a funnel-type switching network is a 64×64 switch realized with 12 ASM chips (see **Figure 23**).

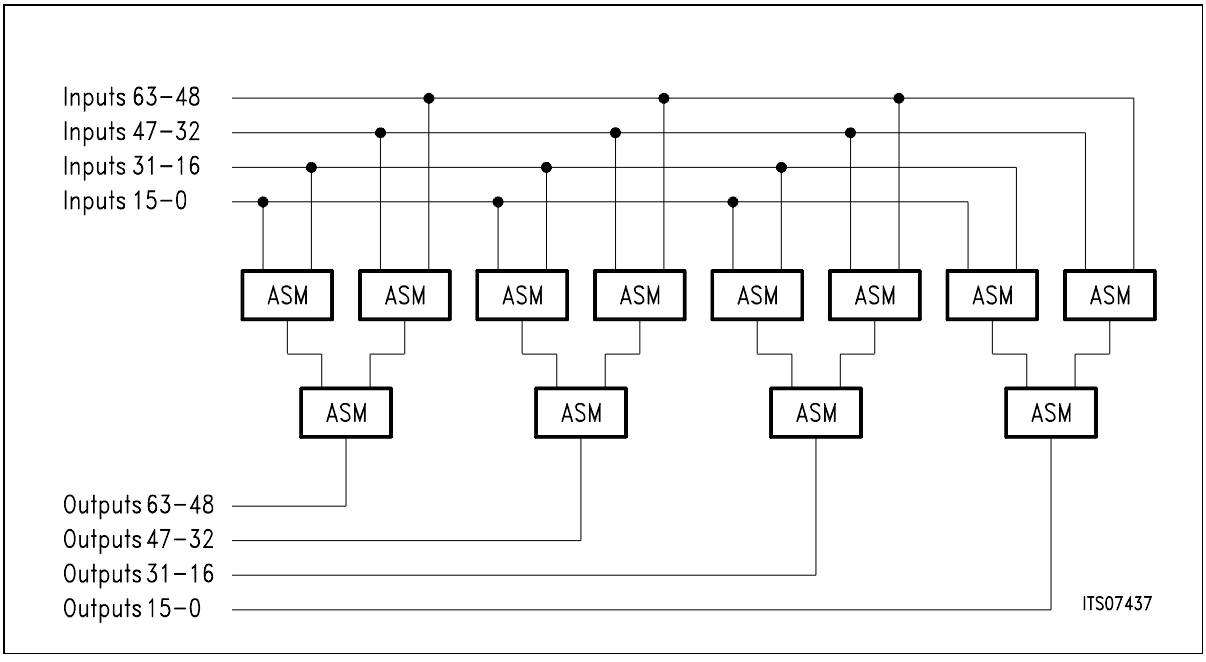


Figure 23 10 Gbit/s Switching Network

The switching network of **Figure 23** consists of 4 ‘funnels’, each built with 3 chips. The 2 ASMs of the first row have different filter values programmed for each funnel. Their outputs are grouped as one 16-bundle, i.e. there is only one logical output. The ASM of the second row of each funnel does the routing evaluation, i.e. it forwards the cells to the specified output or output bundle. See **Chapter 6.1** for programming details.

The next size of a funnel-type switching network is a 128×128 switch realized with 56 ASM chips. It consists of 8 funnels of 7 ASMs with the 128 inputs of all funnels connected in parallel. **Figure 24** shows the first of the 8 funnels.

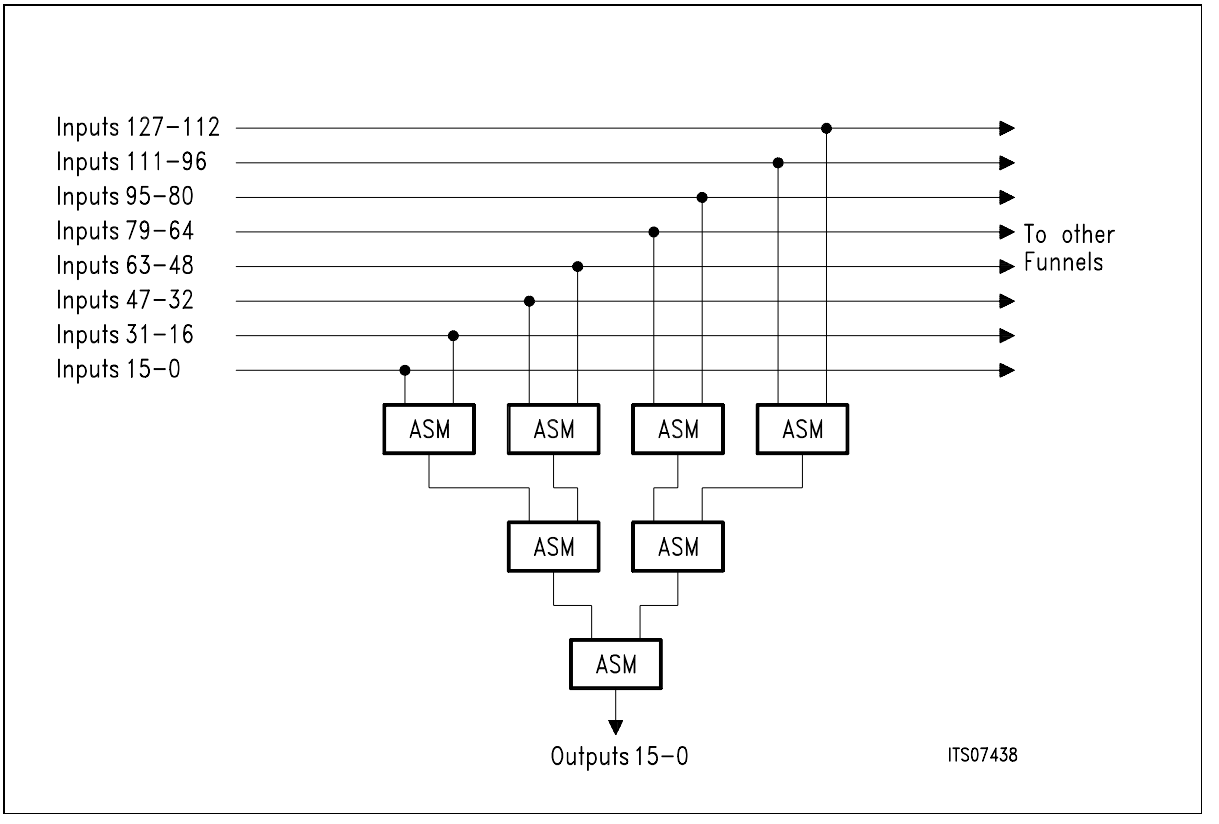


Figure 24 7-Chip Funnel for 20 Gbit/s Switching Network

The following diagram shows possible switch sizes and the required number of ASM chips for funnel-type switching networks.

Table 2 Size and Chip Count for Funnel-type Switching Networks

No. of Stages	No. of ASMs	Switch Size	Switch Throughput [Gbit/s]
1	2	32×32	5
2	12	64×64	10
3	56	128×128	20
4	240	256×256	40

The general expressions for funnel-type switching networks with s stages using a 2 b $\times$ b switching chip are:

Number of funnels = 2^S,

Number of switch ports = $b \times 2^S$,

Number of switching chips = $(2^S - 1) \times 2^S$.

Note that funnel-type switching networks are ‘non-blocking’. This term is defined in the following way in this document:

Note: A switching network is non-blocking if all input and output lines have the ATM cell load L, the load L is not exceeded at any interconnection line between ASMs. This means that any mixture of connections can be set-up between inputs and outputs without considering the interconnection lines.

If e.g. in a non-blocking switching network a connection is to be set-up from input j to output k, it has just to be checked if input j and output k both have enough spare bandwidth. If this is the case the connection can be set-up and there will be no overload on any of the used interconnection lines.

The non-blocking feature is easily checked for the funnel-type networks. If the output load of a funnel has the value L, the input load of the last stage has the value L/2, the input load of the last but one stage has the value L/4 and so on. The traffic in the funnel is more and more concentrated.

3.6.2 Banyan Switching Networks

Banyan networks belong to the class of single-path networks, i.e. there is only one single path from an input to a given output. Banyan network have the advantage to be less chip consuming than funnel-type networks, but they are blocking. An implication for the network control SW is that for Banyan networks it must keep track of the load on all interconnection links.

As described above depending on the distribution of connections between inputs and outputs a new connection may have to be rejected because of an overload on an internal line even if input and output line have the required capacity available. The probability for such a blocking event is depending on the load of the network. As shown in a paper by **Theimer [6]** the blocking probability is negligible if the load is below 50 %. This can be achieved by various means:

- The application itself has low average load. This could be the case e.g. in a LAN environment, where most of the switch ports are connected to PCs. Banyan networks are especially useful for LANs, as they allow to connect a large number of PCs.
- The traffic load can be reduced by using two switching network planes in the load sharing mode.
- Another method to reduce the load on the interconnection lines is to use bundles. This, however, reduces the maximum size of the switching network (**Figure 26**).

Figure 25 shows a generic Banyan network with 3 stages consisting of b $\times$ b switching elements. It contains b times the 2-stage sub-network shown in the frame.

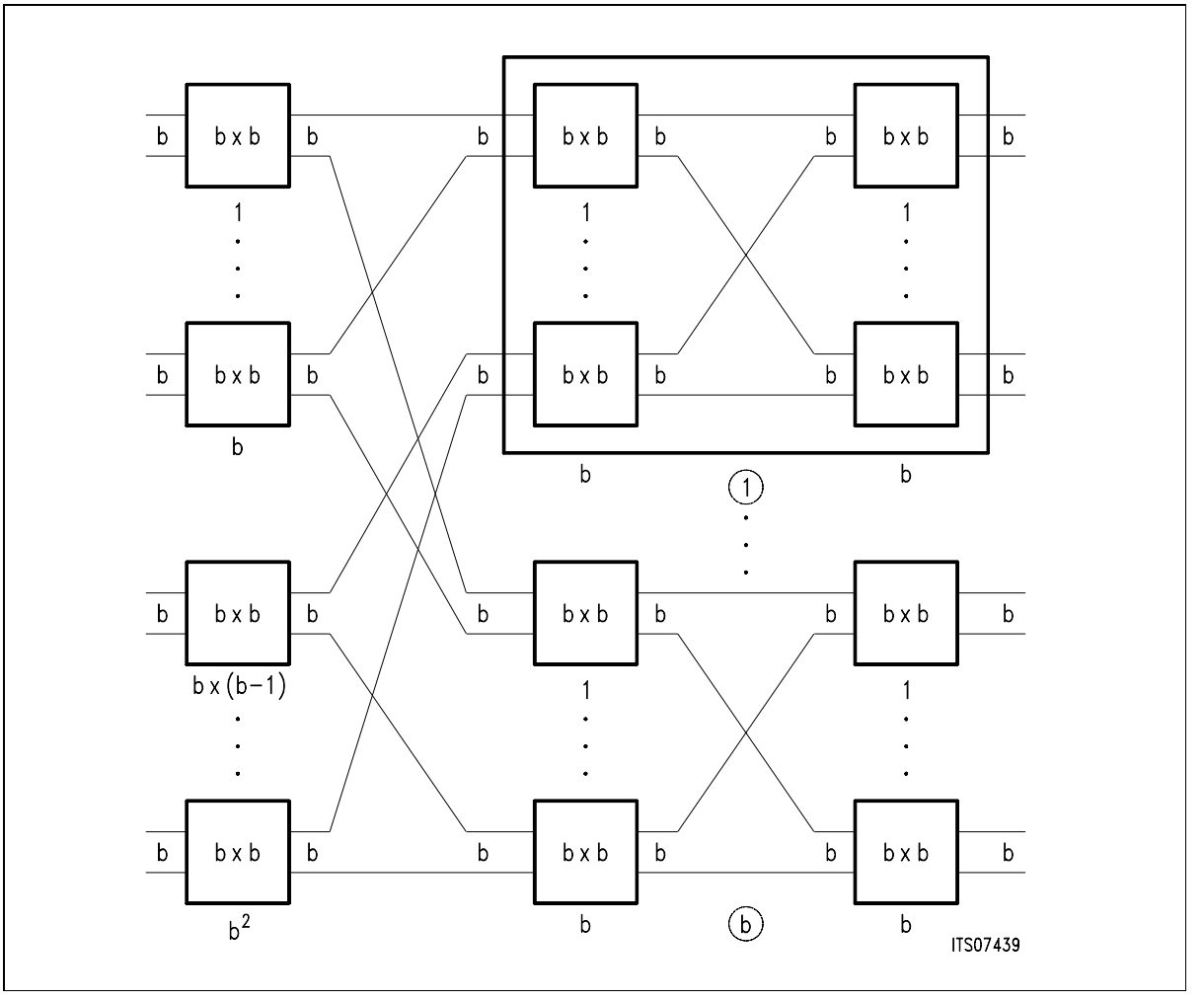


Figure 25 Generic Banyan Network

The 3-stage switching network built with switching elements of size b × b has b^3 ports.

Using ASM chips there are two possibilities for the b × b element:

1. Either a single ASM can be used with 16 inputs unconnected giving a switching element of size 16 × 16 or
2. Pairs of 2 ASMs can be built in a mini-funnel (see **Figure 22**) giving a switching element of size or 32 × 32.
3. The non-blocking 10 Gbit/s funnel (**Figure 23**) can be used, giving b = 64.

The switch sizes realizable with both possibilities are summarized in the table below together with the required number of ASMs.

Table 3 Size and ASM Chip Count for Banyan Networks

Switching Element	No. of Stages	No. of ASMs	Switch Size
16×16	1	1	16×16
	2	32	256×256
	3	1768	4096×4096
32×32	1	2	32×32
	2	64	1024×1024
	3	3072	32768×32768

It can be seen that Banyan networks are much more effective than funnel-type concerning chip count: E.g. with 56 ASMs a funnel-type switch of size 128×128 can be built, whereas 64 ASMs are required for a 1024×1024 Banyan-type switch.

The ASMs in Banyan networks do not need the filter function, but only the routing functionality. In each stage the ASM chips will be programmed to evaluate different parts of the routing field of the internal cell header.

As mentioned above the interconnection lines between ASMs in Banyan networks can be bundled. An example is shown in **Figure 26**.

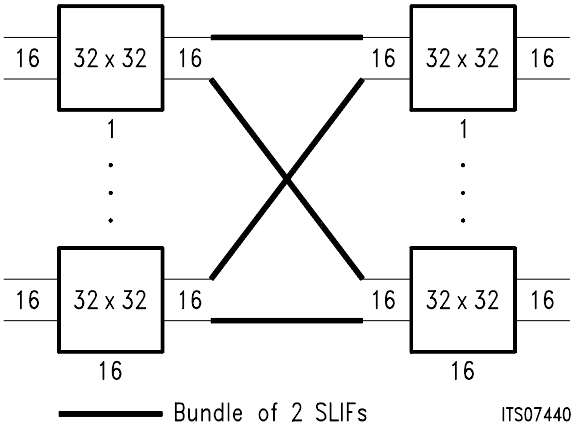


Figure 26 40 Gbit/s Banyan Switch with Bundles of 2

Each 32×32 switching element in **Figure 26** consists of a mini-funnel as shown in **Figure 22**. The 32 outputs of the switching elements of the first stage are combined to 16 2-bundles. This reduces the load on the interconnection lines to below 50 %. The

switching network is still more chip saving than the funnel-type network of the same size: It needs 64 ASMs instead of 240.

3.6.3 Multiplexers/Concentrators

Both funnel- and Banyan-type switching network cores can be expanded by adding multiplexers to concentrate the incoming traffic. This is especially useful if subscribers/terminals must be connected to the switch. These are expected not to use the available capacity completely all the time. Appropriate concentration allows more efficient use of the precious switching core. A generic configuration of a switching network core expanded by multiplexers is shown in **Figure 27**.

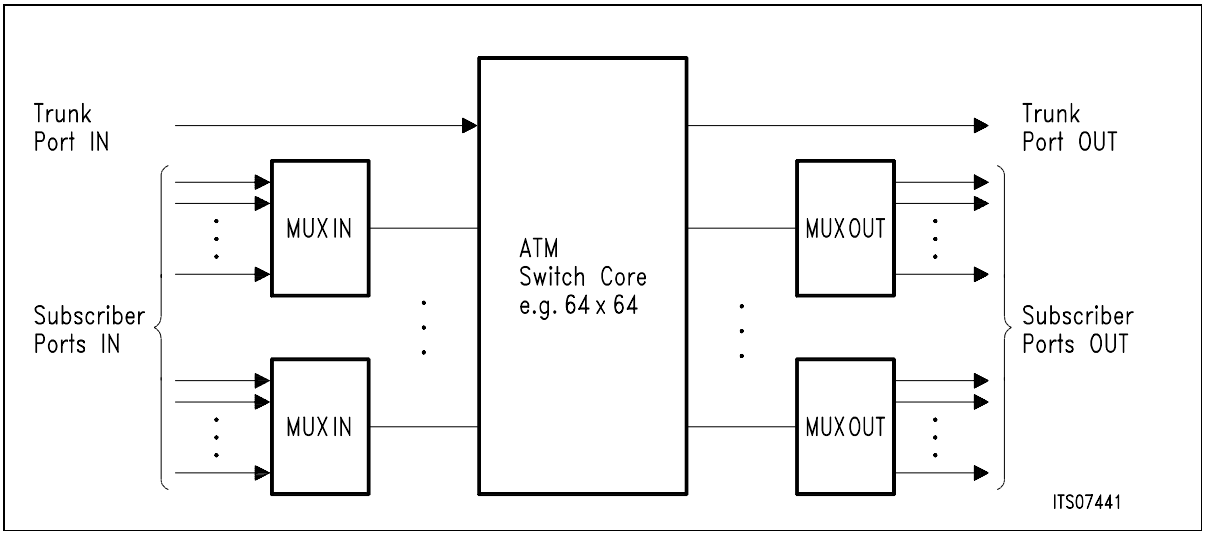


Figure 27 A Switching Network Expanded by Multiplexers

Some of the ports of the switch core in **Figure 27** are connected directly to the switching core. These could be trunk ports (in WAN applications) or server ports (in LAN applications). The other ports are expanded by multiplexers. Each multiplexer concentrates traffic from subscribers (WAN) or terminals (LAN). In both cases applications which are assumed to have low average traffic.

There are three different operation modes for the ASM to support multiplexers:

– The input multiplexer is used e.g. to concentrate the traffic of several subscriber/terminal ports to one (core) switch port. In this mode the ASM forwards all cells to one output bundle.
– The output multiplexer is used for demultiplexing an aggregate cell stream from a switch core port to different access ports. In this mode the ASM evaluates a part of the routing field of the internal cell header to determine the output.
– In split mode one ASM operates as both input and output multiplexer. In this mode one group of inputs is defined to operate in normal mode including filter, routing and multicast options. Cells coming in at these inputs are forwarded to one output

(bundle). The cells input at the other group of input lines are treated in a special way; they are forwarded to the outputs using a predefined field of the routing field.

An application example of an ASM in split mode is shown in **Figure 28** below. In this example 12 (subscriber) line cards are multiplexed onto a bundle of 4 SLIF lines. A bundle has the advantage that the load management has to consider only one logical 622 Mbit/s equivalent link instead of four 155 Mbit/s equivalent links.

Inputs 0 … 3 work in MUXIN-mode, all other inputs in MUXOUT-mode. Inputs 16 … 31 are not connected. It can be seen that each line card has a mean bit rate of 622 Mbit/s / 12 = 51.8 Mbit/s to the core – without taking the short path traffic into account. The ASM allows short path connections from one LIC directly to an other LIC, which do not influence the traffic to the switch core. See **Chapter 6.1** for a programming example for a split mode multiplexer.

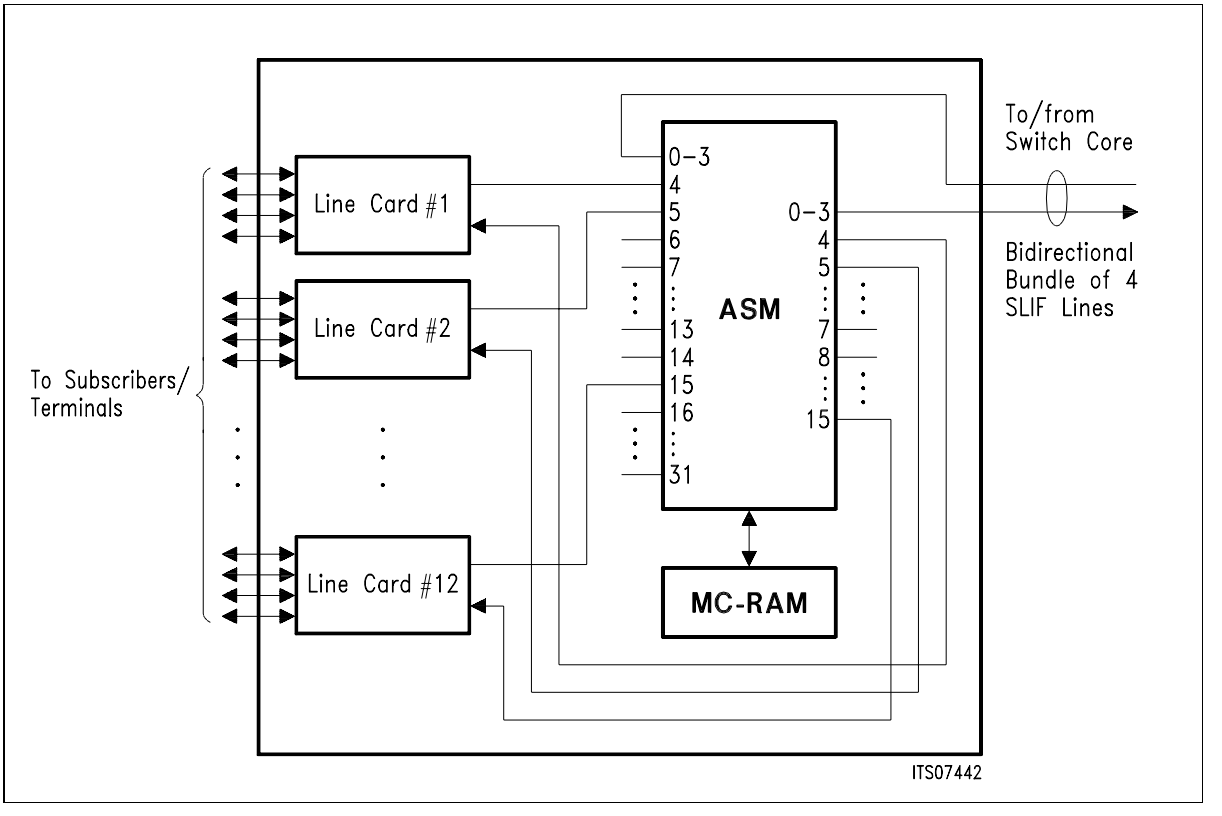


Figure 28 Single Chip Bidirectional Multiplexer

Note that an ASM could also operate stand-alone in a configuration as in **Figure 28** by omitting the lines to the switch core. In such a case it constitutes a 16×16 switching network. Considering the bit rate of roughly 155 Mbit/s for each line, an ATM switch with a total throughput of 2.48 Gbit/s can be realized with only one ASM.

3.6.4 Multicast Operation

The multicast function is usable in all modes except the multiplexer mode where all cells are forwarded to one output. If a multicast header is detected by an ASM the MCRA field of the routing header is used as address to the multicast lookup table. This is an external RAM of 64 k entries of 17 bits which is initialized by the microprocessor. 16 bits of each entry are associated to the outputs of the ASM (the 17^{th} bit is a parity bit). A cell is forwarded to those outputs where the corresponding bit is set. Obviously the following special cases are possible:

– No output bit is set ⇒ the multicast cell is discarded.
– Only one output bit is set ⇒ the cell is forwarded to one output only as in the normal routing case.
– All output bits are set ⇒ full broadcast case, the cell is replicated to all outputs.

Note: For a multicast connection the same MCRA must be set-up in the whole switching network, also in those ASMs where no branch of the multicast connection passes through. The reason is that at any time an additional branch could be added to a multicast connection (via signalling). If the same MCRA would be used for another connection these two connections could not use the same ASMs. The total number of multicast connections in the whole switch is therefore limited to 64 k.

In a funnel-type switching network only the last stage needs a multicast lookup table, the other stages can be programmed to forward multicast cells as normal cells. Thus the external RAM is only required once per funnel (see **Figure 32**).

Some Notes about Multicast

Multicast connections require a significant amount of ‘work’ to be set-up, i.e. the switch control has to check on all outgoing branches if capacity is available, has to find free VCIs and load these onto the line cards; also for a 1:n multicast connection n backward (merger) connections have to be set-up; it is almost the same effort as to set-up individual one-to-one connections.

Also the OAM (operation, administration and maintenance) functions for one-to-many connections are still unclear, e.g. in case that the connection fails a flood of backward error notification cells will be produced.

However, not all of the multicast applications do translate into multicast connections on the ATM layer; e.g. the many-to-many connections in LANs are resolved in ATM LANs by a single one-to-many connection from the server to the users, or as another example a multi-party video conference does not require multicast ATM connections, as none of the users will have the same picture on the screen; a video conference server will be used to arrange the picture individually for each party.

4 Functional Blocks Description

4.1 Bit Phase Alignment

Each of the data inputs is equipped with a Bit Phase Alignment Circuitry. Its main tasks are to compensate for both jitter and possible wander of the input data streams and to align the incoming bit stream to the internal clock of the ASM.

4.2 Cell Detection

The Cell Detection Circuits are situated just behind the Phase Alignment Blocks. Their primary function is to identify and check the Synchronization Octet (<T110 1000>, T = toggle bit), which defines the octet position and the cell start. The result of the check is used to derive the line state.

If only one cell with invalid SYNC-octet occurs, i.e. the following cell has got a valid SYNC-octet, the cell is passed through. The line errors are reported in the Line Failed Register LFR, the Line Error Register LER, and the Interrupt Status Register ISR. If more than one cells with invalid SYNC-octet are received the first is accepted the second is discarded.The second cell also leads to asynchronous state where all cells are discarded. Transition to synchronous state is achieved after 2 cells with valid SYNC-octet. The third cell with valid SYNC-octet is accepted.

The line state is mapped into the Line Asynchronous State Register LASR; line errors are reported in the Line Failed Register LFR, the Line Error Register LER, and the Interrupt Status Register ISR.

4.3 Deactivation of Input Ports

Ports can be deactivated via the Input Online Register IOR. This will discard all cells from this ports without any header check, but the line status will still be reported in LASR and LER.

4.4 Check of Header Parity Bit

The octets 1 to 6 of the internal header are protected by a parity bit P, which is checked for every cell. If a parity error has been detected, the cell is discarded. The error is mapped into the Line Failed Register LFR and the Interrupt Status Register ISR:PE.

4.5 Device-internal Cell Parity Byte

All cells are provided with a trailing odd parity byte covering the whole cell except the Synchronization Octet. The parity generation is done in a byte interleaved way, with every parity bit ‘i’ covering all the bytes at bit number ‘i’ throughout the whole cell.

The parity byte is checked at each output port at the location where the data is in octet format, before the final p/s conversion is done.

An Internal Parity Error is reported in the Interrupt Status Register ISR:IPE. No further action can be provided to mark this corrupted cell. The cell will be discarded by the ASP in downstream direction.

4.6 Empty Cell Removal/Insertion

All Empty Cells from the input ports are discarded. They are identified by the Housekeeping Bits <000>. Except the check of the header parity P no other inspection is done, so that all cells with the Housekeeping <000> are discarded independent from any other cell data.

New Empty Cells are generated for an output port, if no other cell is available, i.e. the output queue is empty, or the port is disabled.

Cells with Housekeeping <000> that have been fed in via the µP-interface, are treated as empty cells and therefore discarded.

4.7 Output Port Bundling

Output ports can be bundled to make it possible to switch links with higher data rate. Groups of 2, 4, 8, and all 16 outputs can be configured via the Output Group Register OGR:OG. Each output port bundle uses one common output queue. The ports send the cells in a staggered mode, so that the original cell sequence can be recovered by the input scan algorithm of the following ASM or ASP. For groups of 16 input ports a different algorithm is used (see **Figure 30**), and therefore they must be specified in the Mode Register MODR:IGx.

4.8 ATM Cell Sequence

Independent from any specified output bundle, the output ports transmit the cells in staggered mode, i.e. the Cell Starts in the 16 output streams are not simultaneous but have a fixed delay to each other. The cell sequence starts with port 0. Port 1 transmits the next cell start 3 octet clocks (= 24 system clocks) delayed in relation to the Cell Start on port 0. The sequence is shown in **Figure 29**.

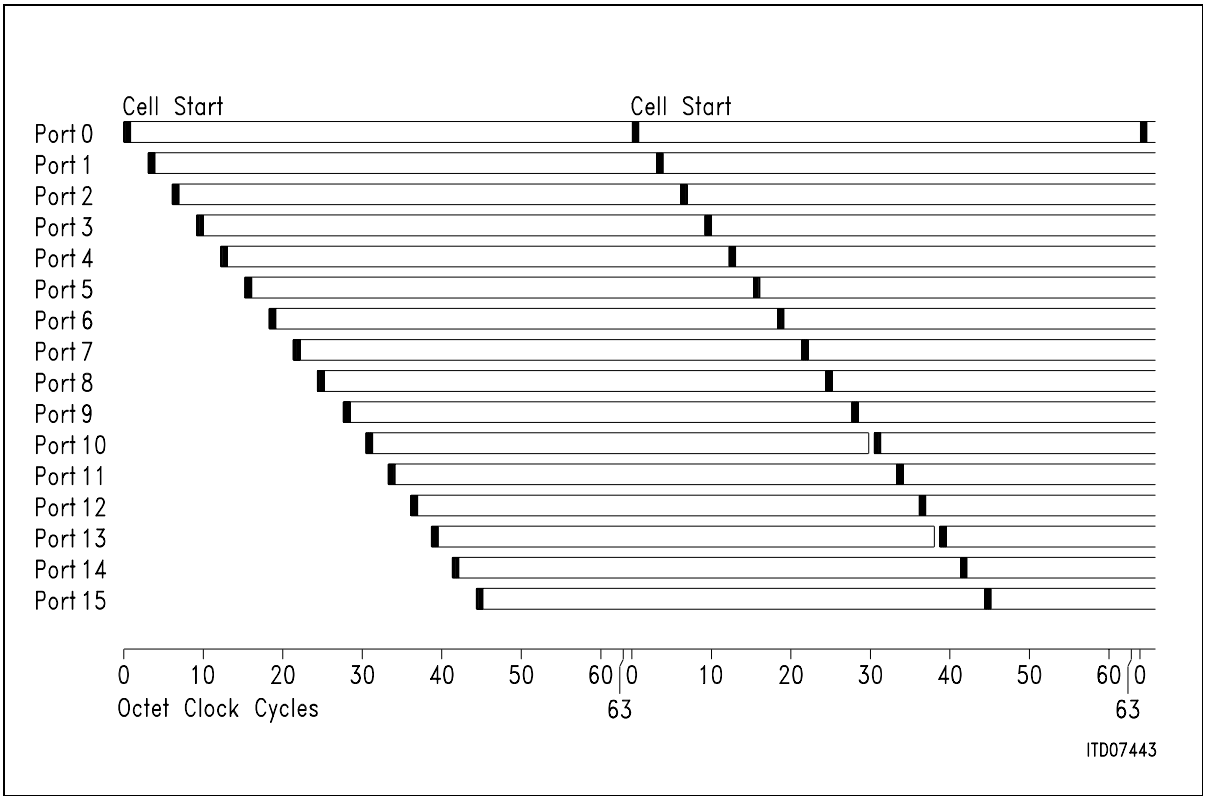


Figure 29 Output Cell Sequence

In the case of port bundling, i.e. a group of ports gets the cells from the same output queue, these staggered output makes it possible for the next ASM to recover the cell sequence.

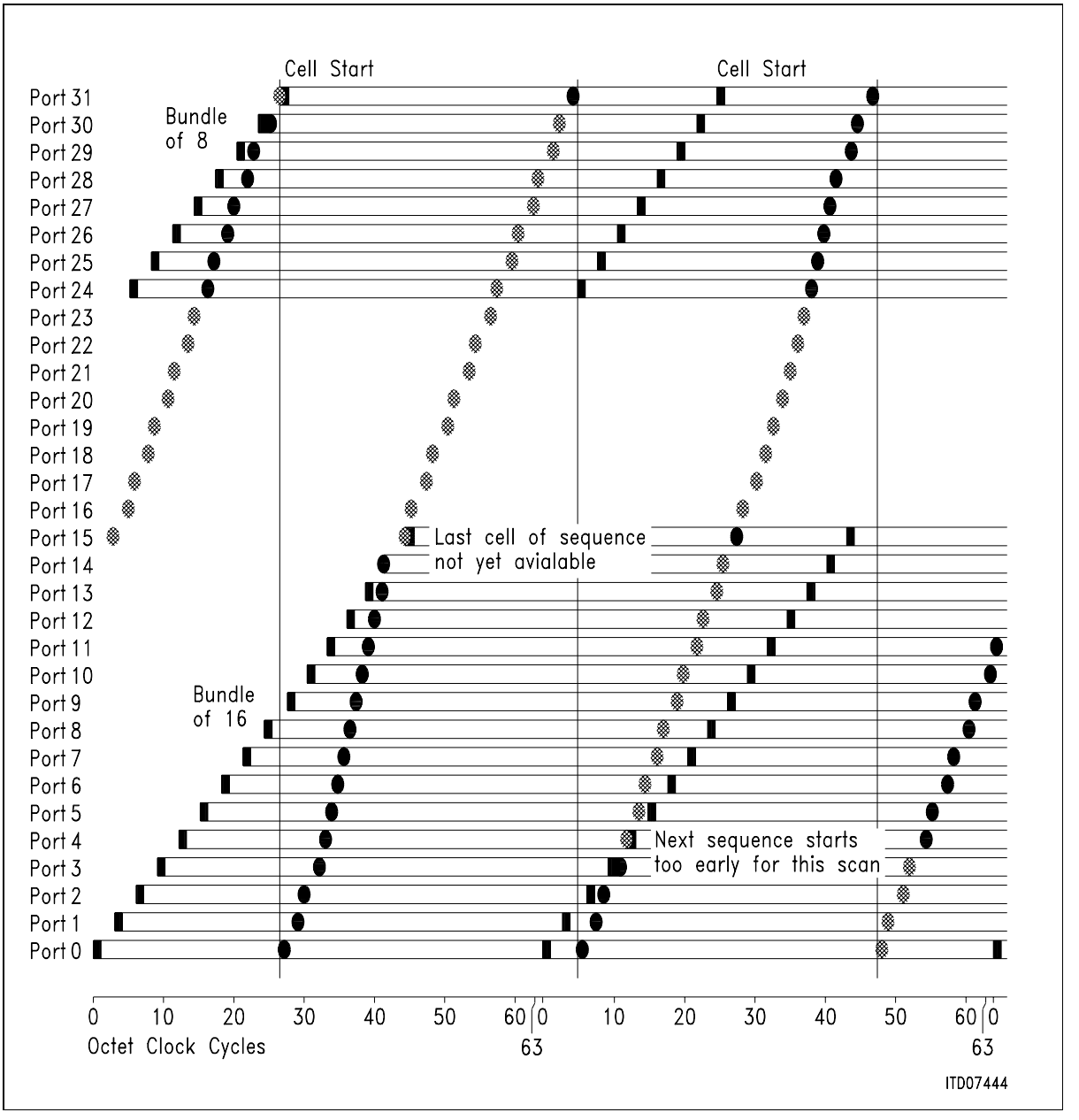


Figure 30 Linear Input Scan

Figure 30 shows this scan while the inputs receive a bundle of 8 and a bundle of 16. It is easy to see that the scan scrambles the sequence of the bundle of 16, because it does not comply with the condition 3. For that reason, another scan algorithm is used if a bundle of 16 is defined via the Mode Register MODR:IG0 or IG1.

The scan algorithm for bundles of 16 works as follows:

- The input ports are partitioned into 2 sections which can possibly receive bundles of 16, i.e. one group contains the ports 0 to 15, the other 16 to 31.

- If the scan crosses an input bundle of 16 (change from ‘cell received’ to ‘no cell available’), the scan leaves the actual section, scans the whole other section, and continues with the port which has ‘no cell available’ before. Such a jump in the sequence is possible only in the second half of the section.
- The possibility to jump is not enabled until one complete section has been scanned and the second section has been started from the beginning.

Note: Pipelining in the implementation can cause that the scan restarts up to 4 ports before that one where it has left the section.

4.9 Routing Evaluation

The Switching Stage Number SSN(3:0) is compared with the Mode Register MODR:SSN(3:0). Cells with matching SSN and if necessary matching routing address are destined for the local processor.

The Housekeeping HK(2:0) is decoded to distinguish Empty Cells <000>, Maintenance Control Cells <011>, Control Cells <110>, and the information ‘other’.

If the Address Identifier ADI(0) is ‘0’, the Routing Address RA(31:0) is compared with the Identification Register IDR:ID(31:0). The result can be masked with the Filter Mask Register FMR:FM(31:0), so that only a part of the Routing Address must be valid to accept a cell. The Output Group Register OGR:OPTR(4:0) defines a four bit section of the Routing Address which contains the destination port number.

When the split mode is activated with MODR:IS(5:0) = n > 0, the cells from the input ports (n – 1) … 0 are handled in a different manner: Only RA(5:4) is compared with ASM_ID(5:4) and without masking, and RA(3:0) is interpreted as destination port number.

If the Address Identifier ADI(0) is ‘1’, a part of the Routing Address RA(15:0), now denoted as MultiCast Identifier MCI(15:0), is used as address for the external Multicast Lookup Table MLT, which delivers the information about the destination port(s).

4.10 Multicast Handling

The Multicast Lookup Table MLT is an external synchronous RAM with 64 k entries. Each entry is 16 bits wide plus an odd parity bit. The bit positions 0 to 15 of an entry denote the output ports 0 to 15, bit 16 is the parity. Since the used external RAM is 18-bit wide, bit 17 remains unused.

The entries can be written via the Multicast Transfer Register MTR and the Multicast Address Register MCA.

A multicast cell normally has more than one destination port. That does not mean that any cell copies are existing in the Central Buffer; each accepted cell is written only once. But the cell location address is copied into the concerned output queues, and so the location will be read repeatedly.

4.11 Output Queue Fairness Management

Queues with an unlimited number of entries have the disadvantage that a burst of cells for one output can fill the whole Central Buffer and therefore can block the traffic for the other queues. For that reason a limit value for each type of queue (single port, bundle of 2, 4, 8, or 16 ports) can be set via the Maximum Queue Length Register MQLR. When the number of entries in a specific queue has reached the limit, this queue will reject all additional cells. This will discard a normal pt-pt cell. A multicast cell must not be discarded, if at least one other destination queue accepts the entry.

4.12 Cell Insertion via the Processor Interface

Two types of local processors may communicate with the processor interface: A microprocessor and a protocol chip. Each has an own address space for one Transmit Cell (TCR1 and TCR2). The processor must not send a Synchronization Octet, but it must append the internal odd parity byte. The Transmit Cell is inserted into the data stream via an internal 33rd input port. This port has no check for a Synchronization Octet, but the complete header evaluation is exercised, so that the cell is treated like a cell from any other port.

4.13 Cell Receiving via the Processor Interface

The ASM has a 17th internal output port with an own output queue, which holds the cells destined for the local processor. The actual cell from this internal port is available in the Receive Cell Register RCR. Two cell types are distinguished: A µP-cell is indicated by an interrupt $\overline{INT0}$, and a communication cell (µP-cell with HK = <110>) activates an interrupt $\overline{INT1}$.

4.14 Procedures for System Failures

Overflows

All types of overflows (buffer-, threshold-, queue-, and µP-queue-overflow) forces that new incoming cells concerned by the overflow are discarded. The different overflow errors are indicated in the interrupt status register ISR.

Line Faults

The incoming cell on each input line of the ASM is checked on SYNC-/ASYNC-state and on parity error of the internal header. If a SYNC-error occurs, the cell is passed through. In case of an ASYNC-error the incoming cells are discarded until the SYNC-status is reached. In case of a parity error only the affected cell is discarded. All errors are indicated in the corresponding registers. Output lines cannot be supervised by the ASM itself. This must be done by the following devices (refer to **Figure 6**).

5 Register Description

The main task of the µP-Interface is to handle all the information which has to be interchanged between the ASM and the external microprocessor such as:

- Error indications — ISR, LASR, LER, LFR
- Input enable and masking instructions — IMR, IOR
- Address information — ILA, OLA/MCA
- µP Commands — COR
- Definition of the thresholds — PTR, MQLR
- Maintenance instructions — MR
- Operation modes — MODR, OGR, IDR, FMR, LPSR
- Cell data: transmission — TCR0, TCR1
  reception — RCR
- Multicast data exchange — MTR

All the data are exchanged in a bytewise operation.

Note: The access to the µP-registers can only be done with a permanently running operating clock.
The loss of the operating clock cuts off any access capability.

In all the register operations the µP acts as the master device; this implies the absolute access priority to the µP-Interface whenever it is necessary (asynchronous operation).

5.1 Registers Table

The following section will give an introduction to the register functions. Additional marks are given for certain functions like hardware reset or default values.

5.1.1 Interrupt Status Register (Read Only)

	7							0	
ISR	ASYNC	SYNCE	PE	CTRLE	IPE	MLTPE	MCMR	PCRCV	00_H
	0	0	0	0	BOV	TOV	QOV	PQOV	01_H

Hardware reset value all 0

Software reset value (no change)

The Interrupt Status Register ISR displays all events which can cause an interrupt $\overline{INT0}$ to the µP. If an event sets a bit in the ISR to '1', it remains in that state until the µP resets the flag. At the same time, an interrupt $\overline{INT0}$ is activated if the bit is not masked in the Interrupt Mask Register IMR and the interrupt is not already active.
The µP read operation onto the ISR (00_H, 01_H) has no influence to the register. This means that every time the µP reads the register, it gets the present status of the ISR:A µP write access onto ISR (00_H, 01_H) with the relevant bit set to '1' clears the interrupt status bit. A write of '0' has no influence to an interrupt status bit. If the interrupt line $\overline{INT0}$ has been active, the reset of the ISR flags force also the deactivation of the interrupt line.
Events that occur during the 'clear bit' access of the µP are not lost due to an internal shadow register which is not accessible for the µP. These events are passed through to the ISR after the µP write access is finished.
Since in the reset phase all lines have been asynchronous for a time, ASYNC will be '1' and the µP should at first write the corresponding flag to '1' to reset it.

ASYNC Asynchronous State

A line is defined to be asynchronous, when two invalid Synchronization Octets are detected successively. In that situation ASYNC is set if the very line is not masked in the Input On-line Register IOR. So ASYNC indicates that one or more non-masked lines are asynchronous. The concerned input lines can be read from the Line Asynchronous State Register LASR. During the ASYNC-state of an input line incoming cells are discarded.

SYNCE Synchronization Error

Has the same function as ASYNC, but it is set if only one invalid Synchronization Octet is detected and the next Synchronization Octet is correct. So if a Synchronization Octet is corrupted, either SYNCE or ASYNC is set. A SYNC-error on a line is only set if the very line is not masked in the Input Online Register IOR.
Cells with invalid Synchronization Octet causing an SYNC-error are passed through. The concerned input lines can be read from the Line Asynchronous State Register LASR. For test purposes, sync. errors can be generated by MR:IVSYNC = 1 of the previous ASM.

PE Parity Error

Result of the internal cell header parity check of all input ports. All incoming cells are checked for correct parity bit P within the internal cell header.
PE = 1 indicates that a parity bit on at least one of the active input lines was found to be invalid. The cells with a parity error are discarded without further evaluation.
The parity checks are only done for lines which are not in the asynchronous state; results from asynchronous lines are masked out.
A parity error on a line is only set if the very line is not masked in the Input Online Register IOR.

CTRLE Control Error

CTRLE indicates an internal hardware error in the address administration. The 300 addresses pointing to all entries of the Central Buffer are permanently exchanged between the Free Cell List RAM (FCL) and one or more output queues in the common Queue RAM. The readout count is stored in the Multicast Count RAM (MCC). All entries in these three RAMs are protected by an additional parity bit. Every stated error is mapped as a Control Error CTRLE.
When a parity error in a Queue RAM occurs, the corresponding address will be erased; this means that the entry under this address in the Central Buffer allocated to this queue is lost. Since the address is not returned into the Free Cell List, the number of available addresses decreases. If the RAM has a permanent failure, after a short time no addresses will be left, resulting in a Buffer Overflow BOV.
For test purposes a Control Error can be generated by setting INVM, INVQ, or INVP in the Maintenance Register MR.

IPE Internal Parity Error

Indicates a parity error of the internal cell parity octet. That means that the cell has been corrupted in the path between S/P converter, Central Buffer, and P/S converter.
For test purposes an IPE can be generated via appropriate test cells.

MLTPE Multicast Lookup Table Parity Error

Indicates a parity error in the external Multicast Lookup Table (MLT) RAM.

MCMR Multicast Misrouting

MCMR indicates that a multicast cell is detected which is not destined for the ASM, i.e. the multicast operation is disabled in the command register (DCMC = 1), so that the control logic does not support multicast. The multicast cell will be discarded.

PCRCV µP-Cell in Receive Buffer

Indicates that a µP-cell is available in the receive buffer for readout. When the ASM sets PCRCV = 1, the RX-bit in the command register COR is activated at the same time. After reading both bytes of ISR, PCRCV is cleared to 0 automatically. The RX must be cleared independent from PCRCV by the µP. The RX-bit can be cleared by reading out of the last cell octet or by overwriting the RX-bit with the µP. After that the ASM will move the next cell (if available) into the receive buffer and the whole process starts again.

BOV Buffer Overflow

Indicates that a cell has been discarded because no free cell entry is available. In practice, it means that 296 to 300 cells are stored in the Central Buffer. The uncertainty is due to the fact that free entry addresses have some clock cycles delay before they can be used again.

Note: A Control Error CTRLE (see above) may have decreased the number of available cell entries.

TOV Threshold Overflow

Indicates that the number of cells in the Central Buffer exceeds (or has exceeded for a time) the limit defined in the Priority Threshold Register PTR. In the Threshold Overflow condition all incoming low-priority cells (with bit CLP = 1 in the external cell header) are discarded.

QOV Queue Overflow

Indicates that a cell has been discarded because no free queue entry is available in the corresponding output queue. The common limit for each type of output queue, except of the µP-queue, is defined in the Maximum Queue Length Register MQL.

PQOV Microprocessor Queue Overflow

Indicates that an incoming µP/communication cell has been discarded, because the number of stored µP/communication cells has reached the limit value for the Maximum Processor Queue Length Register PQLR.

5.1.2 Interrupt Mask Register (Write)

	7							0	
IMR	MASYNC	MSYNCE	MPE	MCTRLE	MIPE	MMLTPE	MMCMR	0	02_H
	0	0	0	0	MBOV	MTOV	MQOV	MPQOV	03_H

Hardware reset value all 1

Software reset value (no change)

Readable for test purposes.

The Interrupt Status Register ISR can be masked by the IMR, by setting the corresponding bit(s) of IMR to 1. That means that only the interrupt for the masked ISR-bit is deactivated. The actual status of the ISR-bit can be read by the µP independent from the mask register.
Attention: The PCRCV-bit can not be masked, to prevent the blocking of the µP-queue for communication cells because of not processed cells by the µP.

5.1.3 Line Asynchronous State Register (Read Only)

	7							0	
LASR	7							0	04_H
	15							8	05_H
	24							16	06_H
	31							25	07_H

Hardware reset value undefined, see below

Software reset value (no change)

Bit i of LASR is assigned to the ASM-input line number i (0 i 31).
A line is defined to be asynchronous, when two invalid Synchronization Octets are detected successively. An input line is marked as asynchronous by setting the line-individual ASYNC bit in LASR. In addition the subsequent parity error indication of the internal header is masked.
During the ASYNC-state of an input line incoming cells are discarded.
The content of the Input Online Register IOR has no influence for LASR.
The LASR indicates the actual status of all input lines, i.e. the register is actualized continuously by the ASM. Every time the µP reads the register, it gets the present status of the input lines.

5.1.4 Input Line Address (Write)

	7	4	0	
ILA	unused	ILA(4:0)		08_H

Hardware reset value all 0

Software reset value (no change)

Readable for test purposes.

ILA defines the input line whose state can be observed in LASYNC, LSYNCE, and LPE in the Line Error Register LER. Value Range 0 to 31.

Note: A change of ILA does not change the values of LER automatically. LER still shows the state of the old ILA adjustment. Therefore after a change the µP *should first read LSR to reset it.*

5.1.5 Line Error Register (Read Only)

	7				3				0	
LER	unused				LSE	LASYN	LSYNC	LPE		09_H

Hardware reset value undefined

Software reset value (no change)

The µP read operation resets the accessed byte to all 0.

LSE Line Sample Error

Indicates too much jitter in the alignment unit of the input specified in the Input Line Address Register ILA.

LASYN Line Asynchronous State

Shows the state of the line specified in the Input Line Address Register ILA. The line is defined to be asynchronous (LASYNC = 1), when two invalid Synchronization Octets are detected successively. The content of the Input Online Register IOR has no influence for LASYNC.

LSYNC Line Synchronization Error

Has the same function as LASYNC, but it is set (LSYNC = 1) if only one invalid Synchronization Octet is detected and the next Synchronization Octet is correct. So if a Synchronization Octet is corrupted, either LSYNC or LASYNC is set. If LSYNC=1 and LASYN=0 the data transfer on the respective input is undisturbed.

LPE Line Parity Error

Result of the parity check of the line, specified in the Input Line Address Register ILA. All incoming cells are checked for correct internal header parity bit P in the internal cell header. LPE = 1 indicates that a parity error was found on that line. This check is only evaluated if the line is in the synchronous state.

5.1.6 Line Failed Register (Read Only)

	7							0	
LFR	7							0	$0A_H$
	15							8	$0B_H$
	23							16	$0C_H$
	31							24	$0D_H$
	unused							32	$0E_H$

Hardware reset value undefined, see below

Software reset value (no change)

The µP read operation resets the accessed byte to all 0.
Bit i of the LFR represents the state of the input line i. If either a Synchronization Error, Asynchronous Line State, or Parity Error is detected, the failure is indicated at the appropriate bit position. If IOR disables a line, parity errors from this line are also masked.
Since in the reset phase all lines have been asynchronous for a time, LFR will be ‘all 1’ and the µP should at first read all bytes of LFR to reset it.
Bit 32 is used for the ASM internal µP input port indicates only parity bit errors.

Note: Events PE, SYNCE, ASYNC that occur during read of LFR may cause loss of information as the line information is reset before the interrupt procedure is able to process the new error.

5.1.7 Input Online Register (Write)

	7							0	
IOR	7							0	$0F_H$
	15							8	10_H
	23							16	11_H
	31							24	12_H

Hardware reset value all 1

Software reset value (no change)

Readable for test purposes.

Bit i of the Input Online Register IOR defines the state of the input line i. Bit i = 1 forces line i to the online state. Bit i = 0 switches the input offline, i.e. all cells from this line are discarded and all errors are masked within the Interrupt Status Register ISR and have no influence to PE, ASYNC, and SYNCE. However, the status can be observed in the LASR, LFR and LER (only SYNC/ASYNC-state).

5.1.8 Command Register (Read/Write)

	7							0	
COR	$\overline{RX}$	TX1	TX0	LPSC	WMLT	RMLT	MCINI	SRES	13_H

Hardware reset value all 0 except $\overline{RX}$=1

Software reset value (no change)

The required operation is initialized by writing a 1 to the corresponding command bit. After the operation has been completed, the ASM resets that bit to 0.

Note: $\overline{RX}$ has a different function: It is set by the ASM and reset by the µP or by the ASM.

The ASM needs 76 octet clocks at maximum to insert a communication/test cell from the transmit buffer into the data stream and therefore to clear TX1/ TX0 and to accept new cells.

$\overline{RX}$ Receive µP/Communication Cell

Indicates that a µP/communication cell is available in the receive buffer for readout. When the ASM sets $\overline{RX}$, the following actions are done depending on the configuration of the ASM and the HK-bits in the internal header of the cell:

1. HK<2:0> of the cell header = 001
   PCRCV in the Interrupt Status Register ISR is set to 1, so that ASM activates the interrupt line $\overline{INT0}$
2. HK<2:0> of the cell header = 001 and MODR:EINT1 = 0
   PCRCV in the Interrupt Status Register ISR is set to 1, so that ASM activates the interrupt line $\overline{INT0}$
3. HK<2:0> of the cell header = 011 and MODR:EINT1 = 1
   ASM activates the interrupt line $\overline{INT1}$

With the readout of the last cell octet, $\overline{RX}$ is cleared automatically. After uncompleted cell readout, $\overline{RX}$ must be cleared by the µP. After that the ASM will move the next cell (if available) into the receive buffer and the whole process starts again.

Note: A read access to the Receive Cell Register RCR is only possible if $\overline{RX}$=0, otherwise the data is invalid.

TX1 Transmit Communication Cell

The command TX1 = 1 forces the ASM to copy the communication cell from the transmit buffer TCR1 into the Central Buffer, i.e. to insert it into the data path. With the write operation of the last cell octet in TCR1 the bit TX1 is set automatically. When this operation is performed and the transmit buffer is available for the next communication cell, TX1 is cleared.
The ASM needs 76 octet clocks at maximum to insert a communication cell from the transmit buffer into the data stream. During that time no further cell can be inserted.

TX0 Transmit µP-Cell

The command TX0 = 1 forces the ASM to copy a µP-cell from the transmit buffer TCR0 into the Central Buffer, i.e. to insert it into the data path. With the write operation of the last cell octet in TCR0 the bit TX0 is set automatically. When this operation is performed and the transmit buffer is available for the next µP-cell, TX0 is cleared.
The ASM needs 76 octet clocks at maximum to insert a µP-cell from the transmit buffer into the data stream. During that time no further cell can be inserted.

LPSC LIC Protection Switch Change

This command (LRSC = 1) forces the ASM to accept the adjustments made in LIC Protection Switch Register LPSR. Previously the data has to be written into the LPSR.
The release of the LPSR forces additionally the output of one Protection Switch Identifier cell (PSI-cell) on every output port, whose configuration has been changed.
After the operation is done, the ASM clears LPSC to 0.

WMLT Write Multicast Lookup Table (MC-RAM)

Write command bit (WMLT = 1), requesting a write access to the MC-RAM. Previously the address has to be written into the Multicast Address Register MCA, and the appropriate data into the Multicast Transfer Register MTR. When the operation is done, the ASM clears WMLT to 0. That may not be immediately, because the ASM must wait for a cycle where the MLT is not in use.

RMLT Read Multicast Lookup Table (MC-RAM)

Read command bit (RMLT = 1), requesting a read access to the MC-RAM. Previously the address has to be written into the Multicast Address Register MCA.
When the data is available in the Multicast Transfer Register MTR, the ASM clears RMLT to 0. That may not be immediately, because the ASM must wait for a cycle where the MLT is not in use.

MCINI Multicast RAM Initialization

This command (MCINI = 1) forces the ASM to initialize the whole external Multicast Lookup Table RAM (MC-RAM) with 0. When the operation is done, the ASM clears MCINI.

Note: After HW-reset the connected Multicast RAM is not initialized.

SRES Software Reset

The Software Reset (SRES = 1) initializes the Free Cell List, Multicast Count RAM, Output Queue RAMs, and the Operation and Maintenance Register. In contrast to the Hardware Reset all other registers, especially the Multicast Lookup Table or the input/output cell synchronism, remain unchanged. After this initialization is done, SRES is cleared (SRES = 0).

5.1.9 Priority Threshold Register (Write)

	7							0	
PTR	PTR(7:0)								14_H

Hardware reset value $255_D = FF_H$ threshold value = 2 × PTR = 510 (no threshold)

Software reset value (no change)

Readable for test purposes.

The Priority Threshold defines a limit for the acceptance of low-priority cells. Low-priority cells are defined by an external cell header with bit CLP = 1. As long as the number of cells stored in the Central Buffer exceeds the threshold value, low-priority cells from the inputs are rejected. The threshold value used for the comparison in the ASM results in the multiplication of the Priority Threshold Register value by 2. So it is possible to define only even threshold values. Values over 300_D (PTR = 150_D) exceed the Central Buffer capability and therefore define no limit.

5.1.10 Maximum Queue Length Register (Write)

	7	0	
MQLR	MQL1(7:0)		15_H
	MQL2(7:0)		16_H
	MQL4(7:0)		17_H
	MQL8(7:0)		18_H

Hardware reset value

MQLx(7:0) = 255_D = FF_H queue length = 2 × MQLx = 510 (no threshold)
x = 1, 2, 4, 8

Software reset value (no change)

Readable for test purposes.

The Maximum Queue Length MQL defines a queue length limit for each type of output queue. MQL1(7:0) defines the queue limit for bundles of 1, MQL2(7:0) the queue limit for bundles of 2, MQL4(7:0) for bundles of 4 and MQL8(7:0) for bundles of 8 and 16. If the number of cell locations stored in a queue exceeds the threshold value, a QOV-error is indicated and the cell is not stored in this queue. The threshold value used for the comparison in the ASM results in the multiplication of the Maximum Queue Length value by 2. So it is possible to define only even threshold values.
The following values define the maximum limits for the various bundle sizes. All values exceeding the maximum queue length are limited to the maximum value.

MQL1(7:0) = 44_D = $2C_H$ = max. queue length from 88_D
MQL2(7:0) = 88_D = 58_H = max. queue length from 176_D
MQL4(7:0) = 150_D = 96_H = max. queue length from 300_D
MQL8(7:0) = 150_D = 96_H = max. queue length from 300_D
Queue length values over 88_D for bundles of 1 and 176_D for bundles of 2 exceeds the capacity of the output queues. The queue length value over 300_D for bundles of 4, 8 and 16 exceeds the Central Buffer capability and therefore define no limit.

Note: MQL may be changed to smaller limits only if the actual amount of queue entries is smaller than the new limit to prevent malfunctions.

Note: MQL is not valid for the µP-queue to define a limit (see PQLR).

5.1.11 Processor Queue Length Register (Read/Write)

	7	0	
PQLR	PQLR(7:0)		19_H

Hardware reset value $255_D = FF_H$

Software reset value (no change)

The Processor Queue Length Register defines a limit for the acceptance of the output µP queue. If the number of µP cells stored in the Central Buffer exceeds the threshold value, subsequent µP cells are discarded and PQOV in the Interrupt Status Register is set.
The threshold value used for the comparison by the ASM results in the multiplication of PQLR(7:0) by 2. Thus only even thresholds can be set. Thresholds beyond 304_D (PQLR(7:0)=152_D) exceed the Central Buffer Capacity and therefore define no limit.

Note: If the threshold is changed during the overflow of this queue the new limit will come into effect after transfer of one cell into the data stream.

5.1.12 Multicast Transfer Register (Read/Write)

	7	0	
MTR	Data(7:0)		$1A_H$
	Data(15:8)		$1B_H$

Hardware reset value all 0

Software reset value (no change)

The MTR is a data register for the Multicast Lookup Table (MLT) RAM read/ write-access. The RAM address is defined in the Multicast Address Register (MCA). Read or write access is started with RMLT or WMLT in the Command Register COR. If both are set, the read access has priority over the write access.

Read Access to MLT

- Write MLT address to MCA ($1A_H/1B_H$).
- Set RMLT = 1 in the Command Register COR (12_H, bit 2).
- Wait for RMLT = 0.
- Read data from MTR.

Write Access to MLT

- Write MLT address to MCA ($1A_H$/$1B_H$).
- Write data to MTR (18_H, 19_H).
- Set WMLT = 1 in the Command Register COR (12_H, bit 3).
- Operation is performed when WMLT = 0.

5.1.13 Output Line Address/ Multicast Address Register (Write)

	7	0	
OLA/MCA	MCA(7:0) or OLA(3:0)		$1C_H$
	MCA(15:8)		$1D_H$

Hardware reset value all 0

Software reset value (no change)

Readable for test purposes.

Usage 1: OLA(3:0) defines the output line to be provided with an invalid Synchronization Octet by setting IVSYNC in the Command Register COR. Used for test purposes. Value range is 0 to 15. Output grouping does not influence the function.

Usage 2: MCA(15:0) defines the RAM address to be used for µP read/write access to the Multicast Lookup Table (MLT). The data to be transferred will be placed into the Multicast Transfer Register MTR.

5.1.14 Maintenance Register (Write)

	7							0	
MR	0	IVINP	IVSYNC	IVMLTP	IVMCCP	IVQRP	IVFCP	DPQ	$1E_H$
	0	0	0	DPA	DOS	SWPQ	AANIC	AAC	$1F_H$
	0	0	0	0	STCO(3:0)				20_H
	0	0	0	0	STFO(3:0)				21_H

Hardware reset value all 0

Software reset value address $1E_H$, bit (5 … 1) = 0

other no change

Readable for test purposes.

IVINP Invalidate Input Ports

This function (IVINP = 1) permits the test of the asynchronous line state detection. It falsifies the comparison values for the synchronization octet of all inputs as long as IVINP is set. For the test IVINP must be set for at least 128 octet clocks.

IVSYNC Invalidate Sync Octet

This function (IVSYNC = 1) permits the test of the synchronization error detection in the input unit of a subsequent ASM or ASP chip. It corrupts the toggle bit T in the synchronization octet ‘T110 1000’. The output line which shall be provided with this invalid synchronization octet is specified in the Output Line Address register OLA(3:0). After one synchronization octet was corrupted, IVSYNC is cleared (IVSYNC = 0) by the ASM.

IVMLTP Invalidate Multicast Lookup Table Parity

Device test function: When IVMLTP = 1, the parity bit of the Multicast Lookup Table is inverted, causing a Multicast Lookup Table Parity Error MLTPE in the Interrupt Status Register ISR. After one parity bit was corrupted, IVMCCP is cleared (IVMCCP = 0) by the ASM.

IVMCCP Invalidate Multicast Count Parity

Device test function: When IVMCCP = 1, the parity bit of the Multicast Count RAM is inverted, causing a Control Error in the Interrupt Status Register ISR. After one parity bit was corrupted, IVMCCP is cleared (IVMCCP = 0) by the ASM.

IVQRP Invalidate Queue RAM Parity

Device test function: When INVQ = 1, the parity bit of the parity checker observing the Output Queue RAM bus is inverted, causing an immediate Control Error CTRLE in the Interrupt Status Register ISR. After one parity bit was corrupted, IVQRP is cleared (IVQRP = 0) by the ASM.

IVFCP Invalidate Free Cells List Parity

Device test function: When INVP = 1, the parity bit of one Free Cell List input is inverted, causing a Control Error CTRLE in the Interrupt Status Register ISR after the invalidated address has traversed the Free Cell List FIFO. This test function works only with data cells at the ASM inputs, not with empty cells. After one parity bit was corrupted, IVFCP is cleared (IVFCP = 0) by the ASM.

DPQ Disable Readout of µP-Queue

Device test function: When DPQ = 1, the readout of the µP-queue entries is disabled; no interrupt is generated. Used to test the Processor Queue Overflow PQOV in the Interrupt Status Register ISR.

DPA Disable Phase Alignment

Device test function: When DPA = 1, the phase alignment unit works with a fixed clock phase and therefore in a synchronous manner.

DOS Disable Overscan

Device test function: When DOS = 1, the input scan is set to a fixed relation to the output scan. The scan sequence is <output0, input0, input1, output1, input2, input3, …, output15, input30, input31, µP output, none, none, µP-input, 12 × none>.

SWPQ Switch all Accepted Cells to the µP-Queue

Device test function: When SWPQ = 1, the cell destination unit is disabled. All incoming cells are handled according to the initialized operation mode. If the cell is accepted by the cell acceptance unit, the cell is routed to the µP-queue independent from any specified output port.
This function can be combined with the AAC- or AANIC-bit.

AANIC Accept all non Empty Cells

Device test function: When AANIC = 1, all incoming data with correct synchronization octet from every activated port except of empty cells will be accepted. These cells will be routed according to the initialized operation mode or to the µP output queue specified by the RPQ-bit. The AANIC-bit will be disabled by the AAC-bit.

AAC Accept all Cells

Device test function: When AAC = 1, the cell acceptance unit is disabled. All incoming cells with correct synchronization octet from every port will be routed according to the initialized operation mode or to the µP output queue if specified by SWPQ. The enabled AAC-bit disables AANIC-bit.

STCO(3:0) Select Test Control Output

Device debugging function only: Reset value should not be changed in normal operation.

STFO(3:0) Test Output Select

Device debugging function: Reset value should not be changed in normal operation.

5.1.15 Phase Align Test Register (Read)

	7	0	
PATR	PATR(7:0)		22_H

Hardware reset value undefined
Software reset value (no change)

Device test function only. Shows the current edge distribution of the input specified by the Input Line Address Register ILA.

5.1.16 Free Cells Count Register (Read/Write)

	7	0	
FCNT	FCNT(7:0)		23_H

Hardware reset value $1001\ 1000_B = 152_D = 98_H$
Software reset value (no change)

FCNT can be used for statistical purposes. It has to be multiplied by 2 to obtain the number of free cells in the Central Buffer. The smallest number since the last read of FCNT is stored. After a read access the register is loaded with the reset value 152_D.

5.1.17 Version Code Register (Read)

	7	0	
VERCR	VERC(7:0)		24_H
	VERC(15:8)		25_H
	VERC(23:16)		26_H
	VERC(31:24)		27_H

Hardware reset value address $24_H = 2F_H$
address $25_H = D0_H$
address $26_H = 0B_H$
address $27_H = 0B_H$

Software reset value (no change)

VERC(31:0) Version Code

The version code of the ASM is identically to the boundary scan identity code register and can be read out via the µP-interface. The version code register contains information about manufacturer, ASIC number and version number.

The structure of the version code register is :

Bit 31 … 28	Bit 27 … 12	Bit 11 … 1	Bit 0
Version number	ASIC number	Manufacturer number	1
0000	1011 0000 1011 1101	0000 0010 111	1

5.1.18 Mode Register (Write)

	7							0	
MODR	0	0	IG1	IG0	SSN(3:0)				28_H
	0	AOPC	IS(5:0)						29_H
	0	0	EVMCP	DCMC	EVMCI	EVMCM	ACCEL	APCEL	$2A_H$

Hardware reset value address 28_H = all 0 except of SSN(3:0) = 0001
address 29_H = all 0
address $2A_H$ = all 1 except ACCEL = 0

Software reset value (no change)

Readable for test purposes.

IG1 Input Grouping 1

IG1 = 1 forces the input scan unit to handle the inputs 16 to 31 as a bundle; that means that the cell sequence within the bundle remains unchanged.

IG0 Input Grouping 0

IG0 = 1 forces the input scan unit to handle the inputs 0 to 15 as a bundle; that means that the cell sequence within the bundle remains unchanged.

SSN(3:0) Switch Level Stage Number

SSN allows to mark every ASM in a funnel structure with a specific identification, making it possible to send a µP/communication cell to one specific ASM (see **Figure 33**).
µP/communication cells are accepted only if SSN(3:0) and the routing address is equal to the SSN and the valid routing address in the internal cell header.
The address comparison is done using the Filter Mask register FMR.

AOPC Accept Only Microprocessor Cells

When AOPC = 1, the cell acceptance unit accepts only microprocessor cells identified by the correct switching stage number SSN and by the valid routing address (depends on the operation mode of the ASM). All other incoming cells are discarded.

IS(5:0) Input Select for Split Operation Mode (NORMAL/SPLIT-mode)

Defines the threshold for normal and split mode handling of the inputs:

32_D … 63_D	Fixed routing evaluation for all inputs: RA(3:0) defines the output
0	Normal routing evaluation for all inputs (default): Position of routing bits determined by OPTR(4:0)
n (32 > n > 0)	Split mode: Normal routing evaluation for inputs 31 … n, fixed routing evaluation for inputs (n – 1) … 0

EVMCP Evaluate Multicast Parity

As long as EVMCP = 1 the control logic is able to evaluate the parity bit in the Multicast Look-up Table (MC-RAM). If a multicast look-up table parity error MLTPE occurs this error is indicated in ISR:MLTPE. In case of EVMCP = 0 the parity evaluation of the ASM is disabled. Then a 16-bit wide MC-RAM can be connected to the ASM (e.g. 64 k × 16 bit).

DCMC Discard Multicast

As long as DCMC = 1, the control logic does not support multicast header types. All multicast cells will be discarded and the MCMR-flag in the Interrupt Status Register ISR will be set. DCMC can only be changed by the µP or with a Hardware Reset. The DCMC-bit is independent from the value of EVMCI, i.e. the evaluation of the DCMC-bit is done in the ASM previous to the EVMCI evaluation.

EVMCI Evaluate Multicast Identifier

As long as EVMCI = 1 the control logic is able to identify incoming multicast cells by the ADI(0) = 1 in the internal routing header. In case of EVMCI = 0, the ADI(0) bit is masked by the ASM. Thus, the ASM treats incoming multicast cell as self-routing cells. The evaluation of EVMCI can only be done if DCMC = 0 (see above).

EVMCM Evaluate Multicast Identifier for Split Mode

This bit is identical to the EVMCI bit described above, except that it applies to the special inputs with fixed routing evaluation in split mode. The other, normal inputs of the split mode operation mode are controlled by the EVMCI bit. As long as EVMCM = 1 the control logic is able to identify incoming multicast cells by ADI(0) = 1 in the internal routing header. In case of EVMCI = 0 the cells are treated as self-routing cells.

ACCEL Accept Control Cells

APCEL Accept µP-Cells

These two bits control the acceptance of µP and control cells and which interrupt line is activated at the reception of these cells. Control cells are cells destined to the receive buffer of the ASM (i.e. they have matching SSN and the routing address RA(31:0) matches the ID(31:0) after masking by FMR(31:0)) and the housekeeping field in the cell header has the value HK = 110. µP-cells denote cells which are destined to the receive buffer of the ASM but have any other housekeeping value.

Table 4 µP/Control Cell Handling

ACCEL	APCEL	HK	Comment
0	0	Don't care	µP and control cells are discarded, no interrupts are activated.
0	1	HK ≠ 110	µP-cells activate $\overline{INT0}$.
0	1	HK = 110	Control cells activate $\overline{INT0}$.
1	0	HK ≠ 110	µP-cells are discarded.
1	0	HK = 110	Control cells activate $\overline{INT1}$.
1	1	HK ≠ 110	µP-cells activate $\overline{INT0}$.
1	1	HK = 110	Control cells activate $\overline{INT1}$.

5.1.19 Output Group Register (Write)

OGR

7				0	
OPE(7:0)					$2B_H$
OPE(15:8)					$2C_H$
OG(7:0)					$2D_H$
CBC	OG(14:8)				$2E_H$
0	0	0	OPTR(4:0)		$2F_H$

Hardware reset value all 0

Software reset value (no change)

Readable for test purposes.

OPE(15:0) Output Port Enable

OPE enables the output port i belonging to the bit position i in the register. The output ports are enabled/disabled independent from any output group. An overflow of the corresponding output queue can be reached by disable of all belonging output ports. Further incoming cells are discarded because of the queue overflow. OPE(15:0) = all 0 can be used to test the Buffer Overflow BOV in the Interrupt Status Register ISR.

CBC Change Bundle Configuration

This command (CBC = 1) forces the ASM to disable the inputs of the output queue which shall be changed. Thus, all affected output queues run empty. After that, the new configuration is taken over by the ASM, the inputs of the output queues are reactivated and CBC is cleared by the ASM (CBC = 0).

OG(14:0) Output Grouping

OG enables grouping of adjacent outputs with one commonly used output queue per group.

All 0 No output grouping (default)

Bundle of 2 ports:

OG(0) = 1 Grouping of output ports (1:0)

OG(1) = 1 Grouping of output ports (3:2)

⋮

OG(7) = 1 Grouping of output ports (15:14)

Bundle of 4 ports:

OG(8) = 1 Grouping of output ports (3:0)

OG(9) = 1 Grouping of output ports (7:4)

⋮

OG(11) = 1 Grouping of output ports (15:12)

Bundle of 8 ports:

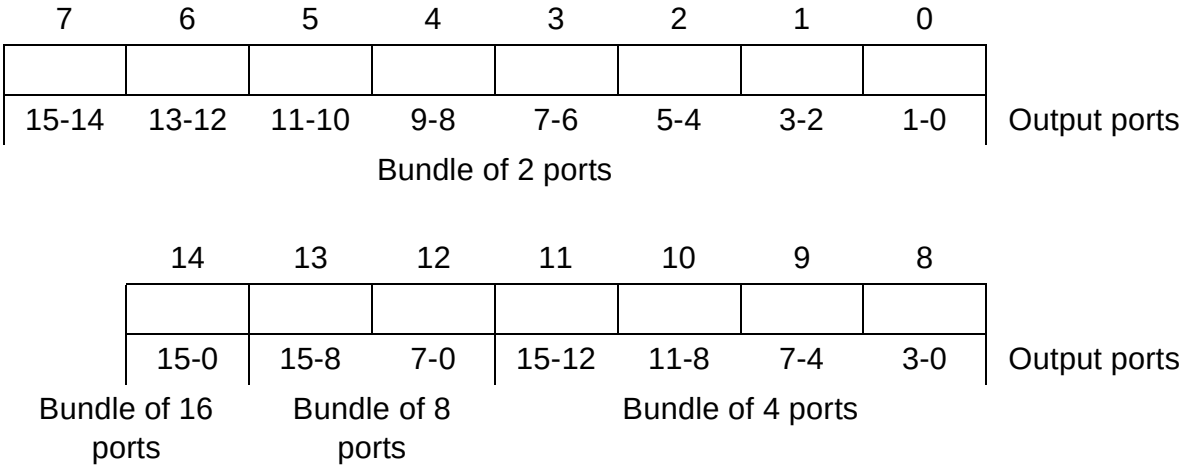
OG(12) = 1 Grouping of output ports (7:0)

OG(13) = 1 Grouping of output ports (15:8)

Bundle of 16 ports:

OG(14) = 1 Grouping of output ports (15:0)

Bits set for a higher bundle overwrites all affected bits of lower bundles, e.g. the bit OG(12) = 1 overwrites automatically the bits OG(9:8) and OG(3:0).



For the following examples the nomenclature is:

1 = n-bundle enabled (n = 2, 4, 8 or 16)

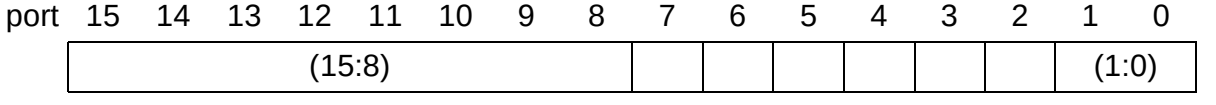
0 = n-bundle disabled (n = 2, 4, 8 or 16)

x = don't care, i.e. these bits can set to '1' but the setting has no effect on enabling bundles, as the corresponding output ports are meanwhile used by present enabled bundle(s) which are higher bundles (e.g. example 1 below : OG(11) is don't care because this 4-bundle uses the output ports 15-12 which are already used by the 8-bundle; a 8-bundle is a higher bundle than a 4-bundle)

Example 1 :

Setting of OG(14:0): 010 xx00 xxxx 0001

Table 5 Grouping of the Output Ports Corresponding to Content of OG(14:0)



(15:8): 8-bundle of output ports 15-8 due to '1' of OG(13)

(1:0): 2-bundle of output ports 1 and 0 due to '1' of OG(0)

Example 2 :

Setting of OG(14:0): 000 0010 1000 xx00

Table 6 Grouping of the Output Ports Corresponding to Content of OG(14:0)

port	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	(15:14)								(7:4)							

(15:14): 2-bundle of output ports 15 and 14 due to ’1’ of OG(7)

(7:4): 4-bundle of output ports 7-4 due to ’1’ of OG(9)

Example 3 :

Setting of OG(14:0): 1xx xxxx xxxx xxxx

Table 7 Grouping of the Output Ports Corresponding to Content of OG(14:0)

port	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	(15:0)															

(15:0): 16-bundle of output ports 15-0 due to ’1’ of OG(14)

OPTR(4:0) Output Pointer

OPN(4:0) defines a four bit output port window within the 32-bit routing address of the internal cell. The value range is 0 … 28_D. Values from 29 … 31_D are not allowed.
The pointer indicates the least significant bit of the four bit word. Cells are routed to the output port decoded out of the four bits. If the output port belongs to an output group defined in OPG(14:0), the cells are routed to this output group.

5.1.20 Identification Register (Write)

	7							0	
IDR	ID(7:0)								30_H
	ID(15:8)								31_H
	ID(23:16)								32_H
	ID(31:24)								33_H

Hardware reset value all 0

Software reset value (no change)

Readable for test purposes.

ID(31:0) ASM IDentification

ID(31:0) is used to distinguish between different ASMs connected to the same inputs sources.
Cells are accepted if the valid bits within ID(31:0) are equal to the valid routing address bits RA(31:0) in the cell header. The valid bits are defined by the filter mask register FM(31:0) (see below).
In case of multicast, the higher word of the Identification Register ID(31:16) can be used for evaluation of the routing address RA(31:16), for Multicast cells renamed as AUX.

5.1.21 Filter Mask Register (Write)

	7	0	
FMR	FM(7:0)		34_H
	FM(15:8)		35_H
	FM(23:16)		36_H
	FM(31:24)		37_H

Hardware reset value all 0

Software reset value (no change)

Readable for test purposes.

FM(31:0) Filter Mask

FM(31:0) defines the valid bits for the comparison of the routing address RA(31:0) in the internal header with the ASM-identification register ID(31:0).

Note: If the Filter Mask is all 0, all cells will accepted by the ASM. This feature is used e.g. in a multiplexer.

5.1.22 LIC Protection Switch Register (Write)

	7	0	
LPSR	LPS1(3:0)	LPS0(3:0)	38_H
	LPS3(3:0)	LPS2(3:0)	39_H
	LPS5(3:0)	LPS4(3:0)	$3A_H$
	LPS7(3:0)	LPS6(3:0)	$3B_H$
	LPS9(3:0)	LPS8(3:0)	$3C_H$
	LPS11(3:0)	LPS10(3:0)	$3D_H$
	LPS13(3:0)	LPS12(3:0)	$3E_H$
	LPS15(3:0)	LPS14(3:0)	$3F_H$

Hardware reset value LPS0(3:0) = 0000
LPS1(3:0) = 0001
LPS2(3:0) = 0010
LPS3(3:0) = 0011
:
LPS15(3:0) = 1111

Software reset value (no change)

Readable for test purposes.

These registers control the output multiplexer (refer to **Figure 10**).

LPS0 … 15(3:0) LIC Protection Switch

The 16 LPS-registers (LPS0 … LPS15) define which output queue is switched to which output line. Here the register LPS0 defines the queue for the output 0, LPS1 the queue for output 1 up to LPS15 the queue for output 15.
Cells routed to an output port which is not connected to an output line, are discarded. Several outputs may be connected to the same output queue.

5.1.23 Transmit Cell Register 0 (Write Only)

	7	0	
TCR0	Transmit Cell Octet # 1		40_H
	:		:
	:		:
	Transmit Cell Octet # 63		$7E_H$
	Transmit Cell Parity (columnwise, odd)		$7F_H$

Hardware reset value unknown

Software reset value (no change)

Via the Transmit Cell Register the µP can insert test cells into the actual cell data stream. Cells from this input are handled in the same way as if they were received on any other ASM input port, but the cell format is different. The first octet, octet 0 = sync. octet, is omitted. Instead of this, after the last octet (octet 63) an odd parity octet must be inserted.
It is not required to exchange the complete contents of TCR0 if only a few octets are different in the next cell. However, the parity octet must be recalculated.
The internal cell transfer starts if TX0 in the Command Register COR has been set to 1 by the µP, and is completed when TX0 has been reset to 0 by the ASM. After that TCR0 may be changed for the next cell. The TX0-bit is also set after writing the last octet (octet 63).

5.1.24 Transmit Cell Register 1 (Write Only)

	7	0	
TCR1	Transmit Cell Octet # 1		80_H
	:		:
	:		:
	Transmit Cell Octet # 63		BE_H
	Transmit Cell Parity (columnwise, odd)		BF_H

Hardware reset value unknown

Software reset value (no change)

The TCR1 register is identical to the TCR0. It allows an additional processor or protocol chip to insert communication cell into the actual cell data stream. The internal cell transfer starts if TX1 in the Command Register COR has been set by the µP, and is completed when TX1 has been reset by the ASM. After that TCR1 may be set for the next cell. The TX1-bit is also set after writing the last octet (octet 63).

5.1.25 Receive Cell Register (Read Only)

	7	0	
RCR0	Receive Cell Octet # 1		$C0_H$
	:		:
	:		:
	Receive Cell Octet # 63		FE_H
	Receive Cell Parity (columnwise, odd)		FF_H

Hardware reset value unknown

Software reset value (no change)

RX = 1 in the Command Register COR indicates that a new cell is available in the Receive Cell Register. The cell format is identical to the format in TCR0/1.
When the last octet, which is the Receive Cell Parity (address FF_H), has been accessed for readout, the ASM resets RX automatically. Otherwise, if the µP does not read the complete cell, RX can be reset by the µP to start the next internal cell transfer into RCR, if there is another cell available in the µP output queue.

Note: The cell parity is not checked by the ASM. This has to be done by the µP or protocol chip.

6 Application

6.1 Example for System Configuration

The following example explains the programming of the routing control registers for a switching network consisting of a 64 × 64 funnel-type switching network core expanded by single chip multiplexers MUX (see **Figure 31**). In the most general case a cell must find its way through the input multiplexer MUXIN, through the switching network core and through an output multiplexer MUXOUT. If input and output of the cell path are at the same multiplexer the way through the core should be omitted in order to avoid unnecessary load inside the core. For the definition of MUXIN and MUXOUT see **Figure 27**. Both are realized by one single ASM working in split mode and connected to the core with a bundle of 4 SLIF lines as shown in **Figure 28**.

Also multicast connections will be set-up where a cell input at one port of the switching network is replicated and output at two or more output ports. Even the full broadcast case is possible where the cell is replicated to all outputs. Some branches of a multicast connection could be at the same multiplexer as the root branch and some other branches at other multiplexers.

Several possibilities exist to address such a network; one of them is described in the following.

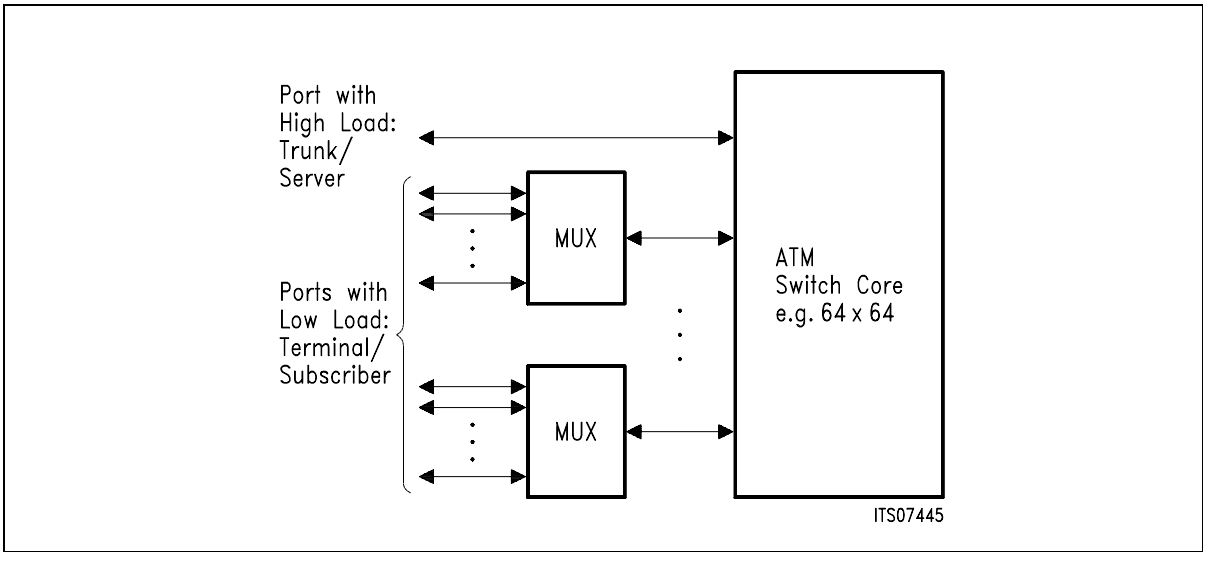


Figure 31 Example Switch

The self-routing ATM cell could have the following assignment of the 32-bit routing field:

Unused	MUXIN	Funnel	Route	Unused	MUXOUT
4	4	4	4	12	4

– MUXIN: this field specifies the path through the input multiplexer. It allows short path connections, i.e. connections between terminals at the same multiplexer.
– Funnels: This field specifies in a bit mapped form one of the four funnels. For point-to-point connections only one of the 4 bits is set to one, the other 3 bits are set to zero; e.g. funnel = 0100 selects the second funnel.
– Route: This field specifies the output of the selected funnel.
– MUXOUT: This field specifies the output of the output multiplexer/concentrator.

The multicast ATM cell could have the following assignment of the 32-bit routing field:

Unused	Funnel	Unused	Multicast routing address
8	4	4	16

– Funnels: This field specifies the funnel(s) which have to accept the cell. These will be those funnels where the connection has branches. Several bits may be set, e.g. funnels = 0101 determines that the cell is forwarded within the second and the fourth funnel. This measure avoids unnecessary cell traffic in the second stages of the first and third funnel. If during the existence of the connection a further branch is established, e.g. at the third funnel, the value of funnels may be changed to 0111. This would not affect the existing branches.
– Multicast routing address: This field is used by the ASMs which have a multicast RAM connected. They use this field to address the external RAM containing in each entry the outputs to which the cell is to be forwarded in a bitmapped form.

6.1.1 Programming of the ASMs

The switching network core in this example has the size 64 × 64 and is realized as two-stage funnel network consisting of 4 funnels (**Figure 32**). The ASMs in the first stage of the funnels work as filters only. All accepted cells are forwarded to one output which is defined as bundle of 16. The second stage accepts all cells and routes them to the output specified in the four ‘Route’ bits of the cell.

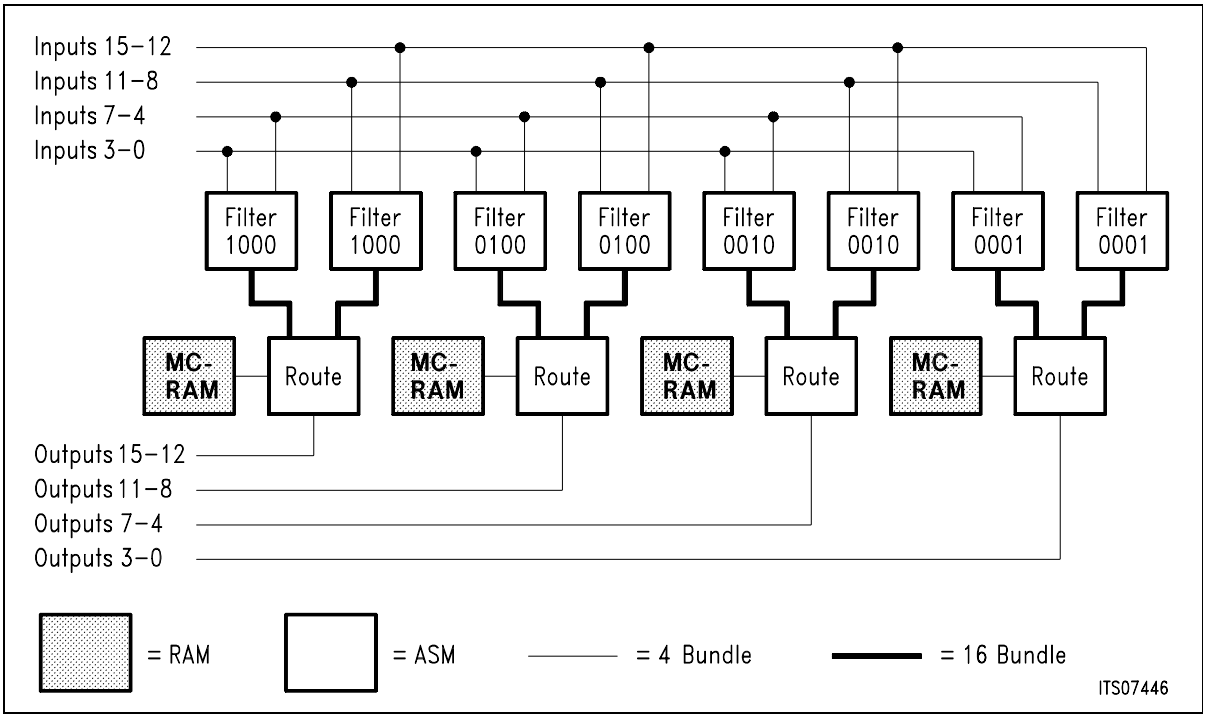


Figure 32 Core Programming Example

Programming of the ASMs in the First Stage

They have different mask register values:

The ASMs ‘Filter 1000’:
FMR(31:0) = 0000 0000 1000 0000 0000 0000 0000 0000
IDR(31:0) = 0000 0000 1000 0000 0000 0000 0000 0000

The ASMs ‘Filter 0100’:
FMR(31:0) = 0000 0000 0100 0000 0000 0000 0000 0000
IDR(31:0) = 0000 0000 0100 0000 0000 0000 0000 0000

The ASM ‘Filter 0010’:
FMR(31:0) = 0000 0000 0010 0000 0000 0000 0000 0000
IDR(31:0) = 0000 0000 0010 0000 0000 0000 0000 0000

The ASM ‘Filter 0001’:
FMR(31:0) = 0000 0000 0001 0000 0000 0000 0000 0000
IDR(31:0) = 0000 0000 0001 0000 0000 0000 0000 0000

All ‘Filter’ ASMs have defined one output bundle of 16:

OGR register:
OPE(15:0) = 1111 1111 1111 1111 enables all outputs

– CBC = 1 to change the bundle configuration, this bit will be reset by the ASM
– OG(14) = 1 to define the bundle of 16, OG(13:0) are don’t care
– OPTR(4:0) = 00000, don’t care, as for one single output the routing bits are not interpreted

The ASMs are programmed to treat also multicast cells as self-routing cells by setting in the Mode register the bit MODR:EVMCI = 0. Then also the multicast cells are filtered and accepted by one or more funnels.

Programming of the ASMs in the Second Stage

FMR(31:0) = all ‘0’, i.e. without filter function
IDR(31:0) = don’t care

OGR register:

– OPE(15:0) = 1111 1111 1111 1111 enables all outputs
– CBC = 1 to change the bundle configuration, this bit will be reset by the ASM
– OG(11:8) = 1111 to define four bundle of 4, all other OGR bits ‘0’
– OPTR(4:0) = 10000, points to the 16^{th} bit position of the routing header field of the cell, thus the routing header bits RA(19:16) indicate the output of the ASM.

The ASM inputs are programmed as two bundles of 16 by setting in the mode register IG0 and IG1 to ‘1’.

Programming of the ASMs in the Multiplexers

FMR(31:0) = all ‘0’, i.e. without filter function
IDR(31:0) = don’t care

OGR register:

– OPE(15:0) = 1111 1111 1111 1111 enables all outputs
– CBC = 1 to change the bundle configuration (this bit will be reset by the ASM)
– OG(8) = 1 to define the bundle of 4 for outputs 0 … 3, all other OGR bits ‘0’
– OPTR(4:0) = 11000, points to the 24^{th} bit position of the routing header field of the cell, thus the routing header bits RA(27:24) indicate the output of the ASM.

The ASM is programmed in split mode by defining inputs 0 … 3 as inputs with fixed routing evaluation, i.e. using the four least significant bits of the routing header RA(3:0). This is done by programming in the Mode register MODR:IS(5:0) = 000100, i.e. the decimal value 4. The cells input at inputs 4 … 31 are treated normally, with the RA(27:24) bits defining the 4-bit field of the output port.

6.1.2 Examples

1) A self-routing cell has the routing header field

RA(31:0) = 0000 0000 0100 0110 0000 0000 1011

– MUXIN = 0000, i.e. the cell is forwarded to output 0 which is part of the output bundle 0 … 3. The cell is forwarded to the core.
– Funnel = 0100, i.e. the second funnel accepts the cell
– Route = 0110, i.e. the cell is forwarded to output 6 of the second funnel
– MUXOUT = 1011, i.e. the cell is forwarded to output 11 of the output multiplexer

2) A multicast cell has the routing header field

RA(31:0) = 0000 0000 0101 0000 0000 0000 0001 1100

– The input multiplexer has a multicast RAM attached and uses the multicast routing address field MCRA(15:0) = 0000 0000 0001 1100 to address the external RAM. The entry may contain the value 0001 0000 0000 0001, i.e. the cell is duplicated to output 0 and to output 12 of this ASM. Output 12 leads to another terminal/subscriber connected to the same ASM, whereas output 0 is part of the bundle of 4 going to the core.
– Funnels = 0101, i.e. the cell is forwarded into the second and fourth funnel.
– The ASMs of the second stages of the two funnels as well as the output multiplexers use the MCRA(15:0) to address their multicast RAM. The cells are forwarded according to the pattern stored under the respective address in the RAMs.

6.2 State after Reset

During the reset state (reset = low) all outputs provide a fixed potential (P-output = high-level; N-output = low-level). When the reset is finished (low-high transition), the ASM becomes active after a latency time, i.e. all output ports provides empty cells. The register values now contain default values, which can be checked via the µP-interface.

After a HW-reset only cells with the SSN = 001 are accepted by the ASM independent from the routing address and are made available via the µP-queue. The output ports deliver only empty cells.

The following section describes the operation state of the ASM after a HW-reset. All register values are defined in section. Here only these values are mentioned which specifies the operation mode of the ASM.

- All data inputs (0 … 31) are enabled
  IOR(31:0) = ‘all 1’
- No input grouping for bundles of 16
  MODR:IG0 = ‘0’ for input ports 0 … 15
  MODR:IG1 = ‘0’ for input ports 16 … 31
- µP-cell acceptance with switching stage number SSN = ‘1’
  MODR:SSN(3:0) = ‘0001’
- All inputs accept only microprocessor cells identified by the correct SSN; all other cells are discarded.
  MODR:AOPC = ‘1’
- No µP-queue limitation
  MODR:PQL = ‘0’
- Interrupt for µP-cells are enabled
  MODR:ACCEL = ‘0’
- The $\overline{\text{INT1}}$ for control cells is disabled, i.e. an incoming control cell with correct SSN activates an interrupt $\overline{\text{INT0}}$ and not the $\overline{\text{INT1}}$.
  MODR:APCEL = ‘1’
- All bits of the interrupt status register ISR except PCRCV are masked, i.e. only µP cells (and no error states) can activate an interrupt.
  IMR = ‘all 1’
- No routing address evaluation, i.e. the µP-cells are only checked for the SSN
  FMR(31:0) = ‘all 0’

After reset the operation mode will be programmed into the ASM(s) of a switching network. This is done using the registers MODR, OGR, IDR and FMR. See the examples described in **Chapter 6.1** for the usage of these registers.

6.3 Test and Communication Channels

The ASM provides functions to support communication channels via the data lines. This is useful for the communication channel between processors and for testing data paths.

To support the communication channels the ASM provides two insertion buffers and one extraction buffer together with the associated transfer registers. A comparison mechanism based on the switching stage number field SSN of the ATM cells determines if a cell is to be extracted from the cell stream and directed to the µP. Two different interrupts are foreseen to inform the µP about the extraction of a cell. Thus two different channels can be supported, e.g. one for control and one for test.

Communication Channel

Especially larger switching networks may extend over several boards, connected e.g. via a backplane. On each board a local processor could be located. At board start-up the on-board processor can be loaded from a main processor with data or program information. During operation the communication channel can be used for conveying e.g. maintenance information and (multicast) connection set-up information. See **Figure 33** for an example configuration where the main processor is connected like a line card via the PXB 4110 SARE chip.

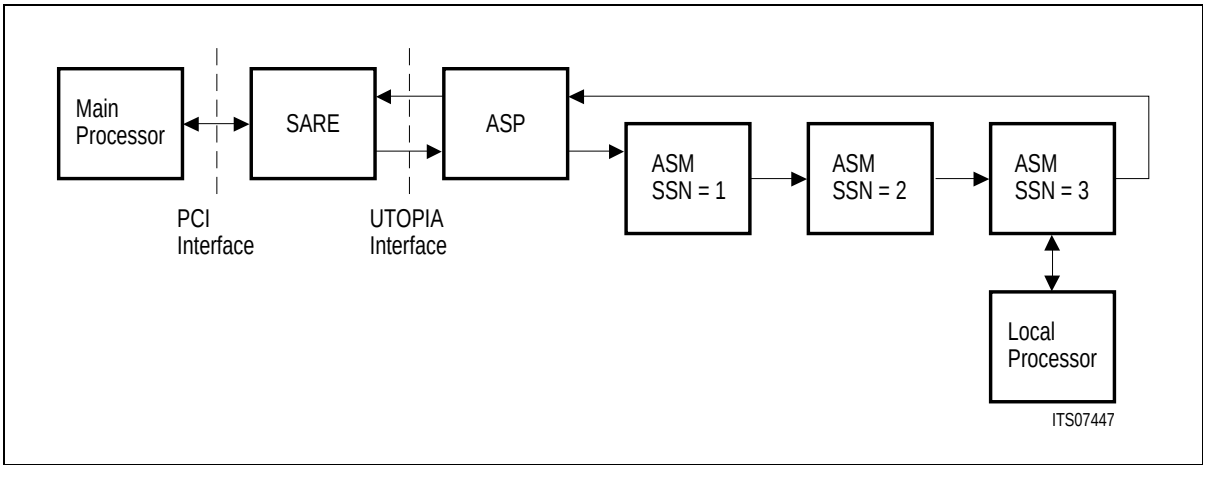


Figure 33 ASM Addressing Concept Using SSNs

For the start-up phase where a large amount of data could be loaded to an on-board processor additional features are provided. It is assumed that during the system start-up phase no user data cells are transferred by the switching network. Therefore the MODR:AOPC bit of the destination ASM can be set to disable all other cells than µP cells. In addition the MODR:PQL bit can be cleared to allocate the whole central buffer for the µP queue.

During operation the control channel between on-board processor and main processor is used to convey maintenance information and the set-up of multicast connections. Maintenance informations are e.g. failure indications and status reports, as the results of

routine checks. The set-up, release or modification of a multicast connection requires to update the entries in all multicast tables in the switch for the multicast routing address. No action in the switching network is required for the set-up of point-to-point connections, as the address of self-routing cells is only added in the ASP.

Test Channel

The communication channels can also be used to test the data paths of the switching network. To check the output data path of an ASM a test cell is inserted by the ASM under test via one of the two transmit registers TCR0 and TCR1. The cell is received either by a subsequent ASM or by the ASP. To check the input data path of an ASM test cells are inserted by a preceding ASM or the ASP. The SSN(3:0) field of the internal cell header allows to destine the test cell specifically to a certain ASM, where it is extracted.

Cells are only extracted by an ASM if SSN and routing address match. **Figure 33** shows in an example how the addressing concept using the SSN works. Subsequent ASMs of a multi-stage switching network have e.g. increasing SSN numbers. So test cells can be directed to every ASM.

The maintenance control cell (see **Table 1**) has a special behavior. This cell is not influenced by the setting of the output multiplexer and uses always the default output. To test the switchover of the output multiplexer test cells with other housekeeping combination as 011b should be used.

Also the buffer limits for fairness management and low priority cells can be tested using the test channel. For this purpose the readout of the output queues is disabled by clearing the OGR:OPE(15:0) bits. Then multiple test cells are sent to the different output queues to check both the maximum and the adjustable limit. This can be done for different combinations of output grouping.

6.4 Error Detections and Indications

6.4.1 External Error Detection

The ASM supervises the high speed data inputs on the following errors:

– Synchronization State (SYNC/ASYNC)

The ASM checks the SYNC-octet of each incoming cell. If only one SYNC-octet of a cell is invalid, this error is indicated in the registers ISR, LFR, and LER (dependent on ILA). The corrupted cell is not discarded.

If two or more consecutive cells with invalid SYNC-octet are detected, this error is indicated in the registers ISR, LASR, LFR, and LER (dependent on ILA).

The transition to the ASYNC-state is attended with three additional actions:

- No header evaluation for the affected line
- Discarding of the corresponding cells
- Restart of the synchronization mechanism. The synchronous state is established again if at least two valid SYNC-octets have been detected in series.

– Parity Check of the Internal Header

The ASM checks the parity bit of the internal header (octet 1 … 6) for each incoming cell. If a parity error occurs, this error is indicated in the registers ISR, LFR, and LER (dependent on ILA). The corrupted cell is discarded.

6.4.2 Internal Error Detection

In the ASM the internal error detection is divided into the supervision of the data path and the control path. The data path is checked by a cell parity byte, the control path is supervised by an additional internal parity bit (e.g. for the cell location data) and by internal plausibility checks.

– Internal Cell Parity Check

The internal cell is protected by an additional parity byte generated at each input port and checked at each output port. If an internal parity error is detected, this error is indicated in the ISR:IPE. The possibly corrupted cell can not be discarded in the ASM. A faulty cell can be detected in a following ASM or ASP.

– Control Path Check

If any failure occurs in the control path, a control error is indicated in the ISR-register. A control error means that cells are discarded. This serious error can only be corrected by a HW-reset.

– Parity Check for Multicast Lookup Table (MLT)

The MLT-entries are also protected with a parity bit. If a parity error occurs, this error is indicated in the ISR:MLTPE. The multicast information of the corrupted entry will be ignored, so that the cell will be discarded.

6.5 Test of Error Indications

The error indications of the ASM can be tested by the µP according to **Table 8**.

Note: Some of the tests cause loss of data cells and are therefore not executable in service. These tests would only be done at system/board start-up.

Table 8 Testing of Error Indications

Error Indication	Abbr.	Testability
Async State	ASYNC	Via at least 2 successive MR:IVSYNC operations; causes loss of data.
Sync Error	SYNCE	Via one MR:IVSYNC operation.
Header Parity Error	PE	Via test cells; causes loss of data.
Control Error	CTRLE	Via MR:IVQRP or MR:IVFCP operations; causes loss of data.
Internal Parity Error	IPE	Via test cells; causes loss of data.
MLT Parity Error	MLTPE	Via MR:IVMCCP operations; may cause loss of data.
Multicast Misrouting	MCMR	Via test cells; causes loss of data.
Buffer Overflow	BOV	Via test cells and/or via OGR:OPE; causes loss of data.
Threshold Overflow	TOV	Via PTR equal to ‘0’; causes loss of low priority cells.
Queue Overflow	QOV	Via MQLR equal to ‘0’; causes loss of data.
Microprocessor Queue Overflow	PQOV	Via test cells or via bit MR:DPQ.

– ASYNC Error Test

Action: Is done by performing at least two successive IVSYNC operations (by setting the bits MR:IVSYNC = ‘1’, OLA(3:0) = ‘binary coded output port (0 to 15)’) on the same output line address (OLA) within a time frame of 2.46 µs at most.

Effect: Two successive cells of the output line selected are provided with a corrupted Synchronization Octet, to generate an ASYNC error indication to ISR, LASR, LER and LFR.

Note: ASYNC errors can be detected only by a ASM/ASP located behind the generating device; the cells concerned get lost in any case.

– SYNC Error Test

Action: Is done by setting the bits MR:IVSYNC = '1' and OLA(3:0) = 'binary coded output port (0 to 15)') to the required values.

Effect: One of the cells, read out from the selected queue, is provided with a corrupted Synchronization Octet to generate a SYNC error indication to ISR, LER and LFR.

Note: Synchronization Errors can be detected only by a ASM/ASP located behind the generating device. If under worst case conditions the Sync Octet of the preceding or successive cell is also corrupted by sporadic noise an ASYNC error instead of a SYNC error is indicated. Cells concerned only from any single SYNC error do not get lost.

– Header Parity Error Test

Action: Insertion of test cells provided with corrupted parity bit in the internal header.

Effect: Parity Errors are detected and mapped into ISR:PE, LER:LPE, and LFR.

Note: Via the µP-Interface test cells can be inserted into the data stream and are evaluated directly in the header evaluation unit of the ASM.

– Control Error Test

Action: Is done by setting the bit MR:IVQRP = '1' (invalidation of the queue RAM bus checks) and/or the bit MR:IVFCP = '1' (invalidation of the Free Cell list parity bit) of the maintenance register.

Effect: Parity errors are produced within the protected queue path and consequently are indicated as Control Errors CTRLE in ISR.

Note: The test described causes the loss of data in any case.

– Internal Parity Error Test

Action: Insertion of test cells provided with a corrupted IPE octet into the data stream running via the Data Output Circuits.

Effect: Every parity violation is detected in the output checkers and indicated as an Internal Parity Error IPE in ISR.

Note: Test cells leaving the ASM via Output Queue 17 (i.e. the µP-interface) are not parity checked and therefore cannot cause an IPE message (test cell removal via Queue 17 is possible for all the ASMs, getting test cells with a valid SSN/ (RA) indication).

– Multicast Lookup Table Error Test

Action: Is done by setting the bit MR:IVMCCP = '1' (invalidation of the MLT parity bit).

Effect: Parity errors are produced within the protected path and consequently are indicated as Multicast Lookup Table Parity Error MLTPE and in ISR.

Note: The test described may cause the loss of data.

– Multicast Misrouting Test

Action: Is done by inserting cells via TCR0/1 with ADI(0) = '1' (actual cell = multicast cell). The MODR:DCMC-bit has to be set to '1'.

Effect: The cell will not be accepted and ISR:MCMR will be set.

– Buffer Overflow Test

Action: Is done by setting the bits OGR:OGE = 'all 0' (disable of the Output Queues) and selecting the bundle mode 16 (to get one output queue with sufficient queue entries to fill up the Central Buffer); the Central Buffer now can be filled up by e.g. sending cells via the TCR0/1.

Effect: The Central Buffer is filled up by data cells to generate a Buffer Overflow message to ISR:BOV.

– Threshold Overflow Test

Action: Is done by setting the Priority Threshold Register PTR to '0'.

Effect: Every cell, just going to be stored in the Central Buffer leads to a Threshold Overflow indication TOV in ISR.

Note: Non-prioritized cells (characterized by a CLP bit = '1') are rejected and lost.

– Threshold Overflow Test

Action: Is done by setting the Priority Threshold Register PTR equal to '0'.

Effect: Every cell, just going to be stored in the Central Buffer leads to a Threshold Overflow indication TO in GER.

Note: Non-prioritized cells (characterized by a CLP bit = '1') are rejected and lost.

– Queue Overflow Test

Action: Is done by setting the threshold of the Maximum Queue Length Register for the belonging output queue to '0'.

Effect: Every cell location entry, just going to be stored in the output queue RAM leads to a Queue Overflow indication QOV in ISR.

Note: All incoming cells are rejected and lost.

– Microprocessor Queue Overflow Test

Action: Is done by setting the threshold of the Microprocessor Queue (MODR:PQL = '1') and MR:DPQ = '1' (disable readout of µP-queue).

Effect: Every cell location entry which exceeds the threshold value, leads to a Microprocessor Queue Overflow indication PQOV in ISR.

Note: All incoming cells exceeding the threshold value are rejected and lost.

7 Electrical Characteristics

7.1 DC Characteristics

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
(DI, $\overline{\text{DI}}$)					
Input high voltage	V_{IH}	–	1.9	V	
Input low voltage	V_{IL}	0.5	–	V	
Input differential voltage	$V_{ID} = V_{IH} - V_{IL}$	0.100	–	V	1)
(CL, $\overline{\text{CL}}$)					
Input high voltage	V_{IH}	–	1.9	V	
Input low voltage	V_{IL}	0.5	–	V	
Input differential voltage	$V_{ID} = V_{IH} - V_{IL}$	0.100	–	V	1)

1) For AC characteristics, higher input swing is necessary.

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
(DO, $\overline{\text{DO}}$)					
Output high voltage	V_{OH}	1.410	1.535	V	2)
Output low voltage	V_{OL}	0.935	1.060	V	2)
Output differential voltage	$V_{OD} = V_{OH} - V_{OL}$	0.400	0.550	V	

2) Each output line is terminated by a 50 Ω resistor (50 Ω lines). Every two matching resistors belonging to one output pair are connected via one capacitor to ground.
Without external termination resistors, the high level becomes V_{CC} and the low level 0 V (time depends on the capacitive load).

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
(ADR0 … 7, DAT0 … 7, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, TEST, TMOD, RES, TFI0 … 1)[3]					
Input high voltage	V_{IH}	2	V_{CC}	V	[4]
Input low voltage	V_{IL}	0	0.8	V	[4]
(DAT0 … 7, TCO0 … 9)[3]					
Output high voltage	V_{OH}	V_{CC} – 0.6	–	V	
Output low voltage	V_{OL}	–	0.4	V	
($\overline{INT0}$ … $\overline{1}$, RDY)					
Output high voltage	V_{OH}	V_{CC} – 0.6	–	V	[5]
Output low voltage	V_{OL}	–	0.4	V	[5]
(TFO0 … 6)					
Output high voltage	V_{OH}				[6]
Output low voltage	V_{OL}				[6]
(CLO, CSS)					
Output high voltage	V_{OL}				[6]
Output low voltage	V_{OL}				[6]

[3] LVCMOS level.
[4] LVCMOS inputs have to be held on either low or high level to avoid floating input lines, when used.
[5] The open drain outputs are connected to the supply voltage V_{CC} via an external pull-up resistor.
[6] The source-follower outputs are connected to the ground potential GND via an external 50 Ω resistor.

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Input Leakage Current					
DI, $\overline{DI}$; CL, $\overline{CL}$;	I_{IL}	– 1	1	µA	
Control-, µP-signals	I_{IL}	– 1	1	µA	

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
(DO, $\overline{DO}$)					
Output high current	I_{OH}				7)
Output low current	I_{OL}				7)
(TCO0 … 9, DAT0 … 7)					
Output high current	I_{OH}				8)
Output low current	I_{OL}				8)

7) 50 Ω, output voltage between 0 V and V_{CC}.
8) LVCMOS level

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

7.2 AC Characteristics (Conditions: See Operating Conditions, Section 7.5)

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Clock Signal (CL, $\overline{CL}$)					
Input differential voltage	$V_{ID} = V_{IH} - V_{IL}$	0.350	–	V	
Transition time	t_{THL}	0.2	0.6	ns	
	t_{TLH}	0.2	0.6	ns	
Skew	t_{SKHL}	– 0.1	0.1	ns	
	t_{SKLH}	– 0.1	0.1	ns	
Width high	t_{WH}	2.26		ns	
Width low	t_{WL}	2.26		ns	
Jitter (peak-peak)	t_{JPP}		140	ps	
Period	t_{CLK}	4.82		ns	9)
Clock/data frequency deviation	f_D	– 1.0	1.0	kHz	10)
Input Data (DI, $\overline{DI}$)					
Input differential voltage	$V_{ID} = V_{IH} - V_{IL}$	0.200	–	V	11)
Input differential voltage	$V_{ID} = V_{IH} - V_{IL}$	0.300	–	V	12)
Transition time	t_{THL}	0.2	1.0	ns	
	t_{TLH}	0.2	1.0	ns	13)
Skew	t_{SKHL}	– 0.2	0.2	ns	
	t_{SKLH}	– 0.2	0.2	ns	
Jitter (peak-peak)	t_{JPP}		2	ns	
Width high	t_{WH}	2.82	6.82	ns	
Width low	t_{WL}	2.82	6.82	ns	

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
µP-, Test-Signals					
Transition Time	t_{THL}				
	t_{TLH}				

9) The nominal operating frequency is 207.36 MHz, i.e. t_{CLK} = 4.82 ns.
10) The clock frequency f_{CLK} and the data rate can differ at most by the specified value (± 1.0 kHz).
11) Standard jitter requirements.
12) Advanced jitter requirements.
13) The max. transition time should be 1.5 ns if the differential input voltage is at least 0.3 V.

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Reset Signal (RESET)					
Transition time	t_{THL}	3	20	ns	
	t_{TLH}	3	20	ns	
Signal width		100		ns	14)
Output clock (CLO)15)					
Transition time	t_{THL}	0.3	0.7	ns	
	t_{TLH}	0.3	0.7	ns	
Jitter (peak-peak)	t_{JPP}		400	ps	
Width high	t_{WH}	t_{CLK} – 0.6	t_{CLK} + 0.6	ns	
Width low	t_{WL}	t_{CLK} – 0.6	t_{CLK} + 0.6	ns	
Cell Start Signal (CSS)					
Transition time	t_{THL}	0.3	0.7	ns	
	t_{TLH}	0.3	0.7	ns	
Jitter (peak-peak)	t_{JPP}		400	ps	
Width high	t_{WH}	$8 \times t_{CLK} - 0.6$		ns	

Electrical Characteristics

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Output Data (DO, $\overline{DO}$)					
Transition time	t_{THL}	0.2	0.6	ns	
	t_{TLH}	0.2	0.6	ns	
Jitter (peak-peak)	t_{JPP}		300	ps	17)
Width high		4.52	5.12	ns	16)
Width low		4.52	5.12	ns	16)
Skew		– 0.10	0.10	ns	

14) During the low frequency test (1 MHz), a minimum value of $2 \times t_{CLK}$ has to be kept.
15) The clock output frequency is identical to the input clock, i.e. f_{CLO} = 207.36 MHz.
Attention: The phase relation between the clock output and the output data differ to each port.
16) For nominal clock period = 4.82 ns.
17) In case of non terminated open outputs the jitter value for used adjacent outputs can increase to 400 ps.

Note: The proposed solutions for the bit phase alignment circuitry presently can cope with a maximum deviation of the data (and clock) of about $\pm$ 1 ns per cell assuming a frequency deviation of better than 10^{-5} (for asynchronous operation).

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

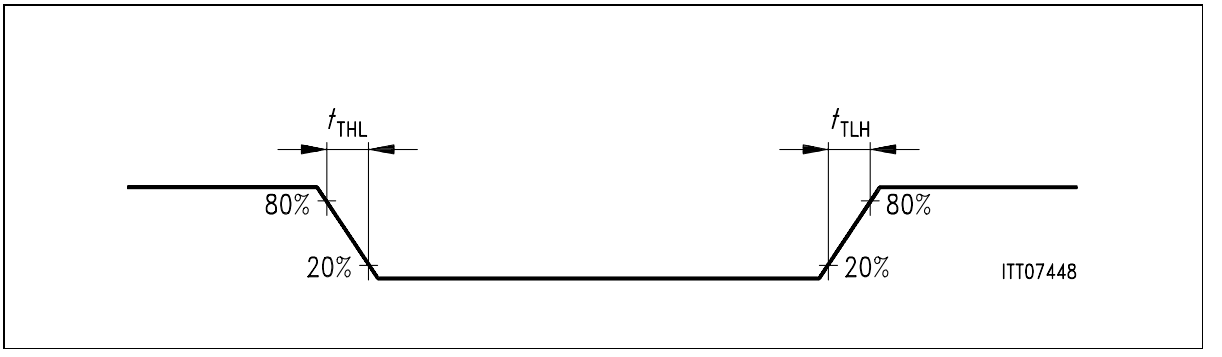


Figure 34 Transition Timing

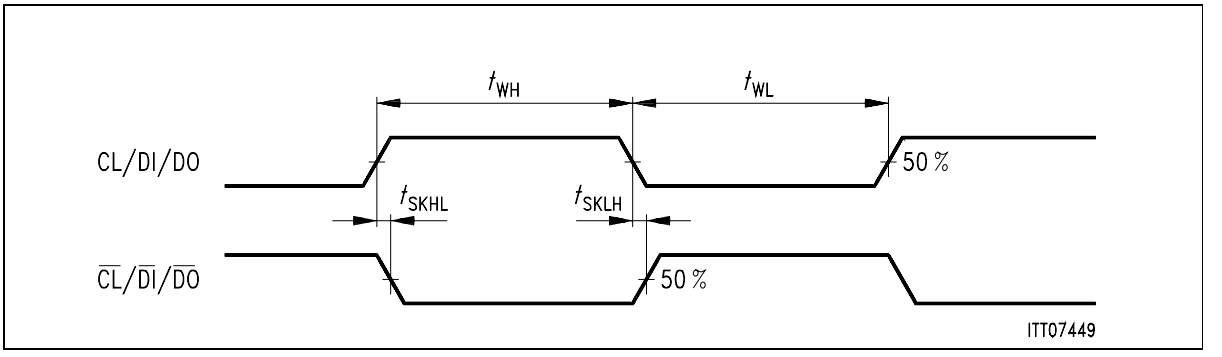


Figure 35 Clock/Data Timing

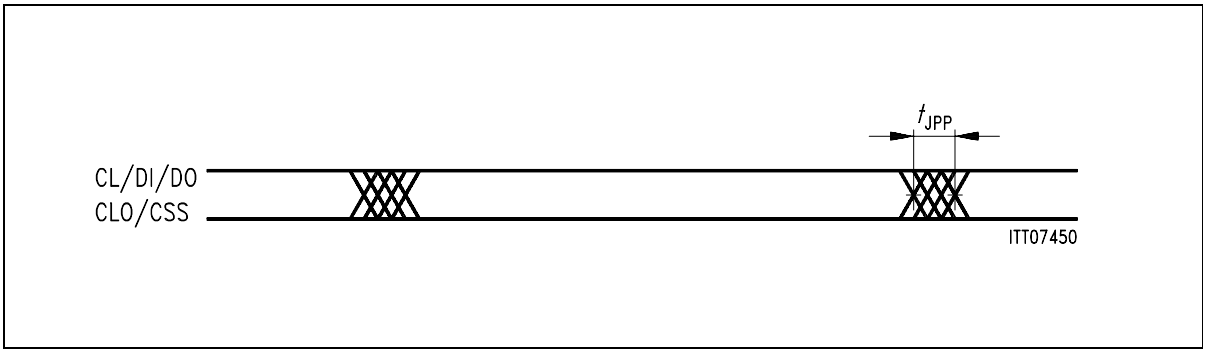


Figure 36 Jitter

7.3 µP-Interface Signals (See Timing Figure 37)

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Write Operation					
ADR setup to write low	t_{AW}	0		ns	
$\overline{CS}$ low to write low	t_{CW}	0		ns	
Write low pulse width	t_{WL}	200		ns	17)
ADR, $\overline{CS}$ hold after write high	t_{WC}	0		ns	
Write inactive time	t_{WI}	20		ns	
RDY (Ready) low delay from write low	t_{WY}	0	20	ns	
RDY (Ready) low pulse width write	t_{RYW}	25	140	ns	
Write high after ready high	t_{RWH}	0		ns	
Data setup to write high	t_{DW}	30		ns	
Data hold after write high	t_{WD}	10		ns	
Read Operation					
ADR setup to read low	t_{AR}	0		ns	
$\overline{CS}$ low to read low	t_{CR}	0		ns	
Read low pulse width	t_{RL}	240		ns	17)
ADR, $\overline{CS}$ hold after read high	t_{RC}	0		ns	
Read inactive time	t_{RI}	20		ns	
RDY (Ready) low delay from read low	t_{RY}	0	20	ns	
RDY (Ready) low pulse width read	t_{RYR}	25	140	ns	
Read high after ready high	t_{RRH}	0		ns	
Data valid after read low	t_{RDV}		180	ns	
Data valid before ready high	t_{DRY}	10		ns	
Data float after read high	t_{DF}		20	ns	

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Interrupt Inactive					
Interrupt high after $\overline{RD}/\overline{WR}$ high	t_{IH}		50	ns	18)
Interrupt inactive delay	t_{ID}	100		ns	

17) This MIN-value is necessary if no READY is used.

18) If an interrupt is pending this will only occur when writing into the command register with RX-bit = 1 or reading RCR(63) or reading ISR.

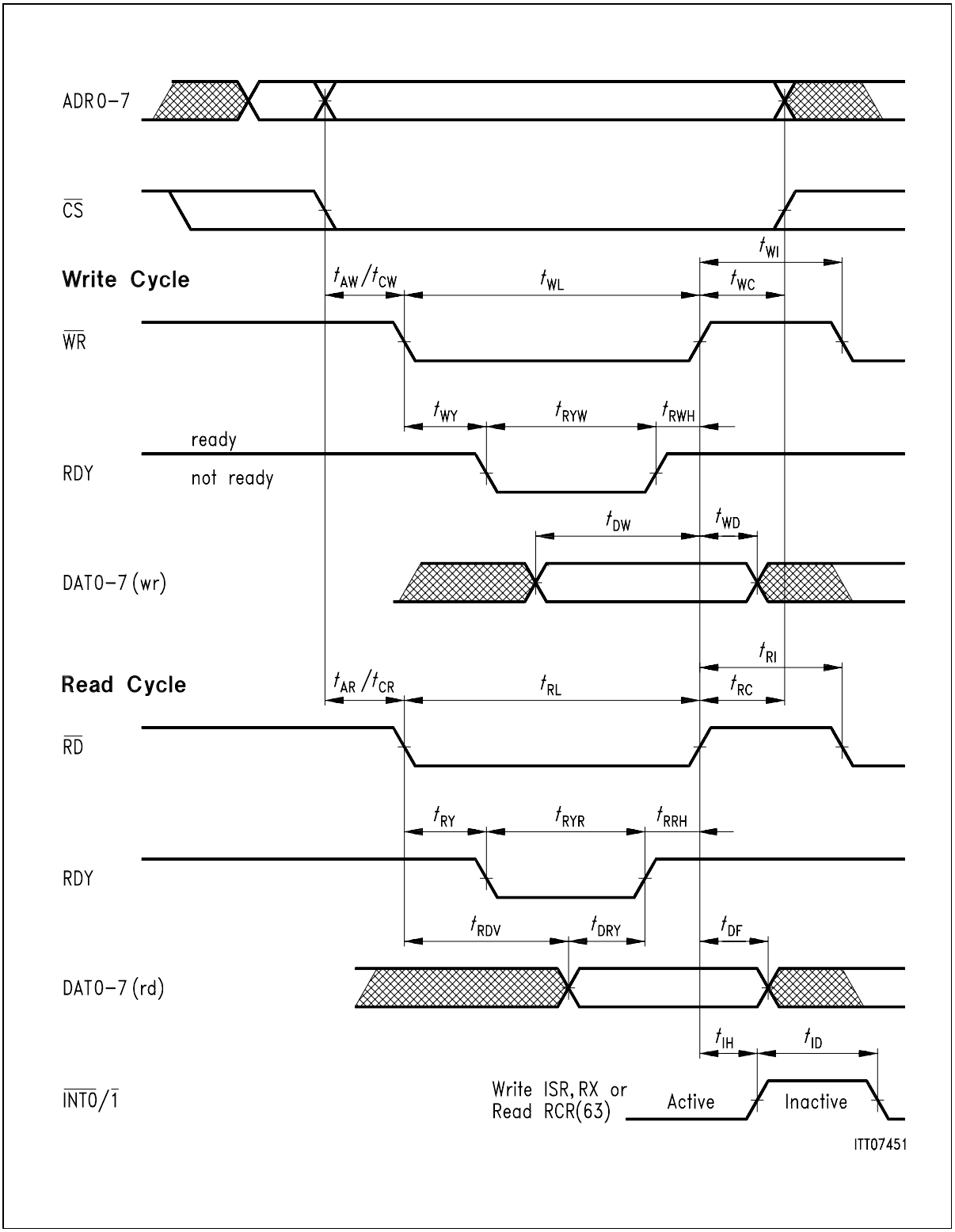


Figure 37 µP Read/Write Cycle

7.4 Multicast RAM Interface Signals (See Timing Figure 38)

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
ASM Parameters					
MCCLK cycle time	t_{CLK}	38.6	38.6	ns	[19]
MCADR setup to MCCLK high	t_{AS}	5		ns	
MCADR hold after MCCLK high	t_{AH}	1		ns	
$\overline{\text{MCWR}}$ setup to MCCLK high	t_{WS}	5		ns	
$\overline{\text{MCWR}}$ hold after MCCLK high	t_{WH}	1		ns	
$\overline{\text{MCOE}}$ low to MCCLK high	t_{ES}	15		ns	
$\overline{\text{MCOE}}$ high after MCCLK high	t_{EH}		10	ns	
MCDAT setup to MCCLK high	t_{DS}	5		ns	
MCDAT hold after MCCLK high	t_{DH}	1		ns	
RAM Parameters					
$\overline{\text{MCOE}}$ low to MCDAT low – Z	t_{LZOE}	0	10	ns	
$\overline{\text{MCOE}}$ high to MCDAT high – Z	t_{HZOE}	2	5	ns	
MCCLK high to MCDAT valid	t_{CD}		12	ns	

[19] MCCLK is derived from the internal Octet Clock, which is 1/8 of the operating clock.

ASM	RAM (e.g. Samsung KM718BV87)
MCCLK	K
MCADR 0 … 15	A 0 … 15
$\overline{\text{MCWR}}$	$\overline{\text{LW}}$, $\overline{\text{UW}}$
$\overline{\text{MCOE}}$	OEN
MCDAT 0 … 15	I/O 0 … 15
MCPAR	I/O 16

Static ‘0’	$\overline{\text{CS}}$, $\overline{\text{ADSP}}$, $\overline{\text{ADSC}}$
Static ‘1’	$\overline{\text{ADV}}$
Not connected	I/O 17

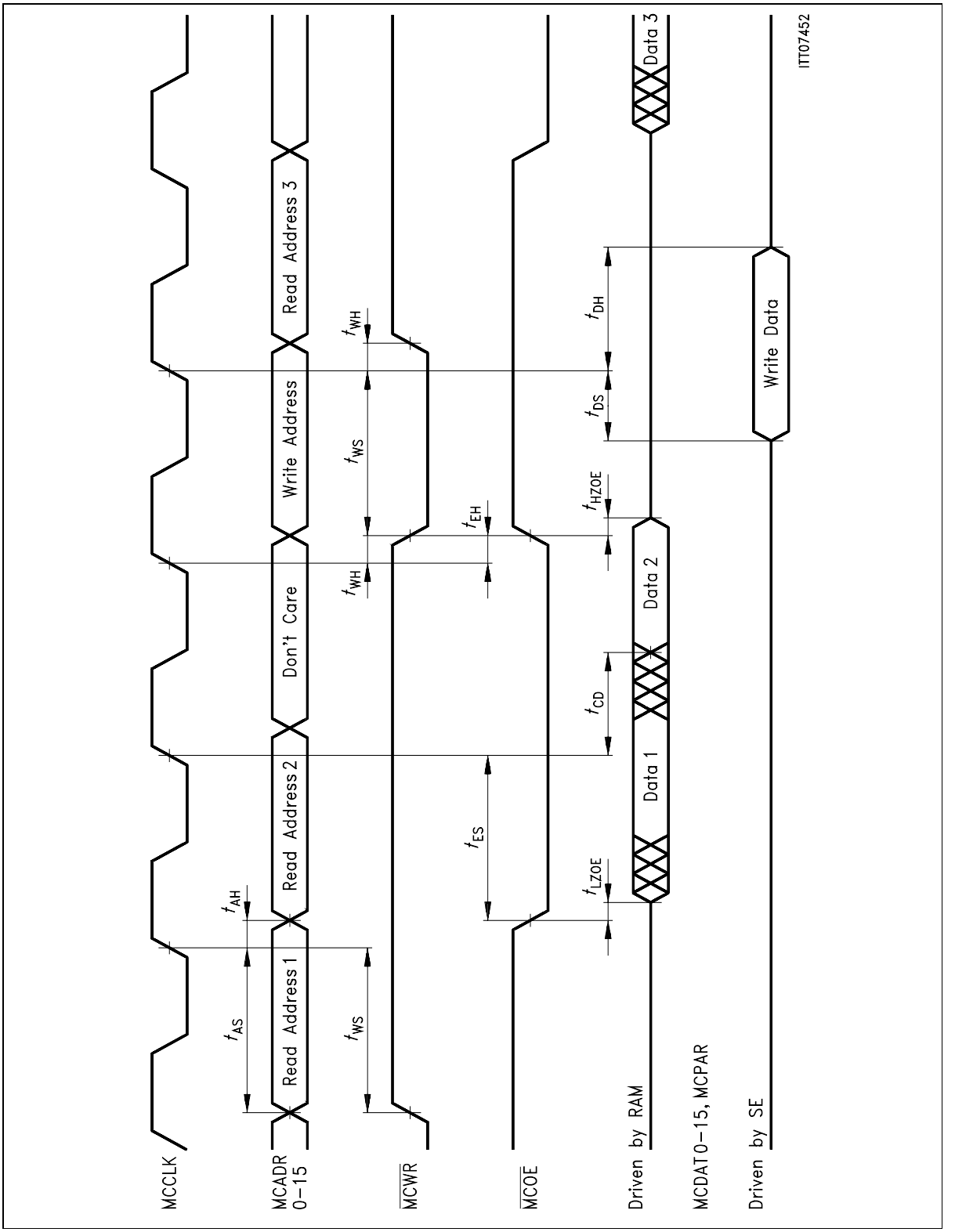


Figure 38 Multicast Timing

7.5 Power Supply

Table 9 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Storage temperature	T_S	– 65	150	°C	
Junction temperature	T_J		125	°C	
Supply voltage	V_{CC}	– 0.5	4.6	V	
Input voltage	V_{IN}	– 0.5	V_{CC} + 0.5	V	
Output voltage	V_{OUT}				
Input/output currents	I	– 20	20	mA	1)
Continuous output current		– 25	25	mA	2)
Power dissipation	P		3.7	W	

1) The cited figures are valid for input voltages of V_{IN} < 0V, V_{IN} > V_{CC} respectively (input currents) and for output voltages of V_{OUT} < 0 V, V_{OUT} > V_{CC} (output currents) respectively.
2) The cited figures are valid for output voltages V_{OUT} between 0 V and V_{CC} (0 V < V_{OUT} < V_{CC}).

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 10 Operating Conditions

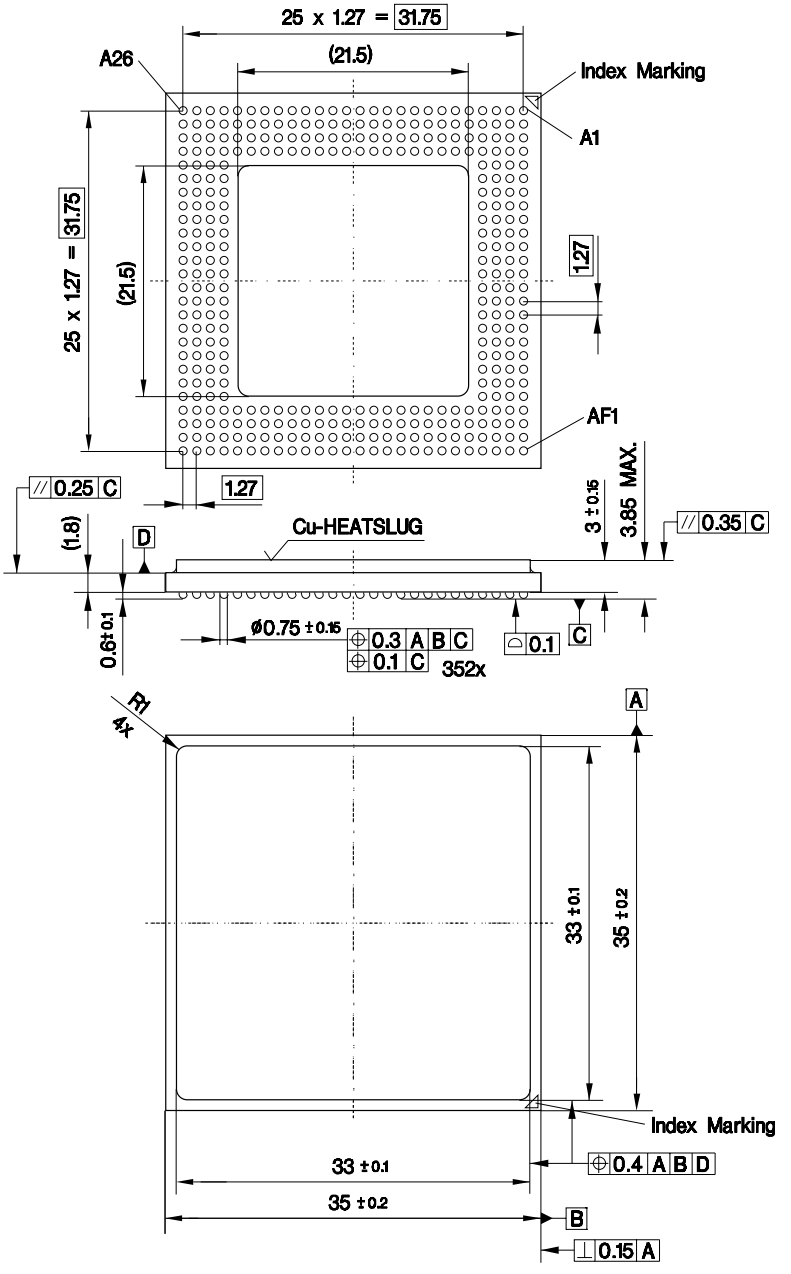
Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		
Supply voltage	V_{CC}	3.135	3.465	V	3)
Digital ground	GND	0		V	
Ambient temperature	T_A	0	70	°C	4)
Junction temperature	T_J		100	°C	

3) The voltages V_{CC} can be switched on and off in any given sequence.
4) The upper limit of the allowed ambient temperature strongly depends upon the package, the mounting and the air flow conditions. In any case the maximum chip junction temperature of 100 °C must not be exceeded for a proper chip operation (see dynamic characteristics).

Note: All timing values are valid for the recommended operating frequency of 207.36 MHz. This frequency has the advantage of having a simple relationship of 4/3 to the SDH/SONET frequency of 155.52 MHz.

8 Package Outlines

P-BGA-352
(Plastic Ball Grid Array Package)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm

9 Appendix

9.1 Performance

The ASM can be modeled in the following way. Each output is represented as a multiplexer with N inputs and one output, each operating at the transmission speed R (see **Figure 39**). The multiplexer has N times higher speed than the inputs, so that all cells are forwarded to the output queue within one cell cycle. Each input receives an equal cell load L/N, such that the output load is L.

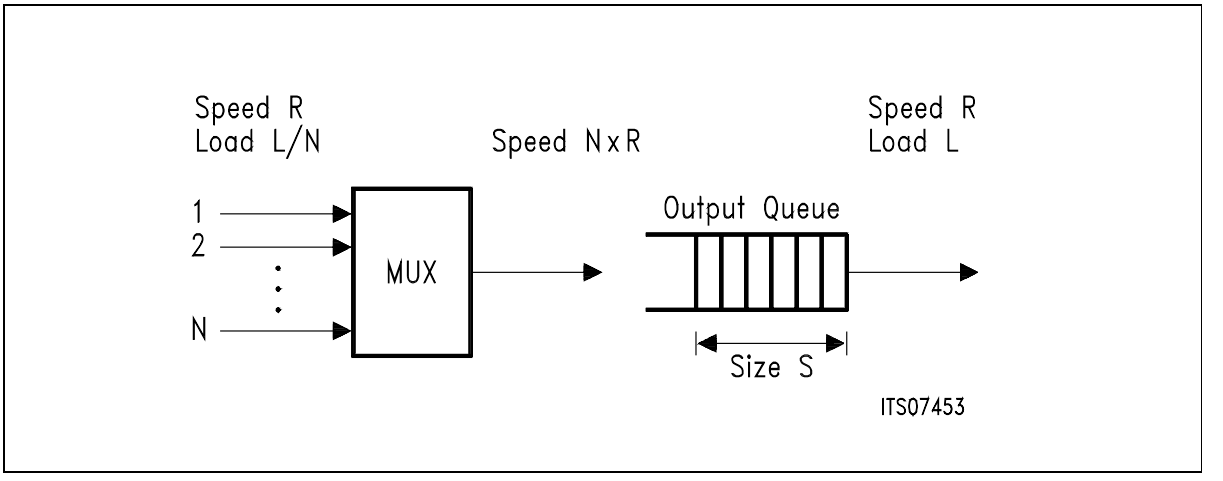


Figure 39 Modeling an ASM Output

Investigations have shown that the behavior of N|1 multiplexers is independent from the value of N for N > 8. The reason is that if the number of inputs increases the load on each input decreases, such that the probability that cells from different inputs arrive at the same time remains constant. The phenomenon, that several cells arrive at the same time leads to a filling of the output queue. If it occurs repeatedly the output queue with a given size S may overflow.

The important parameter to be determined is the probability that the output queue overflows. It can be calculated if a Bernoulli arrival process is assumed. This means that in each cell cycle there is the same probability for a cell arrival. Its value in the case of **Figure 39** is L/N. Theoretically the output queue could become infinitely large, but with very low probability. This probability can be calculated using basic probability calculation **[4]**.

For this purpose a steady state is assumed, i.e. output load L < 1 (otherwise the buffer would constantly fill up). Then the probabilities are calculated that the buffer is filled with 0, 1, 2, … S cells. If these values are summed up the result is the probability that the buffer filling is less or equal to S. In a similar way the probabilities of the propagation delays can be calculated.

The ASM has 16 outputs with 16 associated output queues. The cell storage, however, is done in a common central buffer. With this concept the total required buffer size is not

16 times the size of one buffer, but much less. The reason is, that it is very unlikely that at the same time all queues are filled to maximum value. Mathematically this is expressed by the convolution of the probability distributions.

Numerical results are shown in the following figures. **Figure 40** shows the required buffer sizes for different multiplexers depending on the load of the output. It can be seen that the x|16 multiplexer needs much less than 16 times the x|1-multiplexer. This shows that the shared buffer concept has a minimum buffer usage.

These curves are useful for the definition of fairness levels for output bundles. If e.g. a 4-bundle is to be operated at a load of 0.85, the x|4-curve returns the value of approximately 105 cells.

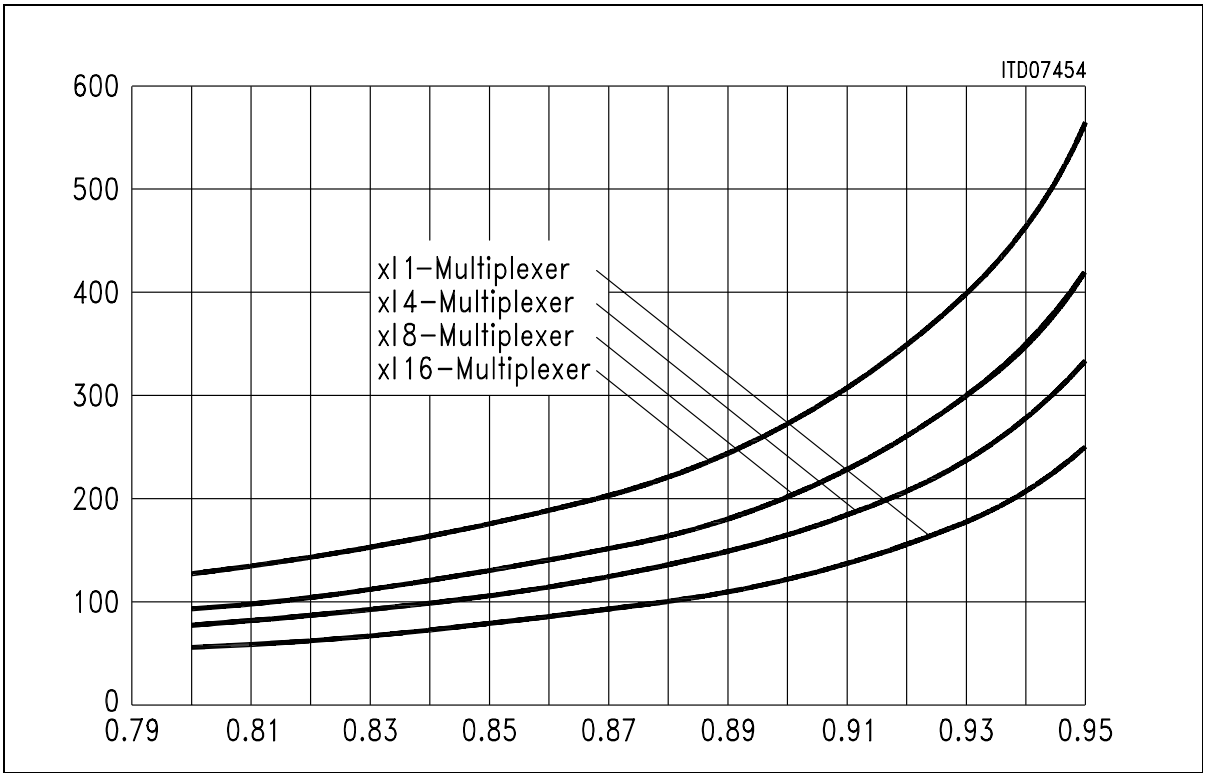


Figure 40 Buffer Sizes for Cell Loss Probability 10^{-11}

Another main performance parameter of the ASM, the cell loss probability depending on the cell load, is shown in **Figure 41**.

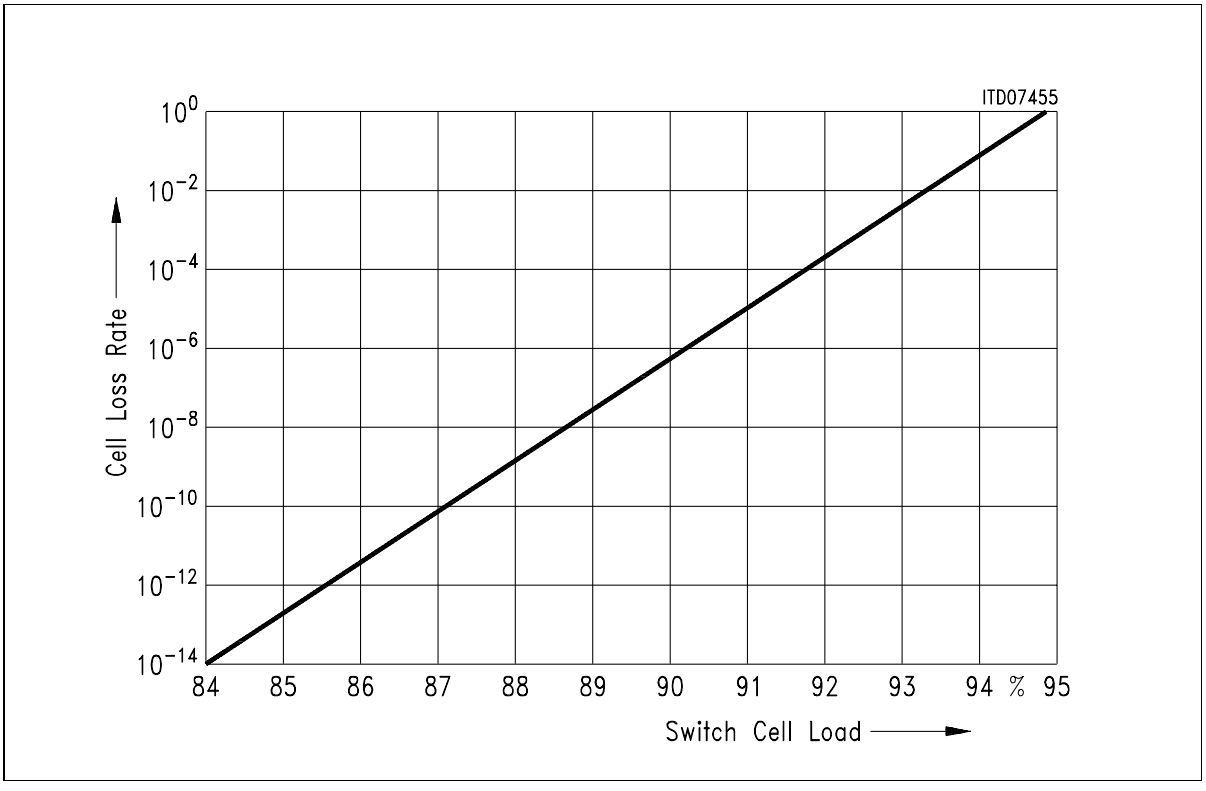


Figure 41 Cell Loss Rate versus Load

Note: The switch cell load must be converted to the real load at the output ports taking into account the speed increase and the internal cell format. Given the external ATM data rate the internal rate can be calculated.

Switch link load = external link load × 64/53 × external ATM rate/switch rate
e.g.
external link load = 149.76 Mbit/s (STS-3c or STM-1 payload rate)
switch rate = 207.36 Mbit/s (using clock speed 155.52 × 4/3 MHz)
external link load = 95 %
result: Switch link load = 82.85 %.

The same model can be used to derive another important performance parameter of the ASM, the cell delay variation CDV. In **Figure 42** below the probabilities for cell propagation delay through the ASM are shown for different load values. The horizontal axis is scaled in cell cycles. The vertical axis shows the probability for a cell to pass the ASM with the respective delay. The minimum propagation delay of 2 cell cycles is the pure cell forwarding delay determined by the HW. The additional delays are due to queueing.

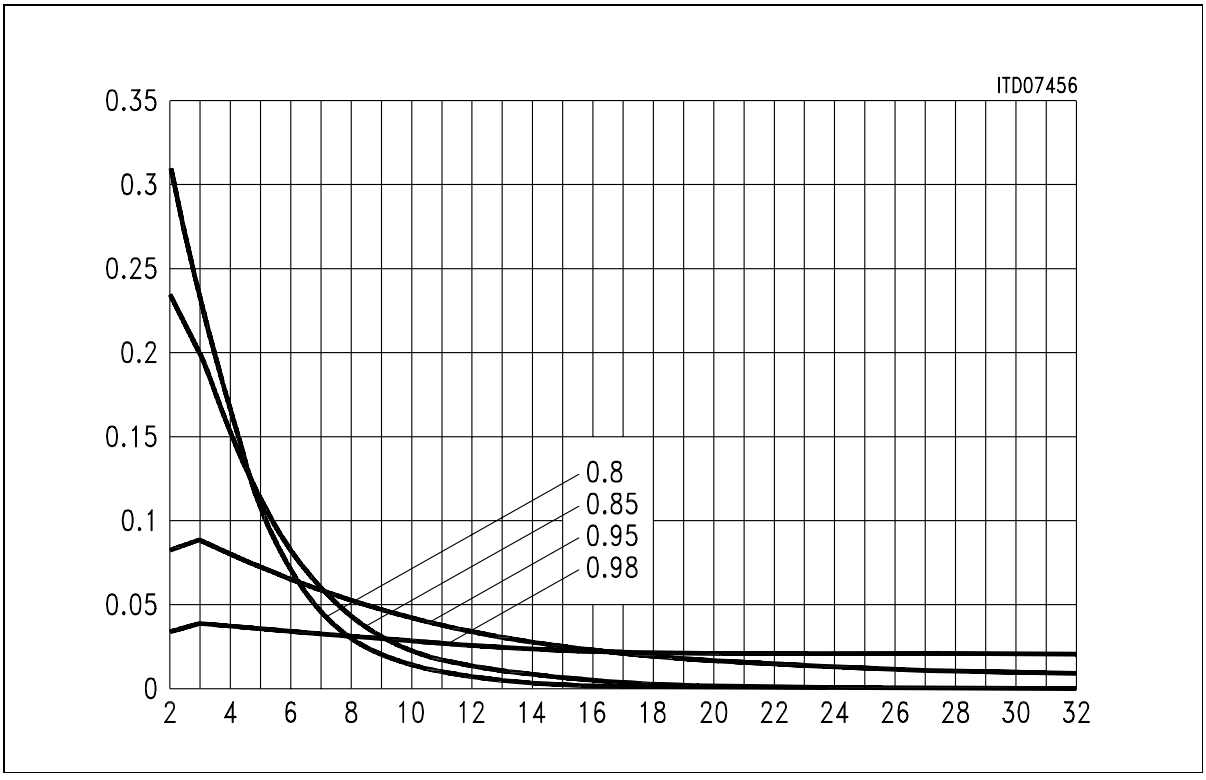


Figure 42 Cell Delay Probability

It can be seen that for a (overall) switch load of 0.8 the probability to experience no queueing delay at all is 0.3, i.e. 30 % of the cells pass the ASM with minimum delay. 24 % of the cells experience a delay of 3 cell cycles, 16 % 4 cycles and so on. If the values are summed up, 98 % of the cells experience a delay less or equal than 10 cell cycles. The remaining 2 % delay probability for all values beyond 10 cell cycles is called 0.02-quantile. Quantiles of special interest is listed the 10^{-9} … 10^{-11}-quantiles, as they are used for dimensioning the maximum allowed load of the links.

10 Overview Lists

10.1 References

1. UTOPIA Level 1 Specification Version 2.01, March 21, 1994, ATM Forum
2. UTOPIA Level 2 Specification Version 1.0, June 1995, ATM Forum
3. IEEE 1596.3 Standard for Low-Voltage Differential Signals for SCI, Draft 1.3, Nov. 95
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10.2 Glossary and Abbreviations

Table 11 Glossary and Abbreviations

AAC	Accept All Cells
AANIC	Accept All Non Empty Cells
ACCEL	Accept Control CELl
AMX	ATM Multiplexer
AOPC	Accept Only µP-Cells
APCEL	Accept µP-CELl
ASN	ATM Switching Network
ASYNC	ASYNChronous State
ATM	Asynchronous Transfer Mode
ATM-1	ATM for STM-1 channels with 155.52 Mbit/s
ATM-4	ATM for STM-4 channels with 622.08 Mbit/s
ATM-16	ATM for STM-16 channels with 2488.32 Mbit/s
BOV	Buffer OVerflow
CBC	Change Bundle Configuration
CLP	Cell Loss Priority

Table 11 Glossary and Abbreviations

COR	COmmand Register
CTRLE	ConTRoL Error
DCMC	DisCard MultiCast
DOS	Disable OverScan
DPA	Disable Phase Alignment
DPQ	Disable µP-Queue
EVMCI	EValuate MultiCast Identifier
EVMCM	EValuate MultiCast identifier for split mode
EVMCP	EValuate MultiCast Parity
FIFO	First In First Out memory
FM	Filter Mask
FMR	Filter Mask Register
GND	GrouND potential
I/O	Input/Output
ID	ASM IDentification
IG	Input Grouping
ILA	Input Line Address
IMR	Interrupt Mask Register
IOR	Line Online Register
IPE	Internal Parity Error
IS	Input Select
ISR	Interrupt Status Register
IVFCP	InValidate Free Cells List Parity
IVMCCP	InValidate MCC Parity
IVQRP	InValidate Queue RAM Parity
IVSYNC	InValidate SYNChronization Octet
LAN	Local Area Network
LASR	Line Asynchronous State Register
LASYNC	Line ASYNChronous State
LER	Line Error Register
LFR	Line Failed Register

Table 11 Glossary and Abbreviations

LIC	Line Interface Circuit
LPE	Line Parity Error
LPS	LIC Protection Switch
LPSC	LIC Protection Switch Change
LPSR	LIC Protection Switch Register
LSB	Least Significant Bit
LSYNC	Line SYNChronization Error
LVCMOS	Low Voltage CMOS
LVDS	Low Voltage Differential Signals
MASYNC	Mask ASYNChronous State
MBOV	Mask Buffer OVerflow
MC	MultiCast
MCA	MultiCast Address Register
MCINI	MultiCast RAM INItialization
MCMR	MultiCast MisRouting
MC-RAM	MultiCast RAM
MCTRLE	Mask Control Error
MIPE	Mask Internal Parity Error
MLT	Multicast Lookup Table
MLTPE	Multicast Lookup Table Parity Error
MMCMR	Mask MultiCast MisRouting
MMLTPE	Mask Multicast Lookup Table Parity Error
MODR	MODe Register
MPE	Mask Parity Error
µP	MicroProcessor
MPE	Mask Parity Error bit
MPQOV	Mask Microprocessor Queue Overflow
MQLR	Maximum Queue Length Register
MQOV	Mask Queue Overflow
MR	Maintenance Register
MSB	Most Significant Bit

Table 11 Glossary and Abbreviations

MSYNCE	Mask Synchronization Error
MTOV	Mask Threshold Overflow
MTR	Multicast Transfer Register
MUX	MUltipleXer
NRZ	Non-Return to Zero
OG	Output Grouping
OGE	Output Port Enable
OGR	Output Group Register
OLA	Output Line Address
OMR	Operation and Maintenance Register
OPE	Output Port Enable
OPQ	OutPut Queue
OPTR	Output PoinTeR
P	Parity
PCRCV	µP-Cell in ReCeiVe buffer
PE	Parity Error
POV	Processor Queue OVerflow
PQL	µP-Queue Length
PQOV	MicroProcessor Queue OVerflow
P/S	Parallel/Serial Converter
PSI	Protection Switch Identifier
PTR	Priority Threshold Register
PT-PT	Point-to-Point
QOV	Queue Overflow
RAM	Random Access Memory
RCR	Receive Cell Register
RMLT	Read Multicast Lookup Table (MC-RAM)
ROM	Read Only Memory
RX	Receive µP/communication Cell
S/P	Serial/Parallel Converter
SCI	Scalable Coherent Interface

Table 11 Glossary and Abbreviations

SLIF	Switch Link InterFace
SRES	Software Reset
SSN	Switch Stage Number
STCO	Select Test Control Output
STFO	Select Test Fullcustom Output
STM	Synchronous Transfer Mode
STM-1	STM basic signal with 155.52 Mbit/s
STM-4	STM multiplex signal with 622.08 Mbit/s
STM-16	STM multiplex signal with 2488.32 Mbit/s
SWPQ	SWitch µP-Queue
SYNC	SYNChronous state
SYNCE	SYNChronization Error
t.b.d.	To be defined
TCR	Transmit Cell Register
TOS	Test Output Select
TOV	Threshold OVerflow
TRT	Test Routing Bits
TX0	Transmit µP-cell
TX1	Transmit communication cell
V_{cc}	Supply Voltage
WA	Wide Area Network
WMLT	Write Multicast Lookup Table (MC-RAM)