Am25S373 • Am54S/74S373
Am25S533 • Am54S/74S533

Octal Latches with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- 8-bit, high-speed parallel latches
- Am25S/54S/74S373 has non-inverting inputs
- Am25S/54S/74S533 has inverting inputs
- V_{OL} = 0.5V (max) at I_{OL} = 20mA
- Am25S versions with I_{OL} = 32mA
- Hysteresis on latch enable input for improved noise margin
- 3-state outputs interface directly with bus organized systems
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

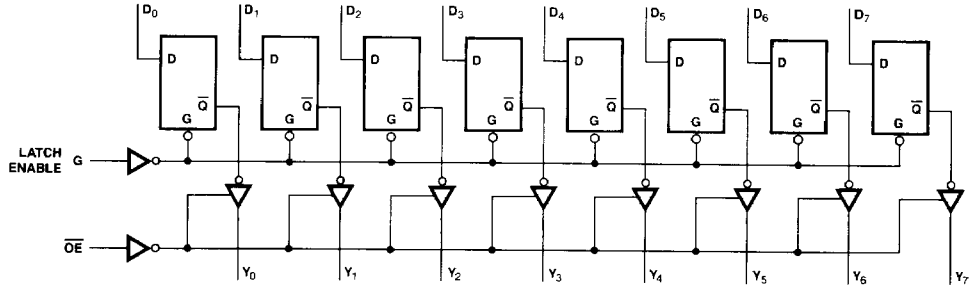
The Am25S/54S/74S373 and Am25S/54S/74S533 are octal latches with 3-state outputs for bus organized system applications. The latches appear to be transparent to the data (data changes asynchronously) when latch enable, G, is HIGH. When G is LOW, the data that meets the set-up times is latched. Data appears on the bus when the output enable, $\overline{OE}$, is LOW. When $\overline{OE}$ is HIGH the bus output is in the high-impedance state.

The 'S373 presents non-inverted data at the outputs while the 'S533 is inverting.

The devices are packaged in a space-saving (0.3-inch row spacing) 20-pin package.

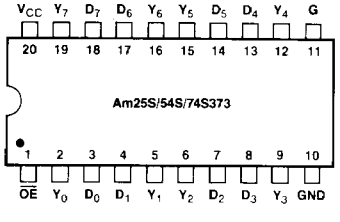
Am25S373 and Am25S533 versions are also available offering V_{OL} = 0.5V (max) at I_{OL} = 32mA.

LOGIC DIAGRAM
Am25S/54S/74S373



Inputs D_0 through D_7 are inverted on the Am25S/54S/74S533. BLI-222

CONNECTION DIAGRAMS – Top Views



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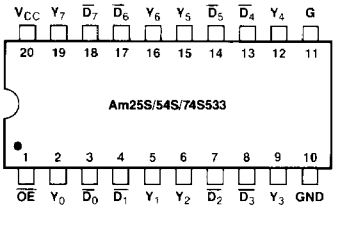

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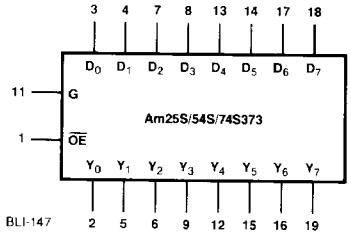
Note: Pin 1 is marked for orientation.

LOGIC SYMBOLS



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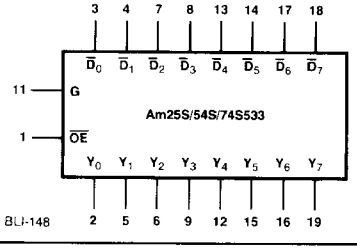

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V_{CC} = Pin 20
GND = Pin 10

Am25S373 • Am25S533

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

Am25S373/533XC, DC, PC	T_A = 0 to 70°C	V_{CC} = 4.75 to 5.25V
Am25S373/533XM, DM	T_A = −55 to +125°C	V_{CC} = 4.50 to 5.50V
Am25S373/533FM	T_C = −55 to +125°C	V_{CC} = 4.50 to 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −2.0mA	2.4	3.4		Volts
			COM'L, I_{OH} = −6.5mA	2.4	3.1		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20mA			.45	Volts
			I_{OL} = 32mA			.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V				−250	μA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX	V_O = 0.5V			−50	μA
			V_O = 2.4V			50	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−40		−100	mA
I_{CC}	Power Supply Current (Note 4) 'S373	V_{CC} = MAX			105	160	mA
	Power Supply Current (Note 4) 'S533				110	168	

Notes:
1. For conditions shown as MIN or MAX use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Inputs grounded; outputs open.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

ORDERING INFORMATION

Package Type	Temperature Range	Am25S373 Order Number	Am54S/74S373 Order Number	Am25S533 Order Number	Am54S/74S533 Order Number
Molded DIP	0 to 70°C	AM25S373PC	SN74S373N	AM25S533PC	SN74S533N
Hermetic DIP	0 to 70°C	AM25S373DC	SN74S373J	AM25S533DC	SN74S533J
Dice	0 to 70°C	AM25S373XC	SN74S373X	AM25S533XC	SN74S533X
Hermetic DIP	−55 to +125°C	AM25S373DM	SN54S373J	AM25S533DM	SN54S533J
Hermetic Flat Pak	−55 to +125°C	AM25S373FM	SN54S373W	AM25S533FM	SN54S533W
Dice	−55 to +125°C	AM25S373XM	SN54S373X	AM25S533XM	SN54S533X

Am54S/74S373 • Am54S/74S533
ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

Am54S/74S373/533XC, DC, PC	T_A = 0 to 70°C	V_{CC} = 4.75 to 5.25V
Am54S/74S373/533XM, DM	T_A = −55 to +125°C	V_{CC} = 4.50 to 5.50V
Am54S/74S373/533FM	T_C = −55 to +125°C	V_{CC} = 4.50 to 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description		Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −2.0mA	2.4	3.4		Volts
				COM'L, I_{OH} = −6.5mA	2.4	3.1		
V_{OL}	Output LOW Voltage		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20mA			0.5	Volts
V_{IH}	Input HIGH Level		Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level		Guaranteed input logical LOW voltage for all inputs	MIL			0.8	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage		V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current		V_{CC} = MAX, V_{IN} = 0.5V				−250	μA
I_{IH}	Input HIGH Current		V_{CC} = MAX, V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current		V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{OZ}	Off-State (High-Impedance) Output Current		V_{CC} = MAX	V_O = 0.5V			−50	μA
				V_O = 2.4V			50	
I_{SC}	Output Short Circuit Current (Note 3)		V_{CC} = MAX		−40		−100	mA
I_{CC}	Power Supply Current (Note 4)	'S373	V_{CC} = MAX			105	160	mA
		'S533				110	168	

Notes:
1. For conditions shown as MIN or MAX use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Inputs grounded; outputs open.

FUNCTION TABLES

Am25S/54S/74S373

Inputs			Internal	Outputs	Function
$\overline{OE}$	G	D_i	Q_i	Y_i	
H	X	X	X	Z	Hi-Z
L	H	L	H	L	Transparent
L	H	H	L	H	
L	L	X	NC	NC	Latched

Am25S/54S/74S533

Inputs			Internal	Outputs	Function
$\overline{OE}$	G	$\overline{D_i}$	Q_i	Y_i	
H	X	X	X	Z	Hi-Z
L	H	L	H	H	Transparent
L	H	H	L	L	
L	L	X	NC	NC	Latched

H = HIGH
L = LOW
X = Don't Care

NC = No Change
Z = High Impedance

DEFINITION OF FUNCTIONAL TERMS

Am25S/54S/74S373

D_i The latch data inputs.

G The latch enable input. The latches are transparent when G is HIGH. Input data is latched on the HIGH-to-LOW transition.

Y_i The 3-state latch outputs.

$\overline{OE}$ The output enable control. When $\overline{OE}$ is LOW, the outputs Y_i are enabled. When $\overline{OE}$ is HIGH, the outputs Y_i are in the high-impedance (off) state.

Am25S/54S/74S533

$\overline{D_i}$ The latch inverting data inputs.

G The latch enable input. The latches are transparent when G is HIGH. Input data is latched on the HIGH-to-LOW transition.

$\overline{Y_i}$ The 3-state latch outputs.

$\overline{OE}$ The output enable control. When $\overline{OE}$ is LOW, the inverted outputs Y_i are enabled. When $\overline{OE}$ is HIGH, the outputs Y_i are in the high-impedance (off) state.

Am25S/54S/74S373
SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Am25S/54S/74S Min	Typ	Max	Units	Test Conditions
t_{PLH}	Enable to Output		7	14	ns	C_L = 15pF, R_L = 280Ω
t_{PHL}			12	18	ns	
t_{PLH}	Data Input to Output		5	9	ns	
t_{PHL}			9	13	ns	
t_s(H)	HIGH Data to Enable	0			ns	
t_s(L)	LOW Data to Enable	0			ns	
t_h(H)	HIGH Data to Enable	10			ns	
t_h(L)	LOW Data to Enable	10			ns	
t_{pwH}	Enable Pulse Width	6			ns	
t_{pwL}		7.3			ns	
t_{ZH}	$\overline{OE}$ to Y_i		8	15	ns	
t_{ZL}			11	18	ns	
t_{HZ}	$\overline{OE}$ to Y_i		6	9	ns	C_L = 5pF, R_L = 280Ω
t_{LZ}			8	12	ns	

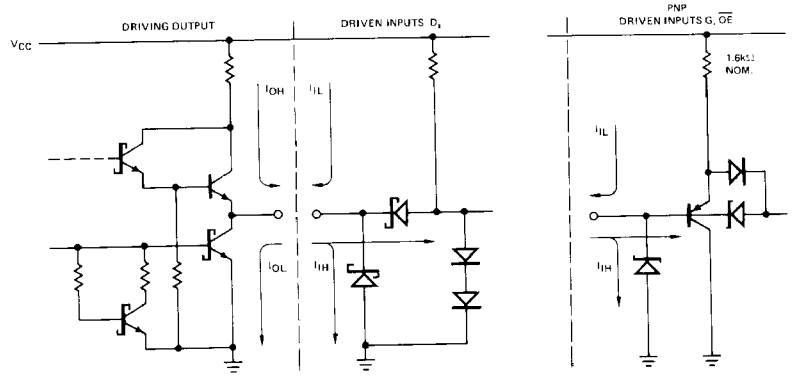
*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am25S/54S/74S533
SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Am25S/54S/74S Min	Typ	Max	Units	Test Conditions
t_{PLH}	Enable to Output		17	24	ns	C_L = 15pF, R_L = 280Ω
t_{PHL}			19	26	ns	
t_{PLH}	Data Input to Output		10	14	ns	
t_{PHL}			14	20	ns	
t_s(H)	HIGH Data to Enable	0			ns	
t_s(L)	LOW Data to Enable	0			ns	
t_h(H)	HIGH Data to Enable	10			ns	
t_h(L)	LOW Data to Enable	10			ns	
t_{pwH}	Enable Pulse Width	6			ns	
t_{pwL}		7.3			ns	
t_{ZH}	$\overline{OE}$ to Y_i		8	15	ns	
t_{ZL}			11	18	ns	
t_{HZ}	$\overline{OE}$ to Y_i		6	9	ns	C_L = 5pF, R_L = 280Ω
t_{LZ}			8	10	ns	

Am25S • Am54S/74S
SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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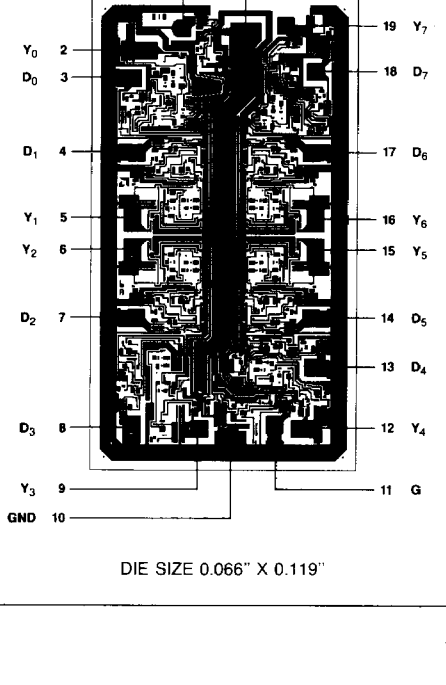
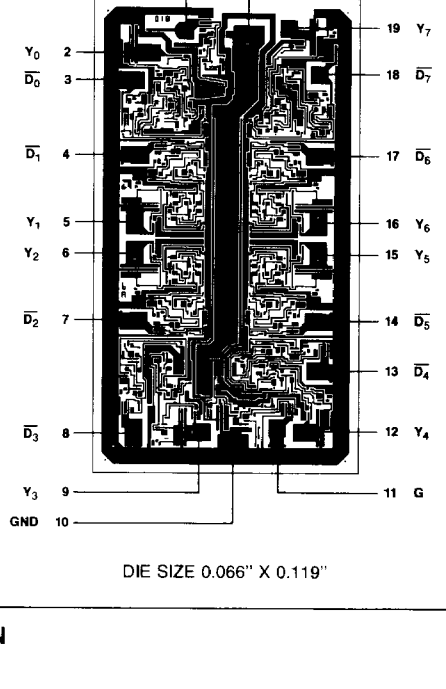
Metallization and Pad Layouts

Am25S/54S/74S373



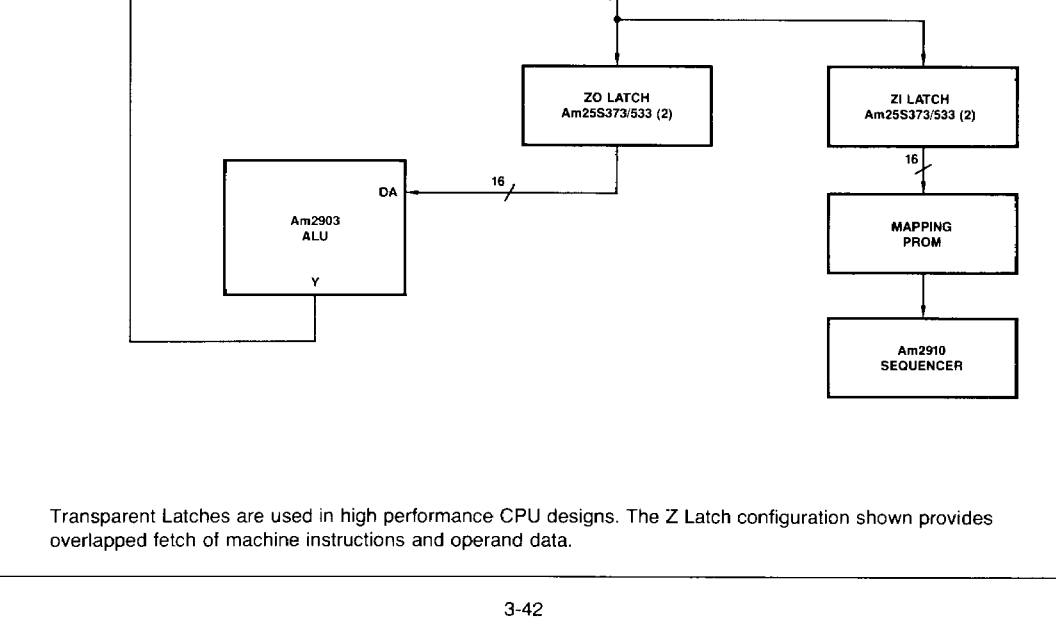
DIE SIZE 0.066" X 0.119"

Am25S/54S/74S533



DIE SIZE 0.066" X 0.119"

APPLICATION



Transparent Latches are used in high performance CPU designs. The Z Latch configuration shown provides overlapped fetch of machine instructions and operand data.

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