

GaAs DPDT Diversity Switch 4.5 - 6.0 GHz

**MASWSS0039
V2**

Features

- Low Insertion Loss: 0.8 dB at 5.2 GHz
- Low Cost 3 mm 12-Lead PQFN Package
- Ideal for WLAN IEEE 802.11a
- 0.5 micron GaAs PHEMT Process
- Integrated DC Blocking Capacitors

Description

M/A-COM's MASWSS0039 is a GaAs PHEMT MMIC DPDT diversity switch in a low cost 3 mm 12-lead PQFN package. It is designed for low insertion loss and allows for independent control and selection of each switch path. It integrates blocking capacitors on all RF ports and thus eliminates the need for additional off-chip DC blocking capacitors.

The MASWSS0039 is ideally suited for applications where very small size and low cost are required. Typical applications are for WLAN IEEE 802.11a systems that employ two antennas for transmit and receive diversity. This part can be used in all systems operating between 4.5 GHz and 6.0 GHz requiring moderate power and diversity switching.

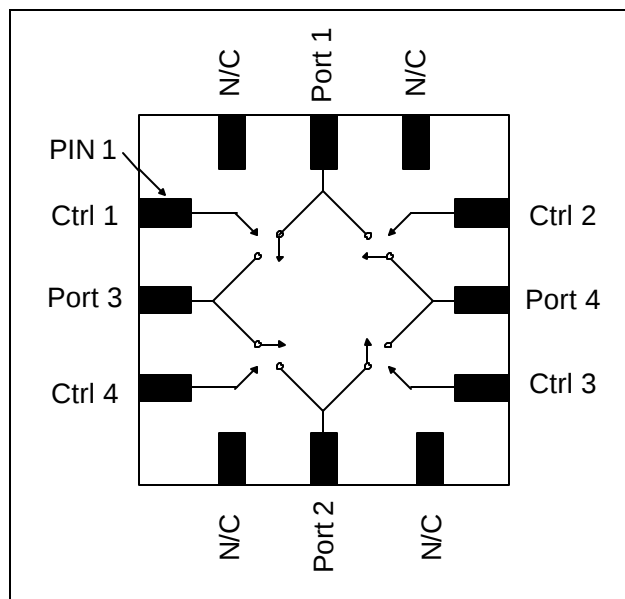
The MASWSS0039 is fabricated using a 0.5 micron gate length GaAs PHEMT process. The process features full passivation for performance and reliability.

Ordering Information

Part Number	Package
MASWSS0039TR	7 inch, 1000 Piece Reel
MASWSS0039TR-3000	13 Inch, 3000 Piece Reel
MASWSS0039SMB	Sample Test Board

Note: Reference Application Note M513 for reel size information.

Functional Schematic



Pin Configuration¹

PIN No.	PIN Name	Description
1	Ctrl 1	Control 1
2	Port 3	RF Port 3
3	Ctrl 4	Control 4
4	N/C	No Connection
5	Port 2	RF Port 2
6	N/C	No Connection
7	Ctrl 3	Control 3
8	Port 4	RF Port 4
9	Ctrl 2	Control 2
10	N/C	No Connection
11	Port 1	RF Port 1
12	N/C	No Connection
13	Paddle ¹	RF and DC Ground

1. The exposed pad centered on the package bottom must be connected to RF and DC ground.

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Electrical Specifications: $T_A = 25^\circ\text{C}$, $Z_0 = 50\ \Omega$, $V_C = 0\ \text{V} / 3\ \text{V}$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Insertion Loss	4.9 GHz	dB	—	0.9	1.3
	5.2 GHz	dB	—	0.8	1.2
	5.8 GHz	dB	—	0.8	1.2
Isolation	4.9 GHz	dB	15	20	—
	5.2 GHz	dB	20	25	—
	5.8 GHz	dB	20	29	—
Return Loss	4.5 - 6.0 GHz	dB	15	25	—
P1dB	5.2 GHz, $V_C = 2.7\ \text{V}$	dBm	—	31	—
	5.2 GHz, $V_C = 3.0\ \text{V}$	dBm	—	33	—
	5.2 GHz, $V_C = 5.0\ \text{V}$	dBm	—	39	—
IP2	Two Tone, +15 dBm / tone, 5 MHz Spacing 5.2 GHz	dBm	—	98	—
IP3	Two Tone, +15 dBm / tone, 5 MHz Spacing 5.2 GHz, $V_C = 3\ \text{V}$	dBm	—	52	—
	5.2 GHz, $V_C = 5\ \text{V}$	dBm	—	55	—
2 nd Harmonic	5.2 GHz, $P_{IN} = 20\ \text{dBm}$	dBc	—	-85	—
3 rd Harmonic	5.2 GHz, $P_{IN} = 20\ \text{dBm}$	dBc	—	-83	—
Trise, Tfall	10% to 90% RF and 90% to 10% RF	nS	—	20	—
Ton, Toff	50% Control to 90% RF	nS	—	35	—
	50% Control to 10% RF	nS	—	40	—
Control Current	$ V_C = 3\ \text{V}$	μA	—	5	25

Absolute Maximum Ratings ²

Parameter	Absolute Maximum
Input Power @ 3 V Control	+32 dBm
Input Power @ 5 V Control	+36 dBm
Operating Voltage	+8.5 volts
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

2. Exceeding any one or combination of these limits may cause permanent damage to this device.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

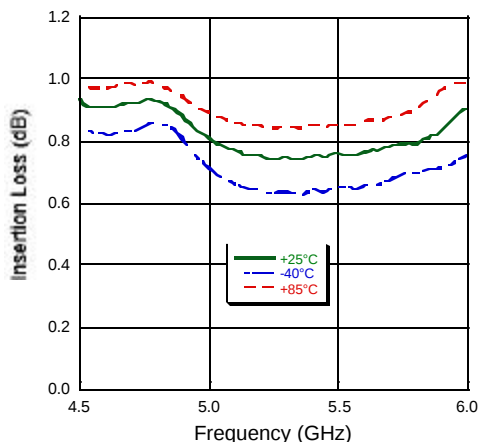
Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

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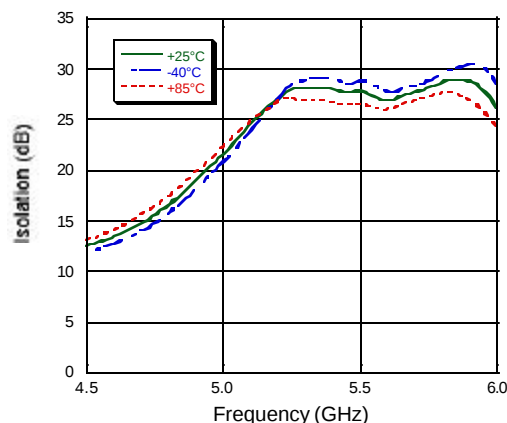
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Typical Performance Curves

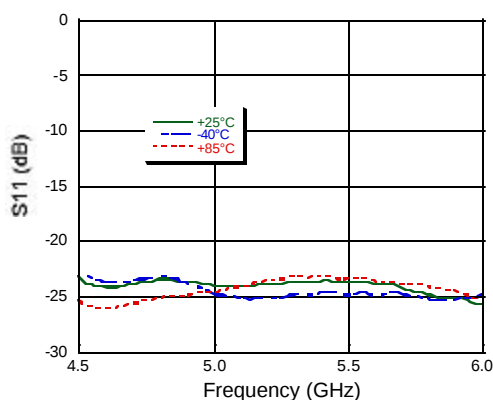
Insertion Loss



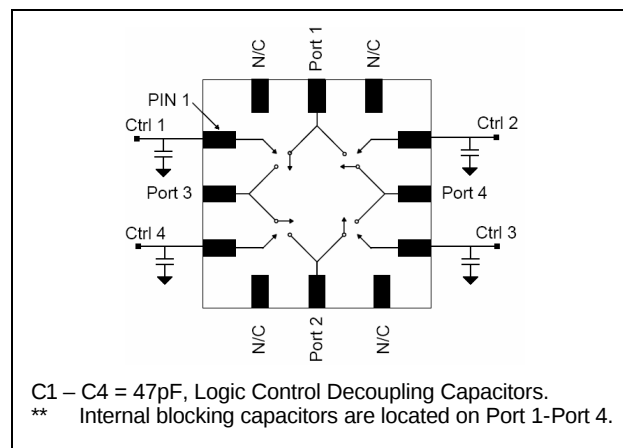
Isolation



Return Loss



Circuit Block Diagram



Truth Table ^{3,4}

Control V1	Control V2	Control V3	Control V4	Port 1 - Port 3	Port 1 - Port 4	Port 2 - Port 4	Port 2 - Port 3
1	0	0	0	On	Off	Off	Off
0	1	0	0	Off	On	Off	Off
0	0	1	0	Off	Off	On	Off
0	0	0	1	Off	Off	Off	On
1	0	1	0	On	Off	On	Off
0	1	0	1	Off	On	Off	On

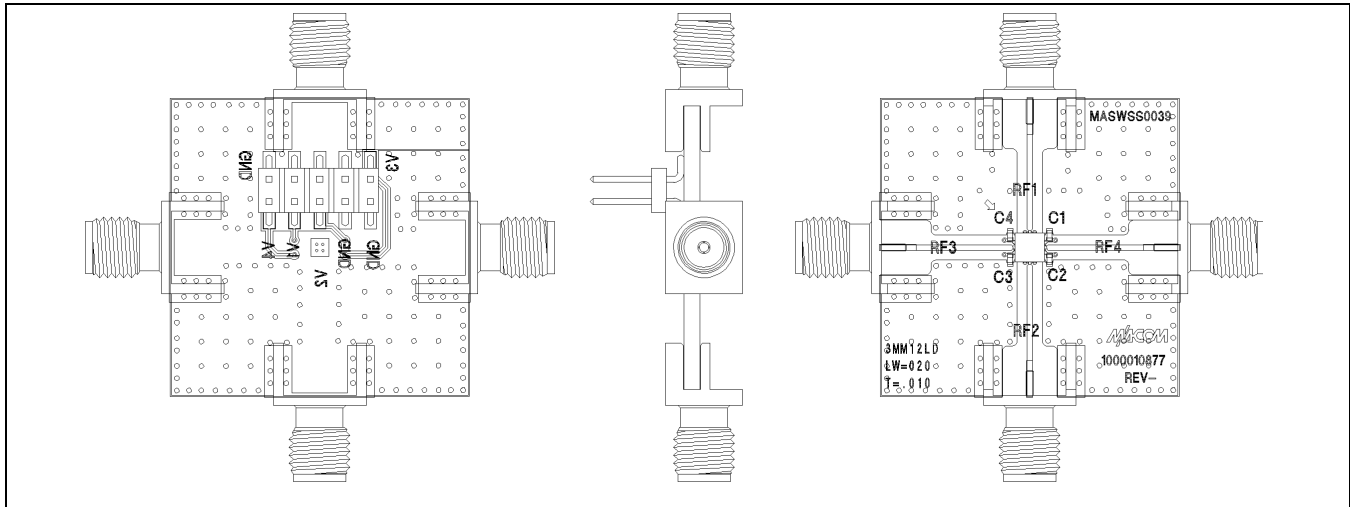
3. 1 = +2.5 V to +5 V, 0 = 0 V ± 0.2 V.

4. Differential voltage, V (state 1) - V (state 0), must be 2.5 V minimum and must not exceed 8 V.

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Evaluation Board



3 mm 12-Lead PQFN

