MCM511001A

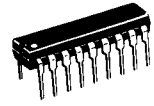
1M × 1 CMOS Dynamic RAM
Nibble Mode

2

The MCM511001A is a 1.0μ CMOS high-speed, dynamic random access memory. It is organized as 1,048,576 one-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost. The fast nibble mode feature allows high-speed serial access of up to 4 bits of data.

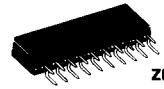
The MCM511001A requires only 10 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 300-mil dual-in-line plastic package (DIP), a 300-mil SOJ plastic package, and a 100-mil zig-zag in-line plastic package (ZIP).

- Three-State Data Output
- Common I/O with Early Write
- Fast Nibble Mode
- Test Mode
- TTL-Compatible Inputs and Output
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle, 8 ms Refresh
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (tRAC): MCM511001A-70 = 70 ns (Maximum)
  MCM511001A-80 = 80 ns (Maximum)
  MCM511001A-10 = 100 ns (Maximum)
- Low Active Power Dissipation: MCM511001A-70 = 440 mW (Maximum)
  MCM511001A-80 = 385 mW (Maximum)
  MCM511001A-10 = 330 mW (Maximum)
- Low Standby Power Dissipation: 11 mW (Maximum, TTL Levels)
  5.5 mW (Maximum, CMOS Levels)



P PACKAGE
300 MIL PLASTIC
CASE 707A

J PACKAGE
300 MIL SOJ
CASE 822

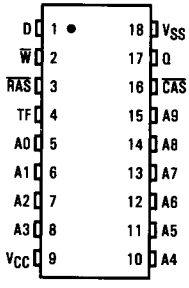


Z PACKAGE
PLASTIC
ZIG-ZAG IN-LINE
CASE 836

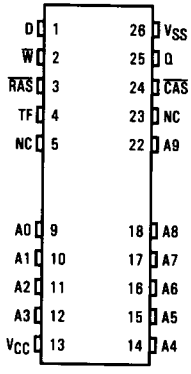
PIN NAMES	
A0-A9	Address Input
D	Data Input
Q	Data Output
$\overline{W}$	Read/Write Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground
TF	Test Function Enable
NC	No Connection

PIN ASSIGNMENT

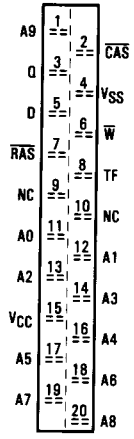
DUAL-IN-LINE



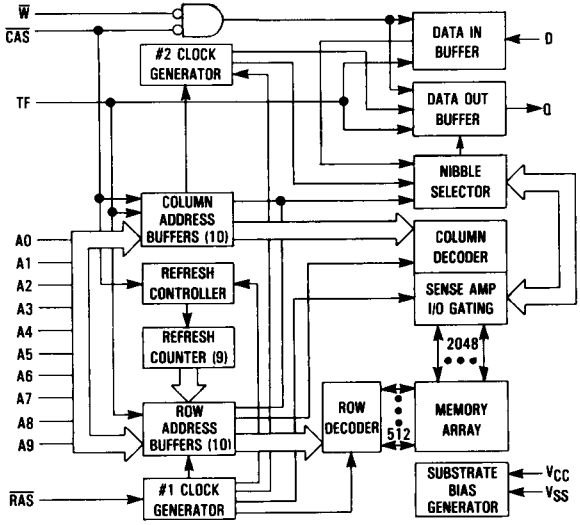
SMALL OUTLINE



ZIG-ZAG IN-LINE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Test Function Input Voltage	$V_{in(TF)}$	−1 to +10.5	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	–	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	−1.0	–	0.8	V	1
Test Function Input High Voltage	$V_{IH\ (TF)}$	V_{CC} + 4.5	–	10.5	V	1

2

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM511001A-70, t_{RC} = 130 ns		–	80		
MCM511001A-80, t_{RC} = 150 ns		–	70		
MCM511001A-10, t_{RC} = 180 ns		–	60		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CAS}$ = V_{IH})	I_{CC3}			mA	2
MCM511001A-70, t_{RC} = 130 ns		–	80		
MCM511001A-80, t_{RC} = 150 ns		–	70		
MCM511001A-10, t_{RC} = 180 ns		–	60		
V_{CC} Power Supply Current During Nibble Mode Cycle ($\overline{RAS}$ = V_{IL})	I_{CC4}			mA	2
MCM511001A-70, t_{NC} = 35 ns		–	60		
MCM511001A-80, t_{NC} = 35 ns		–	50		
MCM511001A-10, t_{NC} = 40 ns		–	40		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2 V)	I_{CC5}	–	1.0	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	2
MCM511001A-70, t_{RC} = 130 ns		–	80		
MCM511001A-80, t_{RC} = 150 ns		–	70		
MCM511001A-10, t_{RC} = 180 ns		–	60		
Input Leakage Current (Except TF) (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	−10	10	μA	
Input Leakage Current (TF) (0 V ≤ $V_{in(TF)}$ ≤ V_{CC} + 0.5 V)	$I_{lkg(I)}$	−10	10	μA	
Output Leakage Current ($\overline{CAS}$ = V_{IH}, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	−10	10	μA	
Test Function Input Current (V_{CC} + 4.5 V ≤ $V_{in(TF)}$ ≤ 10.5 V)	$I_{in(TF)}$	–	1	mA	
Output High Voltage (I_{OH} = −5 mA)	V_{OH}	2.4	–	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	–	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0-A9, D	C_{in}	5	pF	3
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, TF		7	pF	3
Output Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	Q	C_{out}	7	pF	3

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM511001A-70		MCM511001A-80		MCM511001A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	–	150	–	180	–	ns	6
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	155	–	175	–	210	–	ns	6
Nibble Mode Cycle Time	t_{CEHCEH}	t_{NC}	35	–	35	–	40	–	ns	
Nibble Mode Read-Write Cycle Time	t_{CEHCEH}	t_{NRMW}	55	–	55	–	65	–	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	–	70	–	80	–	100	ns	7, 8
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	–	20	–	20	–	25	ns	7, 9
Access Time from Column Address	t_{AVQV}	t_{AA}	–	35	–	40	–	50	ns	7, 10
Nibble Mode Access Time	t_{CELQV}	t_{NCAC}	–	15	–	15	–	20	ns	7
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	–	0	–	0	–	ns	7
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	11
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	50	–	60	–	70	–	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	–	20	–	25	–	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	70	–	80	–	100	–	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	25	75	ns	12
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	13
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	–	5	–	5	–	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	–	10	–	10	–	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	–	10	–	15	–	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	–	15	–	20	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	55	–	60	–	75	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	35	–	40	–	50	–	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The TF pin must be at V_{IL} or open if not used.
6. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a current load equivalent to 2 TTL (−200 µA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
11. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

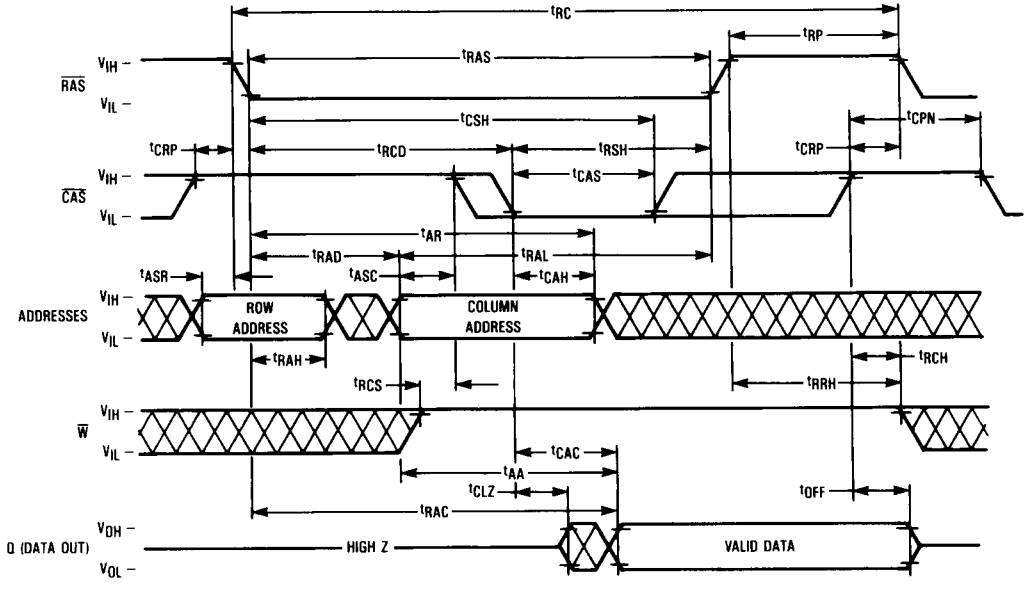
READ, WRITE, AND READ-WRITE CYCLES (Continued)

Parameter	Symbol		MCM511001A-70		MCM511001A-80		MCM511001A-10		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	–	0	–	0	–	ns	14
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	–	0	–	0	–	ns	14
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	–	15	–	20	–	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	55	–	60	–	75	–	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	–	15	–	20	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	–	20	–	25	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	–	20	–	25	–	ns	
Data In Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	0	–	ns	15
Data In Hold Time	t_{CELDX}	t_{DH}	15	–	15	–	20	–	ns	15
Data In Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	55	–	60	–	75	–	ns	
Refresh Period	t_{RVRV}	t_{RFSH}	–	8	–	8	–	8	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	–	0	–	0	–	ns	16
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	20	–	20	–	25	–	ns	16
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	70	–	80	–	100	–	ns	16
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	35	–	40	–	50	–	ns	16
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	–	30	–	30	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	–	0	–	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	–	40	–	50	–	ns	
Nibble Mode Pulse Width	t_{CELCEH}	t_{NCAS}	15	–	15	–	20	–	ns	
Nibble Mode $\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{NCP}	10	–	10	–	10	–	ns	
Nibble Mode $\overline{RAS}$ Hold Time	t_{CELREH}	t_{NRSH}	15	–	15	–	20	–	ns	
Nibble Mode $\overline{CAS}$ to Write Delay Time	t_{CELWL}	t_{NCWD}	15	–	15	–	20	–	ns	
Nibble Mode Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{NRWL}	15	–	15	–	20	–	ns	
Nibble Mode Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{NCWL}	15	–	15	–	20	–	ns	
Test Mode Enable Setup Time Referenced to $\overline{RAS}$	t_{TEHREL}	t_{TES}	0	–	0	–	0	–	ns	
Test Mode Enable Hold Time Referenced to $\overline{RAS}$	t_{REHTEL}	t_{TEHR}	0	–	0	–	0	–	ns	
Test Mode Enable Hold Time Referenced to $\overline{CAS}$	t_{CEHTEL}	t_{TEHC}	0	–	0	–	0	–	ns	

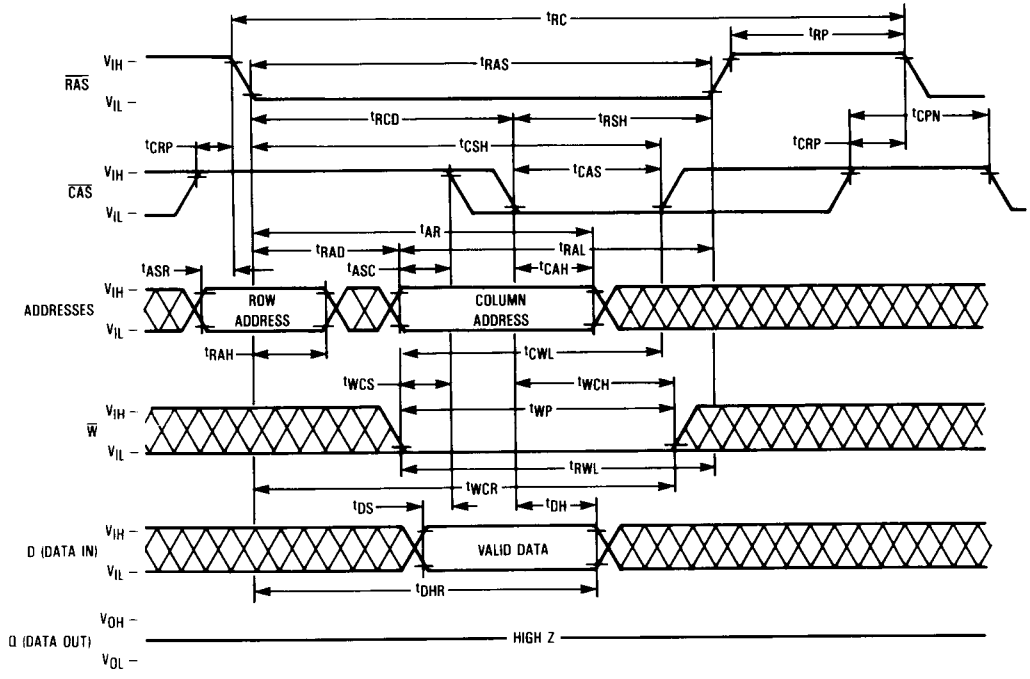
NOTES:

14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{W}$ leading edge in delayed write or read-write cycles.
16. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

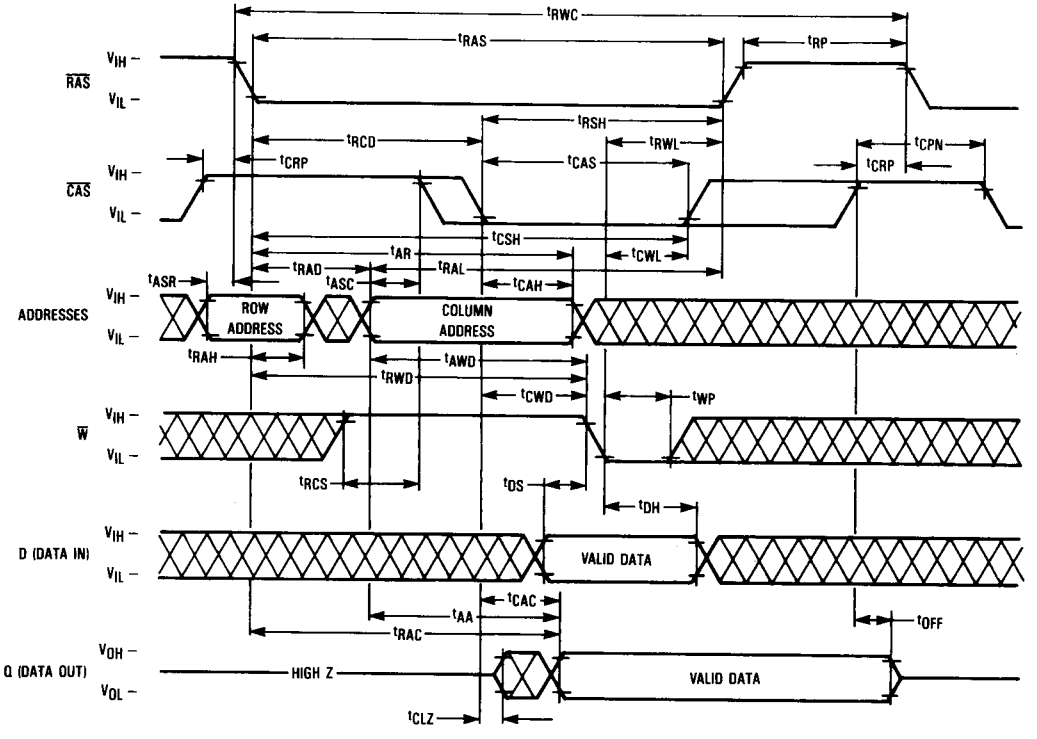
READ CYCLE



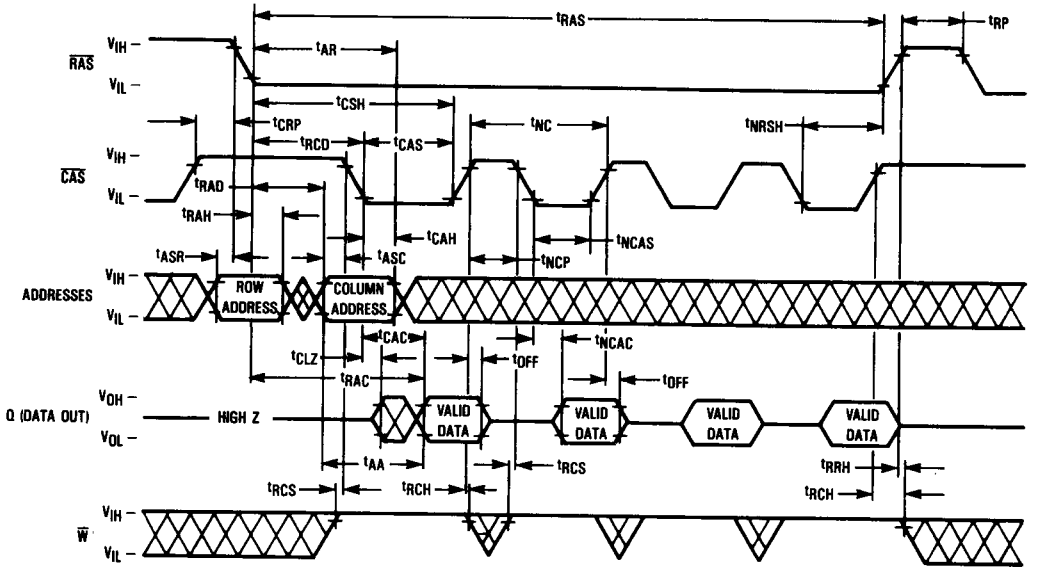
EARLY WRITE CYCLE



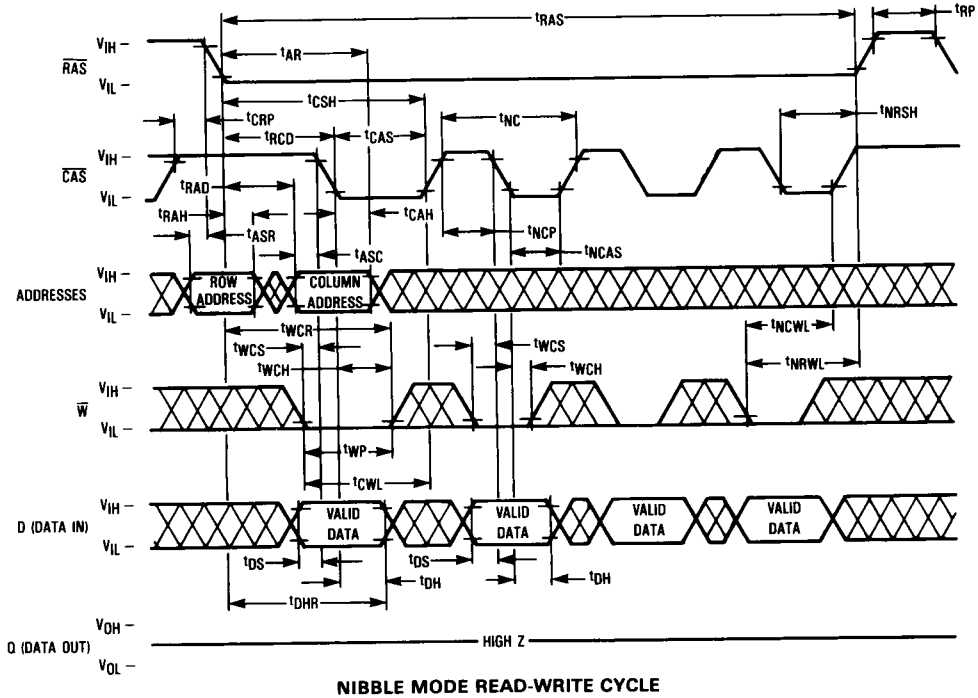
READ-WRITE CYCLE



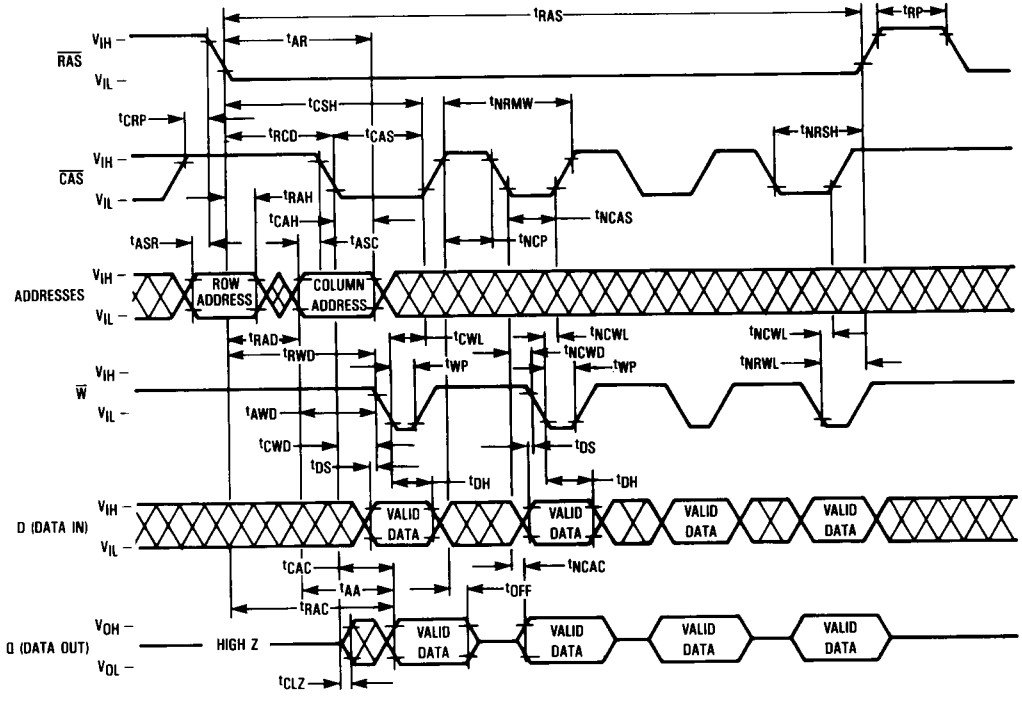
NIBBLE MODE READ CYCLE



NIBBLE MODE EARLY WRITE CYCLE

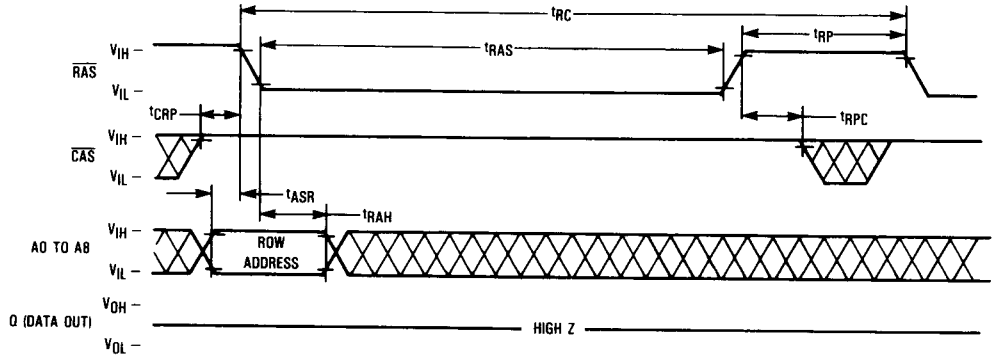


NIBBLE MODE READ-WRITE CYCLE



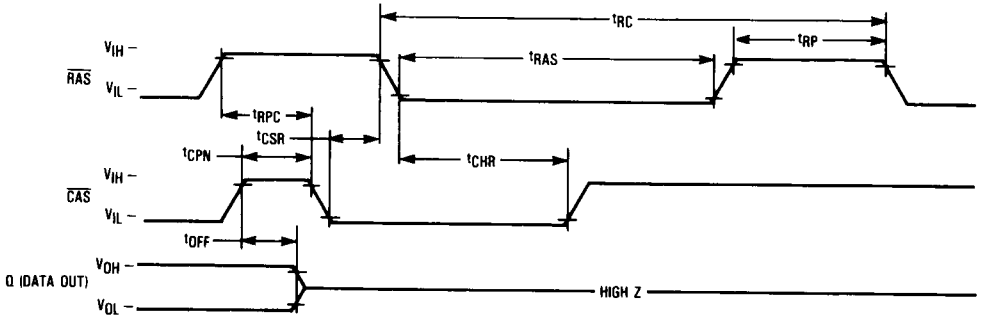
$\overline{RAS}$ ONLY REFRESH CYCLE

($\overline{W}$ and A9 are Don't Care)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

($\overline{W}$ and A0 to A9 are Don't Care)



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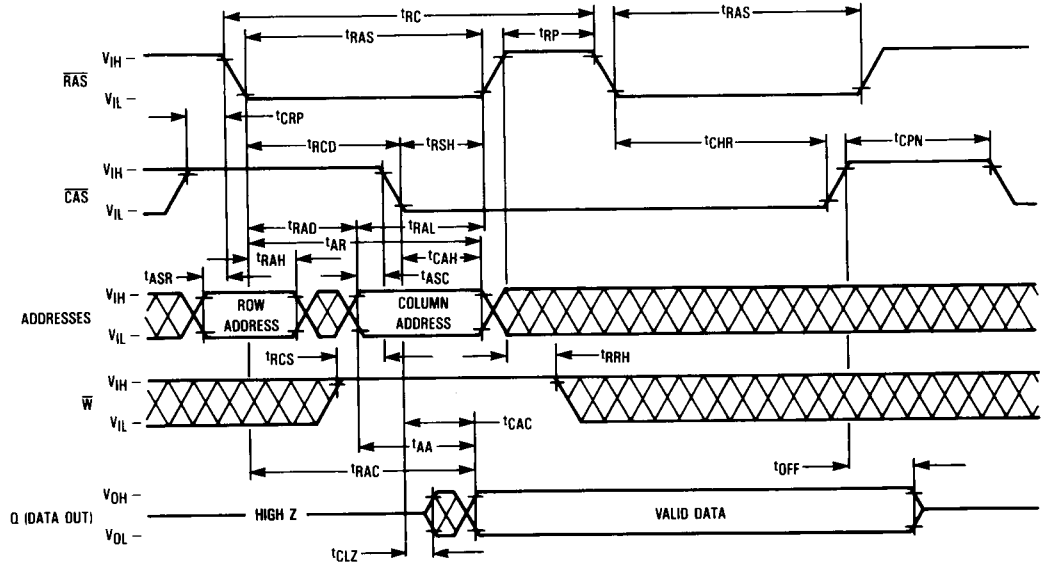
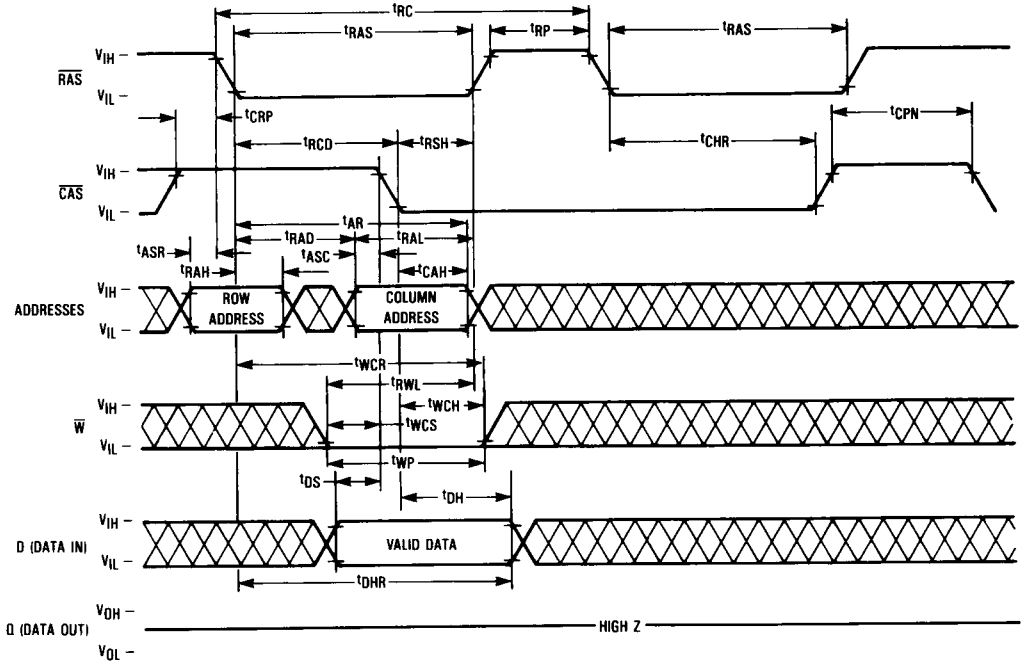
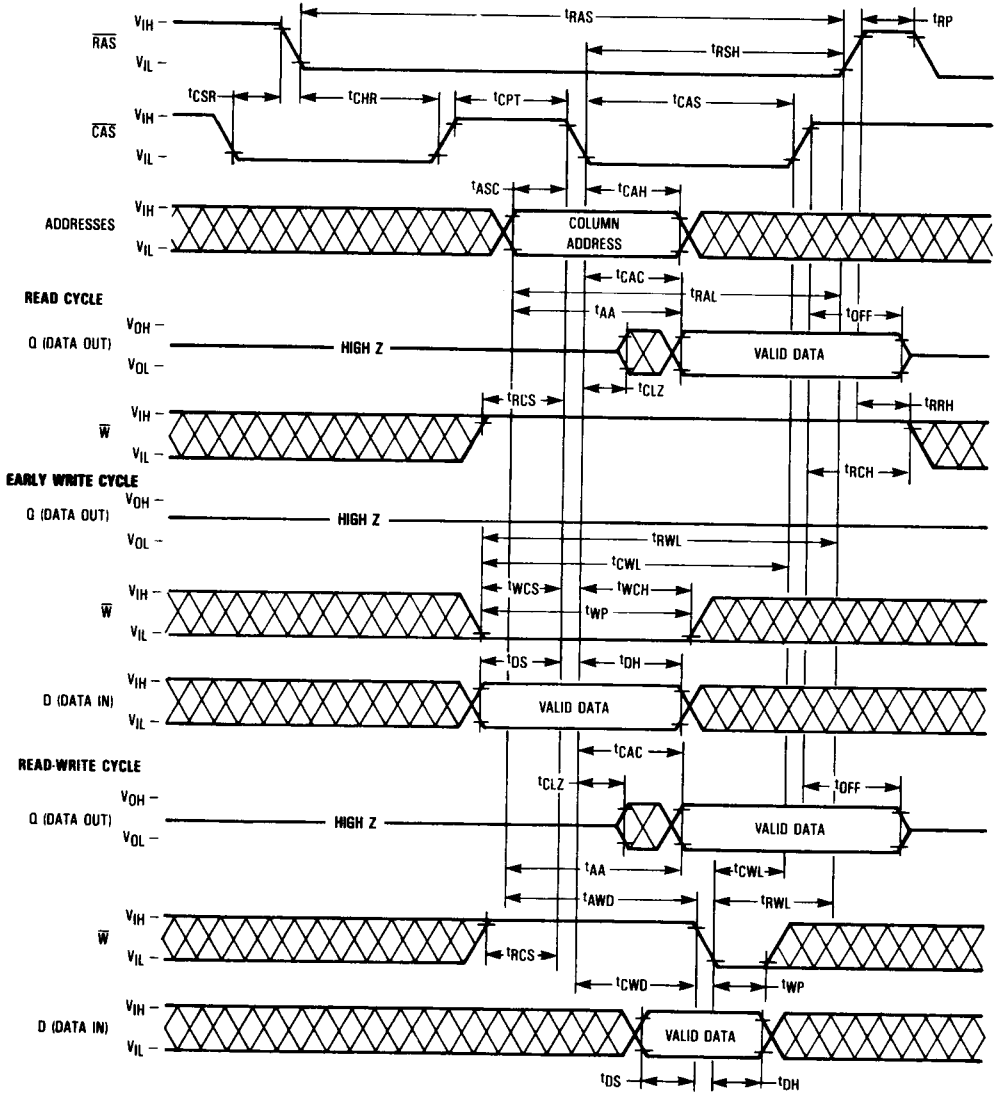
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (EARLY WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to assure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 bit locations in the device. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This "gate" feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are two other variations in addressing the 1M RAM: **$\overline{RAS}$ only refresh cycle** and **$\overline{CAS}$ before $\overline{RAS}$ refresh cycle**. Both are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, nibble mode read cycle, read-write cycle, and nibble mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. However, $\overline{CAS}$ must be active before or at t_{RCD} maximum to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{RAS}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{CAS}$ clock active transition (t_{CAC}).

The $\overline{RAS}$ and $\overline{CAS}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS} respectively, to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CAS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{CAS}$ clock is active. When the $\overline{CAS}$ clock transitions to inactive, the output will switch to High Z (three-state).

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, nibble mode early write, and nibble mode read-write. Early and late write modes are discussed here, while nibble mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{W}$, with respect to $\overline{CAS}$. Minimum active times t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Data in (D) is referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because $\overline{W}$ active transition precedes or coincides with $\overline{CAS}$ active transition, keeping data-out buffers disabled. This feature can be utilized on systems with a common I/O bus, provided all writes are performed with early write cycles, to prevent bus contention.

A late write cycle occurs when $\overline{W}$ active transition is made after $\overline{CAS}$ active transition. $\overline{W}$ active transition could be delayed for almost 10 microseconds after $\overline{CAS}$ active transition, $(t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL} and t_T) are maintained. D is referenced to $\overline{W}$ active transition in a late write cycle. Output buffers are enabled by $\overline{CAS}$ active transition but Q may be indeterminate — see note 16 of AC operating conditions table. $\overline{RAS}$ and $\overline{CAS}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{W}$ active transition to complete the write cycle.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{W}$ must remain high for t_{CWD} minimum after the $\overline{CAS}$ active transition, to guarantee valid Q before writing the bit.

NIBBLE MODE CYCLES

Nibble mode allows fast successive serial data operations at two, three, or four bits of the 1M dynamic RAM. Read access time in nibble mode (t_{NCAC}) is considerably faster than the regular $\overline{RAS}$ clock access time t_{RAC}. Nibble mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The address of the first nibble bit is latched by $\overline{RAS}$ and $\overline{CAS}$ active transitions. Each subsequent $\overline{CAS}$ active transition increments the row and column addresses internally to access the next bit in binary fashion. After the fourth bit is accessed, the nibble pattern repeats itself: (0,0) (0,1) (1,0) (1,1) (0,0) (0,1) (1,0) (1,1) . . . . The A10 address determines the starting point of the 4-bit nibble, with row address A10 the least significant of the (column, row) ordered

pair. External addresses are ignored after the first nibble bit is selected.

A nibble mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum of t_{NCP}, while $\overline{RAS}$ remains low (V_{IL}). The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first nibble mode cycle (t_{NC} or t_{NRMW}). Either a read, write, or read-write operation can be performed in a nibble mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive nibble mode cycles and performed in any order. The maximum number of consecutive nibble mode cycles is limited by t_{RAS}. Nibble mode operation ends when $\overline{RAS}$ transitions to inactive, coincident with or following a $\overline{CAS}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature, thus each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM511001A require refresh every 8 milliseconds.

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM511001A. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds.

A normal read, write, or read-write operation to the RAM will refresh all the bits (2048) associated with the particular row decoded. Three other methods of refresh, **$\overline{RAS}$-only refresh**, **$\overline{CAS}$ before $\overline{RAS}$ refresh**, and **hidden refresh** are available on this device for greater system flexibility.

$\overline{RAS}$-Only Refresh

$\overline{RAS}$-only refresh consists of $\overline{RAS}$ transition to active, latching the row address to be refreshed, while $\overline{CAS}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

$\overline{CAS}$ before $\overline{RAS}$ refresh is enabled by bringing $\overline{CAS}$ active before $\overline{RAS}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{CAS}$ active at the end of a read or write cycle, while $\overline{RAS}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{CAS}$ before $\overline{RAS}$ refresh from a cycle in progress (see Figure 1).

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 512 cycles, as indicated by the check data written in each row. See **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read-write cycle**. Repeat this operation 512 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into the cell by performing the **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read-write cycle**. Repeat this operation 512 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

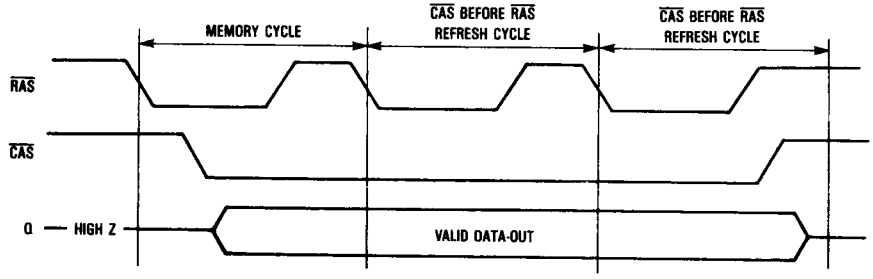


Figure 1. Hidden Refresh Cycle

TEST MODE

Internal organization of this device (256K × 4) allows it to be tested as if it were a 256K × 1 DRAM. Only nine of the ten addresses (A0–A8) are used in test mode; A9 is internally disabled. A test mode write cycle writes data, D (data in), to a bit in each of the four 256K × 1 blocks (B0–B3), in parallel. A test mode read cycle reads a bit in each of the four blocks. If data is the same in all four bits, Q (data out) is the same as the data in each bit. If data is not the same in all four bits, Q is high Z. See truth table and block diagram.

Test mode can be used in any timing cycle except nibble mode cycles. The test mode function is enabled by holding the "TF" pin on "super voltage" for the specified period (t_{TES}, t_{TEHR}, t_{TEHC}; see TEST MODE CYCLE).

"Super voltage" = V_{CC} + 4.5 V

where

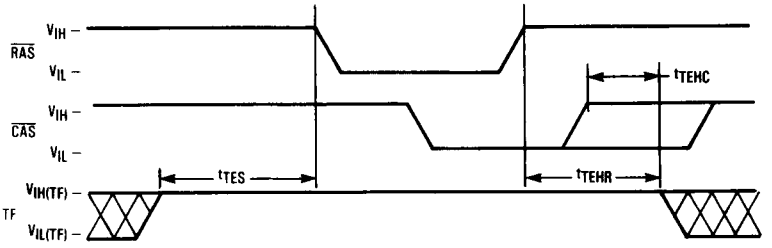
4.5 V < V_{CC} < 5.5 V and maximum voltage = 10.5 V.

A9 is ignored in test mode. In normal operation, the "TF" pin must either be connected to V_{IL}, or left open.

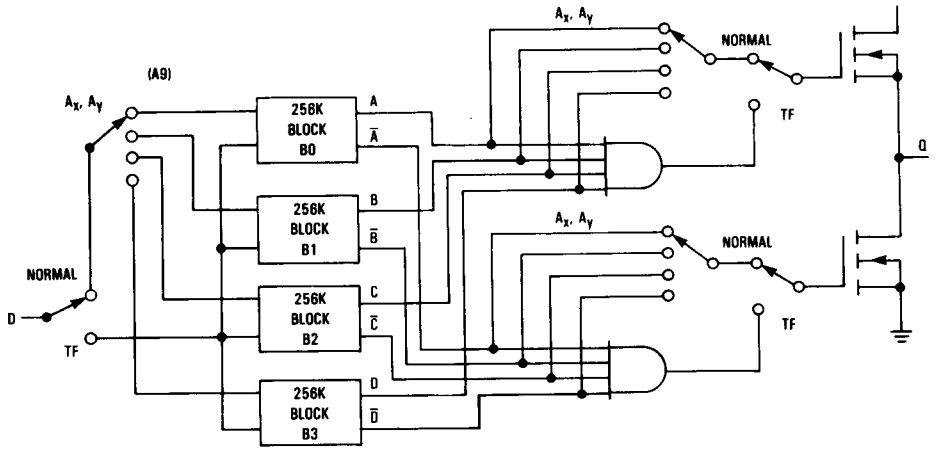
Test Mode Truth Table

D	B0	B1	B2	B3	Q
0	0	0	0	0	0
1	1	1	1	1	1
–	Any Other				High-Z

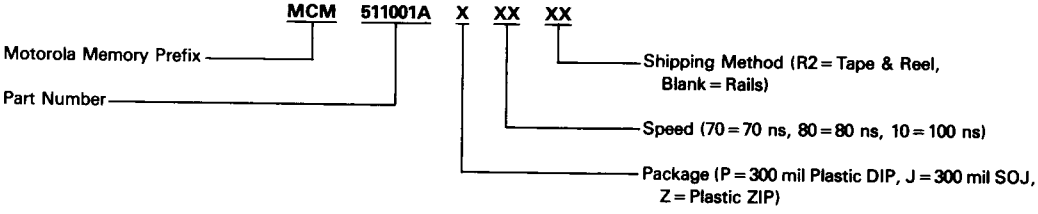
TEST MODE CYCLE



TEST FUNCTION BLOCK DIAGRAM



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—	MCM511001AP70	MCM511001AJ70	MCM511001AJ70R2	MCM511001AZ70
	MCM511001AP80	MCM511001AJ80	MCM511001AJ80R2	MCM511001AZ80
	MCM511001AP10	MCM511001AJ10	MCM511001AJ10R2	MCM511001AZ10

NOTE: For mechanical data, please see Chapter 10.