VITESSE

VSC8223
Datasheet

Extended Multirate STS-12/STM-4, STS-3/STM-1 and FEC Clock and Data Recovery IC

FEATURES

- Extended multirate clock and data recovery support for STS-12/STM-4, STS-3/STM-1, and FEC data rates
- Complies with Bellcore and ITU-T specifications for jitter tolerance, transfer, and generation
- Status indication signals (LVTTL) for:
  Loss of signal (LOS)
  Loss of lock (LOL)
  No reference (NOREF)
- Automatic and manual lock-to-reference modes
- On-die input and output termination
- Selectable high-speed clock output
- Selectable LVPECL reference frequencies: 19.44 MHz, 77.76 MHz, or 155.52 MHz (or FEC)
- Internal phase-locked loop maintains clock output in the absence of data
- Low power CMOS technology
- 2.5 V supply operation
- 0.4 W typical power dissipation
- 48-pin LQFP package

GENERAL DESCRIPTION

The VSC8223 device is a high-performance, extended multirate clock and data recovery (CDR) IC that supports SONET/SDH systems operating at STS-12/STM-4, STS-3/STM-1, and forward error correction (FEC) data rates. The VSC8223 generates a differential bit clock and differential retimed data.

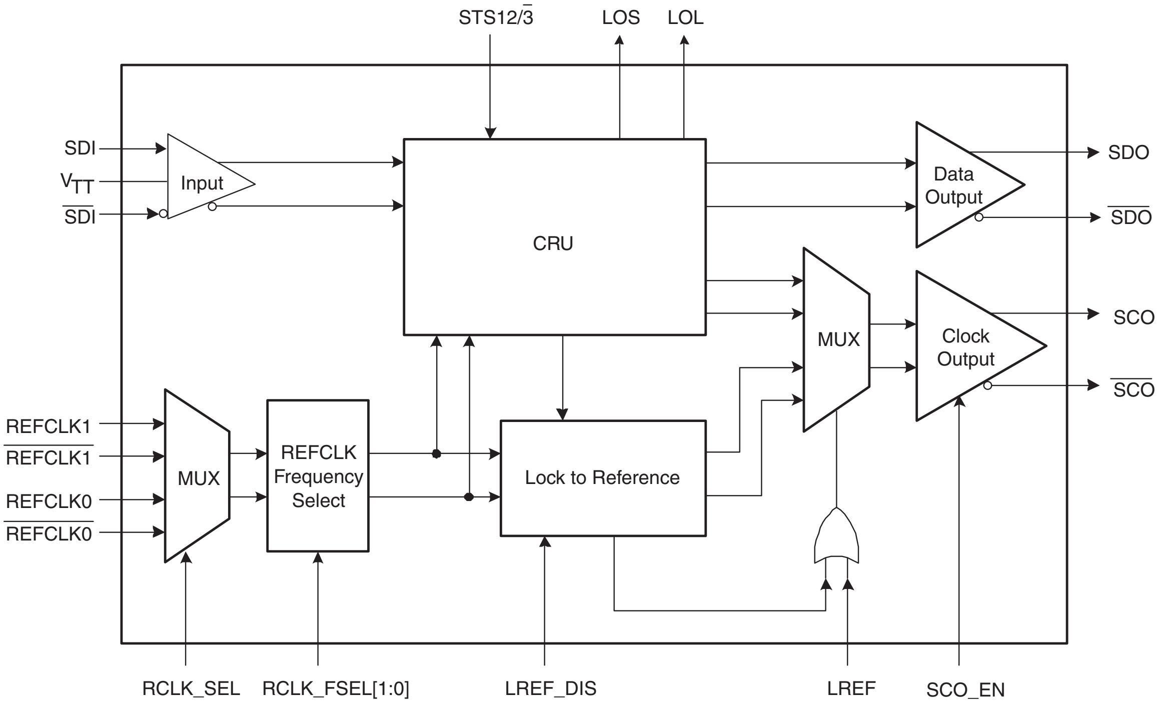
High-speed input and output signals are terminated on-chip to maintain the highest degree of signal integrity possible. Two selectable, externally supplied reference clock (REFCLK[1:0]) inputs support the phase-locked loop (PLL) operation and are used to maintain a lock condition when the high-speed data is missing at the input. A reference clock selector (RCLK_SEL) input allows the user to select between either of the two REFCLK inputs. The reference clock frequency (155.52 MHz, 77.76 MHz, 19.44 MHz or FEC) to the VSC8223 is selected using the RCLK_FSEL[1:0] control signals.

The loss of lock (LOL) status signal indicates the loss of lock of the PLL. The loss of signal (LOS) status signal indicates the occurrence of an all zeros or all ones pattern. During a LOS condition, an all zeros data pattern is output along with a SONET/SDH-quality clock (for SONET/SDH rates only).

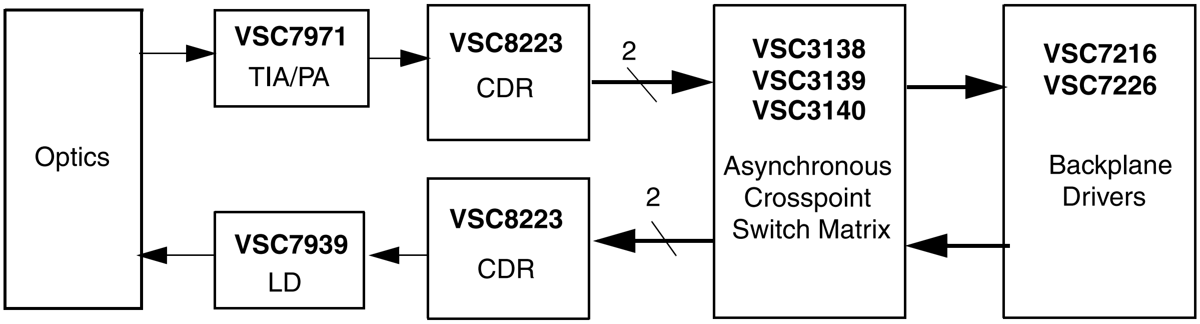
During LOS conditions, the PLL automatically switches to the REFCLK. The PLL automatically switches back to the high-speed input when the LOS signal is de-asserted. The PLL can also be manually forced into the lock to REFCLK mode using the LREF control pin. In addition, the automatic lock to REFCLK mode can be disabled.

The VSC8223 device is available in a plastic, low-profile quad flat package (LQFP) with an exposed pad and a 7 mm × 7 mm body. The device is also available in a lead(Pb)-free package, VSC8223XRV.

Block Diagram



System-Level Block Diagram



REVISION HISTORY

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

Revision 4.0

Revision 4.0 of this datasheet was published in July 2007. The following is a summary of the changes implemented in the datasheet:

- The device is now available in a lead(Pb)-free package.
- ESD and moisture sensitivity specifications were added. For more information, see “Stress Ratings,” page 19 and “Moisture Sensitivity,” page 25.
- The thermal specifications were updated. For more information, see “Thermal Specifications,” page 25.
- The system-level block diagram was updated to reference new products. The LVPECL input terminations diagram was also updated. For more information, see “System-Level Block Diagram,” page 2 and “LVPECL Input Terminations,” page 7.
- For the supported upper and lower data ranges, the lower data range for HIGH (1) was changed from 150 Mbps to 155 Mbps and the lower data range for LOW (0) was changed from 600 Mbps to 622 Mbps.
- The recommended REFCLK input frequencies for STS-12/-3 FEC were updated. For more information, see Table 6, page 10.
- The conditions for the jitter tolerance and jitter transfer bandwidth parameters were updated to include LBW [1:0] = 0, 0.
- The maximum values for the CRU lock time (synchronous and asynchronous switch) parameters were changed to typical values.
- The operating temperature parameter was clarified as ambient to case and the minimum value was changed from –40 °C to –20 °C.
- The minimum values for the power supply current parameters were updated and the power supply requirements table (formerly table 17) was integrated with the recommended operating conditions. For more information, see “Recommended Operating Conditions,” page 19.
- In the electrical specifications section, the voltage input swing (single-ended drive), input high voltage, REFCLK input duty cycle, input HIGH current, input LOW current, and case temperature parameters were removed.
- Errata information was also removed.

Revision 2.0

Revision 2.0 of this datasheet was published in October 2002. This was the first publication of the document.

FUNCTIONAL DESCRIPTION

The VSC8223 extended multirate CDR consists of the following functional blocks:

- High-speed data inputs
- High-speed clock and data outputs
- Low-speed REFCLK LVPECL inputs
- Static LVTTL control inputs
- Static LVTTL status outputs
- Clock and data recovery unit (CRU)
- LOCK to REFCLK unit
- Power and ground

High-Speed Data Inputs (SDI/$\overline{\text{SDI}}$)

The VSC8223 high-speed data input stage provides the following features:

- On-die 100 Ω termination resistance using two series 50 Ω resistors, with the internal junction of the two resistors accessible on an external pin V_{TT}
- AC-coupled operation
- DC-coupled operation (input common-mode voltages must be taken into account)
- Single-ended input operation
- Differential input operation

The high-speed input receivers are terminated on-chip to 50 Ω and are internally biased to accommodate CML or PECL levels. AC-coupling or DC-coupling to the device can be used. However, with DC-coupling, the input common-mode voltage levels must be within the allowable limits. See the following illustrations for different high-speed input termination schemes.

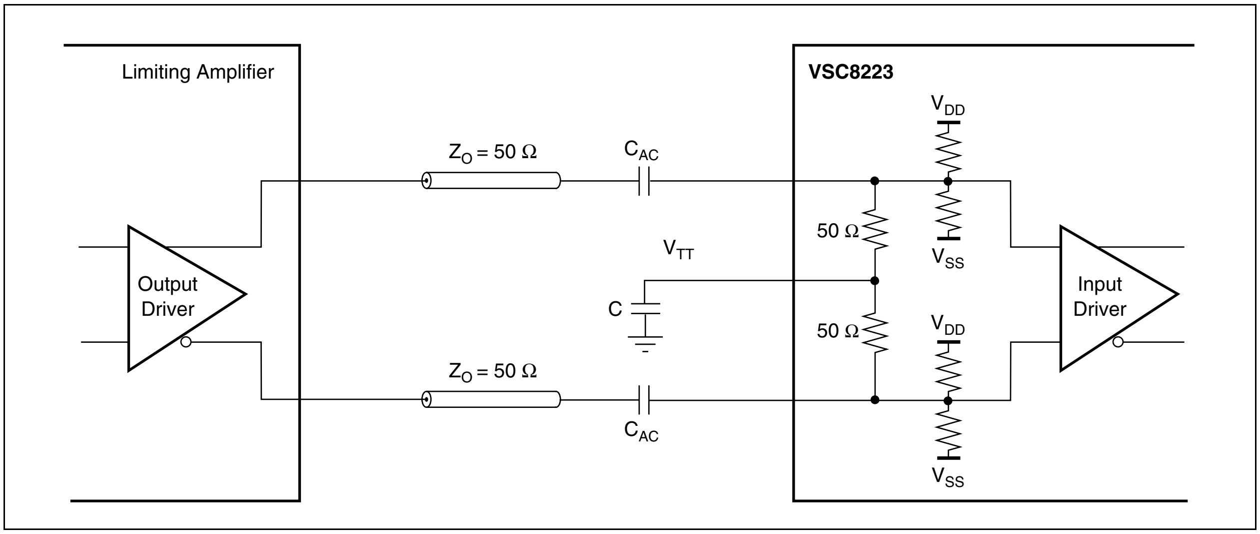


Figure 1. Differential AC-Coupled Input Termination

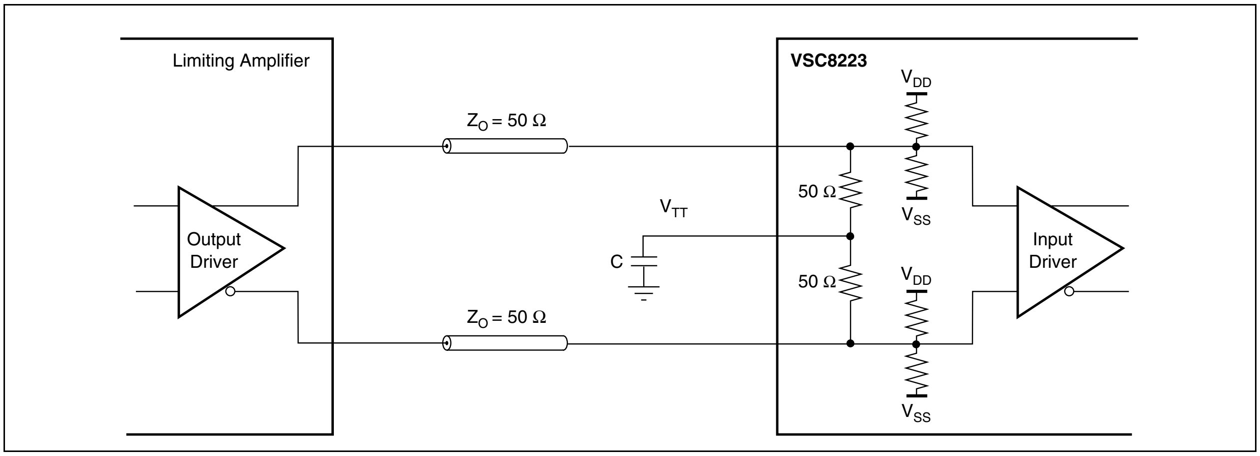


Figure 2. Differential DC-Coupled Input Termination

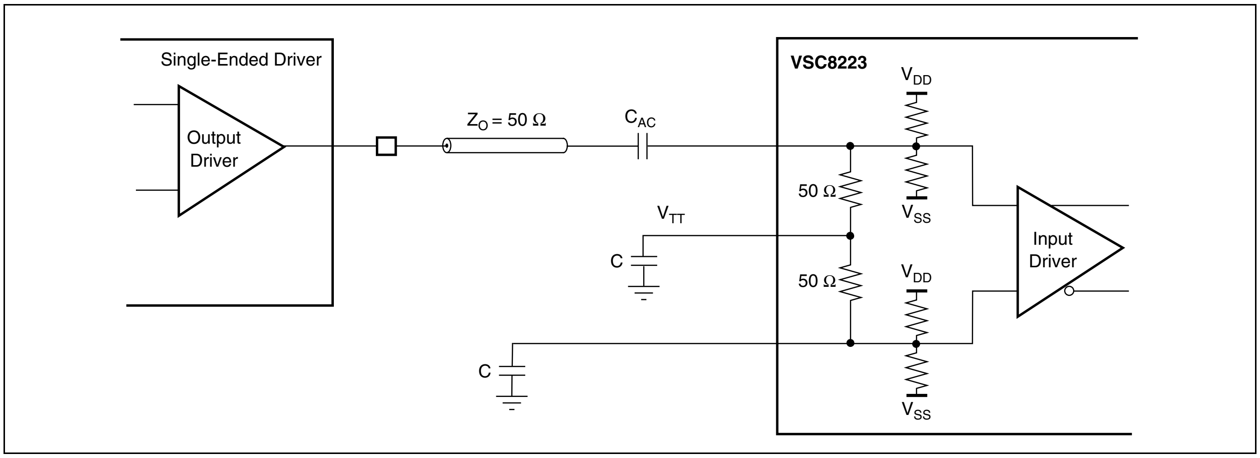
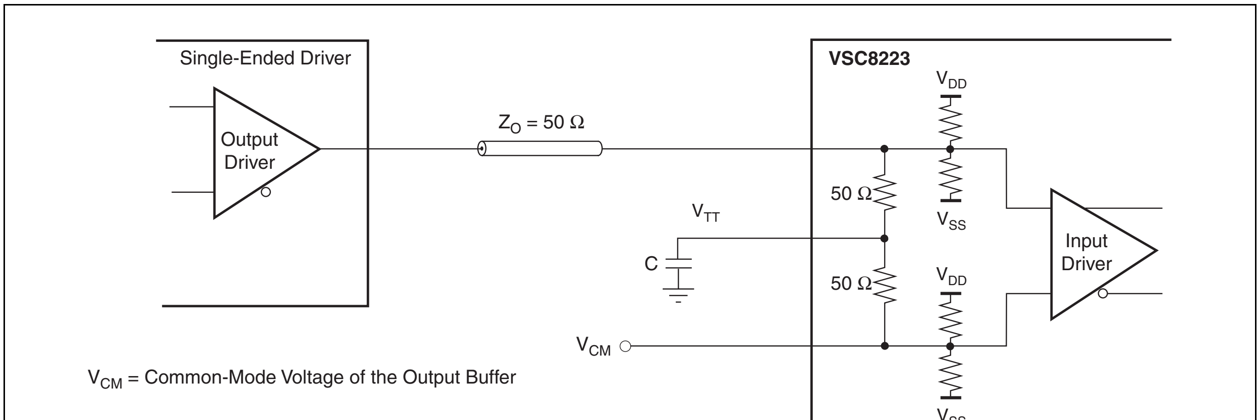


Figure 3. Single-Ended AC-Coupled Input Termination



V_{CM} = Common-Mode Voltage of the Output Buffer

NOTE: For best performance, it is strongly recommended differential input configurations be used. Vitesse does not guarantee device performance will meet datasheet specifications for single-ended termination schemes.

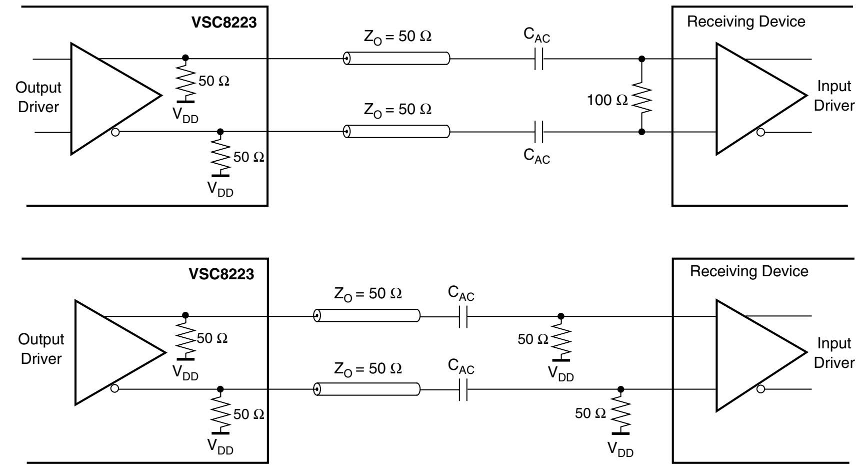
Figure 4. Single-Ended DC-Coupled Input Termination

High-Speed Data and Clock Outputs (SDO/$\overline{\text{SDO}}$ and SCO/$\overline{\text{SCO}}$)

The VSC8223 high-speed data output stage provides the following features:

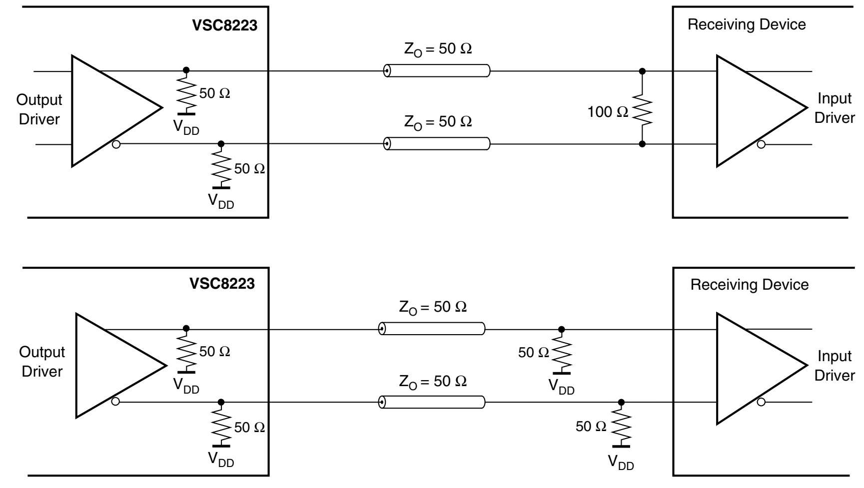
- On-die 50 Ω termination resistance to V_{DD}
- AC-coupled and DC-coupled operation
- Differential output operation
- Single-ended output operation

The high-speed data and clock output drivers are CML and consist of a differential pair designed to drive a 50 Ω transmission line. See the following illustrations for differential termination schemes.



NOTE: The 50 Ω and 100 Ω termination resistors can be internal or external to the receiving device.

Figure 5. High-Speed Output—AC-Coupled Terminations



NOTE: The 50 Ω and 100 Ω termination resistors can be internal or external to the receiving device.

Figure 6. High-Speed Output—DC-Coupled Terminations

Low-Speed REFCLK LVPECL Inputs

The LVPECL REFCLK[1:0] inputs are driven differentially, single-ended, DC-coupled or AC-coupled. For more information, see Table 21, page 18. The REFCLK inputs are internally biased; however, external input terminations must be provided.

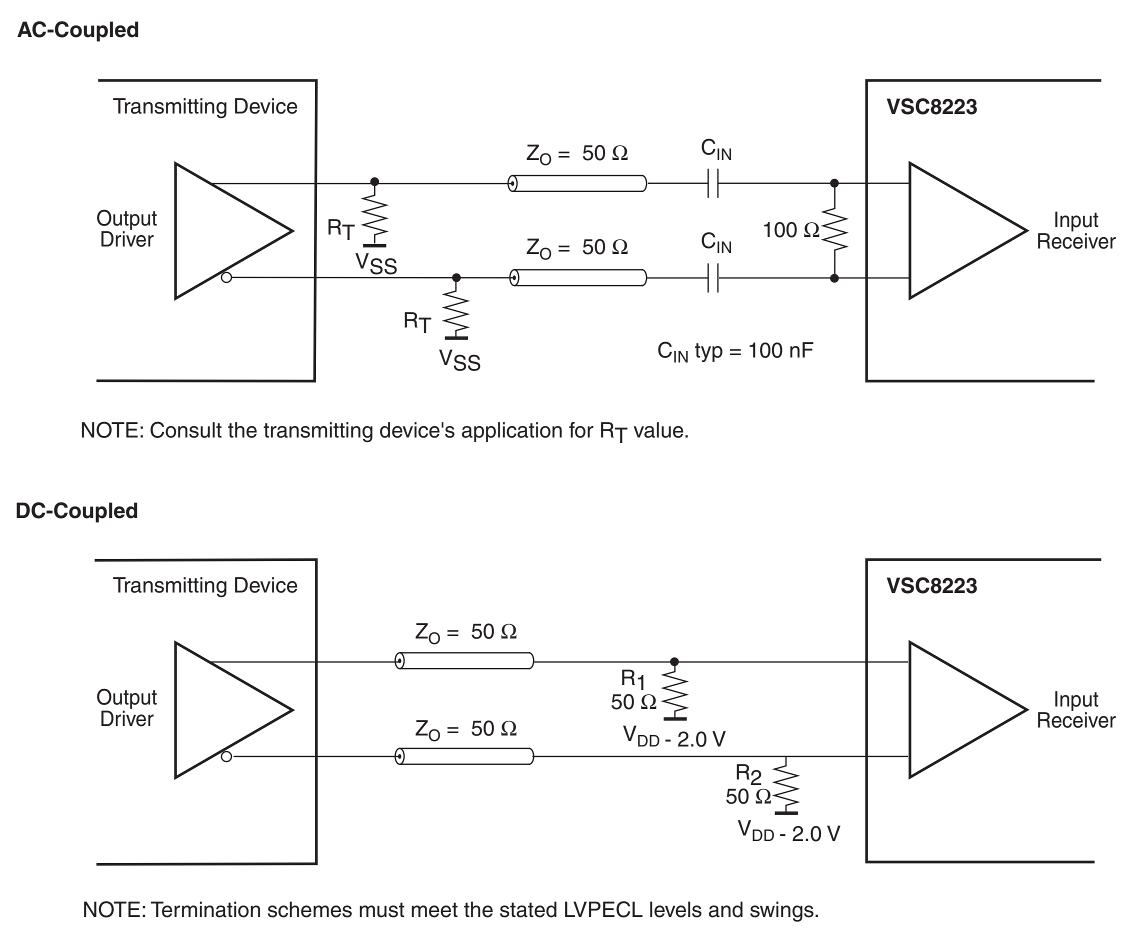


Figure 7. LVPECL Input Terminations

Reference Clock Input Selection

In the following table, the RCLK_SEL signal selects either the REFCLK1 and REFCLK0 inputs.

Table 1: RCLK_SEL Truth Table

RCLK_SEL	REFCLK Input Selected
Floating or not connected	REFCLK0
LOW (0)	REFCLK0
HIGH (1)	REFCLK1

Reference Clock Frequency Selection

In the following table, the RCLK_FSEL[1:0] control signals are used to select the REFCLK input frequency.

Table 2: RCLK_FSEL[1:0] Truth Table

RCLK_FSEL1	RCLK_FSEL0	SONET REFCLK Frequency (or FEC)
LOW (0)	LOW (0)	19.44 MHz(1)
LOW (0)	HIGH (1)	Not allowed
HIGH (1)	LOW (0)	77.76 MHz
HIGH (1)	HIGH (1)	155.52 MHz

1. *Does not meet SONET jitter specifications in lock-to-reference mode; however, it is valid in the normal mode of operation.*

An example application for SONET/SDH systems can be as follows: The regular frequency SONET/SDH reference clock can be connected to the REFCLK0/$\overline{\text{REFCLK0}}$ inputs, and the FEC version of the same clock can be connected to REFCLK1/$\overline{\text{REFCLK1}}$. Up to 15/14 FEC is supported.

Static LVTTL Control Inputs

LVTTL inputs are used for the following signals: RCLK_SEL, RCLK_FSEL[1:0], FC_SEL, STS12/$\overline{3}$, LREF, SCO_EN, and LREF_DIS. The LVTTL input signal levels are specified in Table 15, page 14.

Static LVTTL Control Outputs

LVTTL outputs are used for the following signals: LOS, LOL, and NOREF. The LVTTL output signal levels are specified in Table 16, page 14.

LOS Assertion

The LOS pin indicates inactivity on the SDI, $\overline{\text{SDI}}$ lines. LOS is defined in Telcordia GR-253-CORE, Section 6.2.1.1. LOS is interpreted as described in the following sections. If all-zeros or all-ones pattern exists at the input high-speed input receiver for 2.3 µs or less, LOS must not be asserted. If inactivity lasts 100 µs or greater, LOS must be asserted. If inactivity lasts between 2.3 µs and 100 µs, LOS assertion is left to the choice of the designer. The VSC8223 supports LOS assertion according to the specifications in Table 3, page 9.

LOS Termination

LOS may be terminated after 125 µs of time during which an LOS defect does not exist. LOS must be terminated after 250 µs of time during which an LOS defect does not exist.

NOREF Operation

The NOREF output will go HIGH to indicate that there is no signal on the REFCLK input or that the REFCLK is more than approximately 25% above or below the expected value.

Table 3: LOS Parameters

Symbol	Parameter	Minimum	Maximum	Unit	Condition
t_{LOS_SET}	LOS set time	2.3	100	µs	From data interruption
t_{LOS_CLEAR}	LOS clear time	125	250	µs	From data restoration

LOL

The LOL pin indicates loss of PLL lock. Loss of PLL lock is defined as the condition in which the absolute value of the difference between the frequency of the VCO and the frequency of the incoming serial data is greater than 400 ppm. The LOL specifications are summarized in the following table.

Table 4: LOL Parameters

Symbol	Parameter	Typical	Unit	Condition
t_{LOL_SET}	LOL set time	1	ms	From data interruption
t_{LOL_CLEAR}	LOL clear time	500	µs	From data restoration

Clock and Data Recovery Unit

This circuit meets or exceeds SONET jitter generation, jitter tolerance, and jitter transfer requirements.

The CRU accepts high-speed NRZ data (on SDI/$\overline{\text{SDI}}$ inputs) and recovers the clock for down-stream devices. The on-chip PLL consists of a phase detector, loop filter, VCO, and prescaler. If there is a phase error between the incoming data and the on-chip VCO, the loop filter raises or lowers the control voltage to the VCO to null the phase difference.

The CRU supports STS-12, STS-3, and FEC data rates. The VSC8223 device supports the data rates through the STS12/$\overline{3}$ pin, which is LVTTL. If no connections are made to the STS12/$\overline{3}$ pin, the default data rate supported is STS-12 and STS-12 (FEC). The following table shows the typical upper and lower data rate ranges.

Table 5: Supported Upper and Lower Data Ranges

STS12/$\overline{3}$	Lower Data Rate	Upper Data Rate	Service Type
Floating or not connected	600 Mbps	675 Mbps	STS-12, STS-12 (FEC)
LOW (0)	622 Mbps	675 Mbps	STS-12, STS-12 (FEC)
HIGH (1)	155 Mbps	168 Mbps	STS-3, STS-3 (FEC)

Two reference clock inputs (REFCLK0 and REFCLK1) are provided as clocking inputs to the device. The REFCLK to the CRU is selected by an external TTL control pin (RCLK_SEL). For more information about the REFCLK operation, see Table 1, page 8.

For SONET/SDH operation, the frequency of the REFCLK input to the CRU is 19.44 MHz, 77.76 MHz, or 155 MHz. For detailed information for selecting one of the above reference clocks, see Table 2, page 8.

Table 6: Recommended REFCLK Input Frequencies

STS-12/-3	STS-12/-3 FEC
77.76 MHz	83.314 MHz
155.52 MHz	166.629 MHz

The CRU outputs a high-speed output clock that is the same frequency as the serial bit clock that generated the incoming data stream. The accuracy of this clock is ±20 ppm or better.

Loop Filter

The PLL on the VSC8223 employs one external capacitor and must be connected between FILT0 and GND. The recommended capacitor is a low-inductance 1.0 µF (0603 or 0805) ceramic SMT X7R device, 6.3 WVDC or greater.

VCO

The internal VCO is capable of tuning through the STS-3, STS-12, and FEC frequency ranges.

Prescaler

The prescaler selection is detailed in Table 5, page 9.

Decision Circuit

The decision circuit is a D-FF. The retimed serial data is sent out on SDO and $\overline{\text{SDO}}$. The clock used to retime the serial data is also sent out on SCO and $\overline{\text{SCO}}$ output pins.

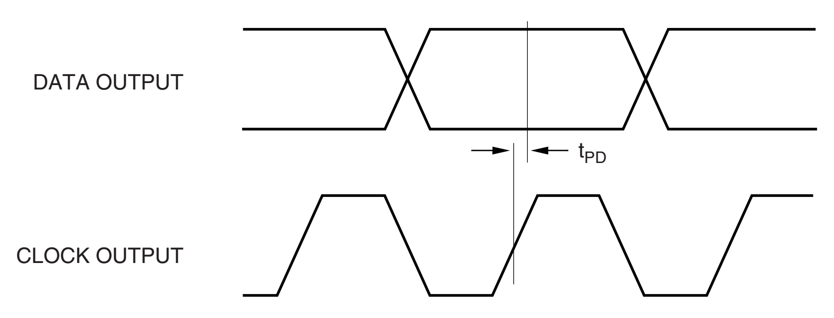


Figure 8. Clock to Data Propagation Delay

Clock Output Enable

The high-speed clock output (SCO/$\overline{\text{SCO}}$) can be disabled by using the SCO_EN pin. The operation of this control signal is detailed in the following table.

Table 7: SCO_EN Truth Table

SCO_EN	Operating Mode
Floating or not connected	High-speed clock output enabled
LOW (0)	High-speed clock output disabled
HIGH (1)	High-speed clock output enabled

Lock to Reference

The VSC8223 provides an automatic lock-to-reference mode (LOCK to REFCLK) during LOS occurrences. This mode can also be manually forced using the LREF signal. During a LOCK to REFCLK condition, the high-speed clock output is the same frequency prior to the LOCK to REFCLK condition and the high-speed data output is forced to a logic 0 level.

For diagnostic purposes or for applications that do not require the automatic LOCK to REFCLK operation, this mode of operation can be disabled using the LREF_DIS control signal.

Table 8: LREF_DIS Truth Table

RCLK_SEL	Operating Mode
Floating or not connected	Normal—CRU locks to incoming data (if present and valid) and automatic LOCK to REFCLK operation is enabled. LREF operates normally.
LOW (0)	Normal—CRU locks to incoming data (if present and valid) and automatic LOCK to REFCLK operation is enabled. LREF operates normally.
HIGH (1)	Disabled—Automatic LOCK to REFCLK operation is disabled and high-speed clock and data outputs are derived from the incoming data stream. LREF operates normally.

The LOCK to REFCLK mode of operation is entered when either event listed below occurs:

- Manually forced with LREF control signal—The LREF signal is used to manually force the VSC8223 into the LOCK to REFCLK mode of operation.
- Clean LOS occurrence—A clean LOS occurs when the incoming optical receiver stops receiving the incoming signal (such as due to a fiber cut) and the optical receiver electronics goes to either a static logic 1 or logic 0 state. For more information, see "LOS Assertion," page 8, "LOS Termination," page 9, and Table 3, page 9.

Table 9: LREF Truth Table

LREF	Operating Mode
Floating or not connected	Normal—CRU locks to incoming data (if present and valid) and automatic LOCK to REFCLK operation is enabled.
LOW (0)	Normal—CRU locks to incoming data (if present and valid) and automatic LOCK to REFCLK operation is enabled.
HIGH (1)	Forced—CRU locks to previously selected REFCLK input and outputs a high-speed clock (with same tolerance as REFCLK signal) and high-speed data outputs are forced to a logic 0 level.

- LOL occurrence—An LOL can occur due to unlockable input data such as if the incoming data was random, if the incoming data exceeded the input jitter tolerance of the VSC8223, or if the incoming data rate was out of the tuning range of the internal VCO. In this case, the high-speed clock outputs, SCO/$\overline{\text{SCO}}$, are within ±400 ppm of the incoming clock.
- Dirty LOS occurrence—A dirty LOS operation can occur due to the same condition as a clean LOS occurrence except the optical receiver does not go to a static logic 1 or 0, but instead oscillates and outputs random, unlockable data to the downstream CDR. This occurrence is seen as a LOL condition by the CRU. In this case, the high-speed clock outputs, SCO/$\overline{\text{SCO}}$ is within ±400 ppm of the incoming clock.

Automatic LOCK to REFCLK Detailed Operation

The automatic LOCK to REFCLK detailed operation is described through the use of four states as outlined in the Table 10, page 12. This description assumes that either LREF or LREF_DIS is not asserted.

The following table lists the automatic LOCK to REFCLK states for the VSC8223 device.

Table 10: Automatic LOCK to REFCLK States

Description	LOS	LOL	SCO/$\overline{\text{SCO}}$	SDO/$\overline{\text{SDO}}$
Device powered off	N/A	N/A	N/A	N/A
Normal Operation—Device is powered on and lockable input data is present	0	0	Phase-locked to input data	Retimed output data
Clean LOS Operation—Device is powered on and static 1 or 0 input data is present	1	0	Phase-locked to REFCLK	Static logic 0
LOL or Dirty LOS Operation—Device is powered on and unlockable input data, other than static 1 or 0, is present	0	1	±400 ppm of N × REFCLK	Static logic 0

The VSC8223 has a number of internally isolated power and ground busses. The V_{DDA} and V_{SSA} busses are used for the internal analog sections. For optimum performance, the V_{DDA} and V_{SSA} busses should be isolated and separately filtered from the other busses.

ELECTRICAL SPECIFICATIONS

Specifications listed in the following tables are guaranteed over the recommended operating conditions listed in Table 22, page 19, unless otherwise noted.

DC Characteristics

The following tables show the DC characteristics for the VSC8223 device.

Table 11: High-Speed Inputs (SDI, $\overline{\text{SDI}}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
V_{SDI_DE}	Voltage input swing (differential drive)	50		1000	mVp–p	Input signal on both true and complement inputs.
V_{ICM}	Input common-mode voltage	1.2		$V_{DD} – 0.1$	V	$V_{IH} < V_{DD}$.
R_{SDI}	Input termination resistance (differential)	80	100	120	Ω	

Table 12: High-Speed Data Outputs (SDO, $\overline{\text{SDO}}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
V_{SDO}	Output data voltage swing	400	500	800	mVp–p	Vp–p swing on true and complement outputs. With 50 Ω to V_{DD}.
V_{OCM}	Output common-mode voltage	$V_{DD} – 0.7$		$V_{DD} – 0.1$	V	With 50 Ω to V_{DD}.
R_{SDO}	Back-terminated output resistance	40	50	60	Ω	

Table 13: High-Speed Clock Outputs (SCO/$\overline{\text{SCO}}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
V_{SCO}	Output clock voltage swing	300	500	800	mVp–p	Vp–p swing on true and complement output.
V_{OCM}	Output common-mode voltage	$V_{DD} – 0.7$		$V_{DD} – 0.1$	V	With 50 Ω to V_{DD}.
R_{SCO}	Back-terminated output resistance	40	50	60	Ω	

Table 14: LVPECL Inputs

Symbol	Parameter	Minimum	Maximum	Unit	Condition
V_{DE_REFCLK}	REFCLK input voltage swing (differential). Normal CRU operation.	155	650	mVp–p	Input signal on both true and complement inputs.
V_{SE_REFCLK}	REFCLK input voltage swing (single-ended). Normal CRU operation.	310	1300	mVp–p	Input signal on either true or complement input with other input terminated.
V_{IH_REFCLK}	REFCLK input HIGH voltage	V_{DD} – 1.165	V_{DD} – 0.70	V	
V_{IL_REFCLK}	REFCLK input LOW voltage	V_{DD} – 2.0	V_{DD} – 1.475	V	

Table 15: LVTTL Inputs

Symbol	Parameter	Minimum	Maximum	Unit	Condition
V_{IH}	Input HIGH voltage	2.0	3.3	V	I_{IH} = 100 mA
V_{IL}	Input LOW voltage	0	0.8	V	I_{LL} = –100 µA

Table 16: LVTTL Outputs

Symbol	Parameter	Minimum	Maximum	Unit	Condition
V_{OH}	Output HIGH voltage	2.2	V_{DD}	V	I_{OH} = 1 mA
V_{OL}	Output LOW voltage	0	0.4	V	I_{OL} = –1 mA

AC Characteristics

The following tables show the AC characteristics for the VSC8223 device.

Table 17: High-Speed Inputs (SDI, $\overline{\text{SDI}}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
DR_{SDI_NORM}	Input data rate, normal CRU operation	0.125		670	Mbps	STS-12 FEC rate.
t_{SDI_R}, t_{SDI_F}	Serial data input rise time and fall time		150		ps	20% to 80% STS-12/STM-4 (FEC). See Figure 11, page 18.

Table 18: High-Speed Data Outputs (SDO,$\overline{\text{SDO}}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
DR_{SDO_NORM}	Output data rate, normal CRU operation	0.125		670	Mbps	STS-12/STM-4 FEC rate
t_{SDO_R}, t_{SDO_F}	Output data rise time and fall time		150		ps	20% to 80%, STS-12/STM-4 (FEC). See Figure 5, page 6. With 50 Ω to V_{DD}.
DC_{SDO}	Data output duty cycle	45	50	55	%	Only relevant with 101010 input data patterns. With 50 Ω to V_{DD}.

Table 19: High-Speed Clock Outputs (SCO/$\overline{\text{SCO}}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
DR_{SCO_NORM}	Output clock rate, normal CRU operation	0.125		670	MHz	Depends on signal.
t_{SCO_R}, t_{SCO_F}	Output clock rise time and fall time		150		ps	20% to 80%, STS-12/STM-4 (FEC). See Figure 5, page 6. With 50 Ω to V_{DD}.
DC_{SCO}	Clock output duty cycle	45	50	55	%	Measured at 50% crossing of peak-to-peak voltage. With 50 Ω to V_{DD}.

Table 20: Clock and Data Recovery

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
J_{GEN1_CLOCK}	Jitter generation (clock output)(1)			8.5	mUI_{rms}	High-speed clock output jitter in the appropriate frequency band. Assumes 1.2 ps rms input data jitter. With 50 Ω to V_{DD}.

Table 20: Clock and Data Recovery *(Continued)*

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
J_{GEN1_DATA}	Jitter generation (data output)(1)			8.5	mUI_{rms}	High-speed data output jitter in the appropriate frequency band. Assume 1.2 ps rms input data jitter. With 50 Ω to V_{DD}.
J_{TOL_12}	Jitter tolerance, STS-12(1)	0.15 1.5 15			UI UI UI	250 kHz < f < 5 MHz 300 Hz < f < 25 kHz 10 Hz < f < 30 Hz LBW [1:0] = 0,0.
J_{TOL_3}	Jitter tolerance, STS-3(1)	0.15 1.5 15			UI UI UI	65 kHz < f < 1.3 MHz 300 Hz < f < 6.5 kHz 10 Hz < f < 30 Hz LBW [1:0] = 0,0.
J_{TBW}	Jitter transfer bandwidth(1)		500		kHz	Meets STS-12/STM-4. Scales linearly for lower data rates. Bandwidth not specified in lock-to-reference modes. With 50 Ω to V_{DD}. LBW [1:0] = 0,0.
J_{TPEAK}	Jitter transfer peaking(1)			0.1	dB	With 50 Ω to V_{DD}. See Figure 10, page 17.
t_{PD}	Data to clock propagation delay	0		150	ps	Center of output data eye from rising edge of SCO. With 50 Ω to V_{DD}.
t_{PWR_UP}	CRU lock time (on power-up)		50		ms	With 50 Ω to V_{DD}.
t_{SYNC}	CRU lock time (synchronous switch)		2500		bit times	When input is switched to a source with the same data rate. With 50 Ω to V_{DD}.
t_{ASYNC}	CRU lock time (asynchronous switch)		50		ms	When input is switched to a source with a different data rate. With 50 Ω to V_{DD}.
t_{LREF}	LOCK-to-REFCLK switch time		100		µs	Time after assertion of LOS for clock output to be valid. With 50 Ω to V_{DD}.
t_{LREF_REC}	Recover from LOCK-to-REF-CLK switch time		100		µs	Time after deassertion of LOS for valid clock and data. With 50 Ω to V_{DD}.

1. *Jitter generation, tolerance, transfer, and peaking specifications measured using SONET methodologies.*

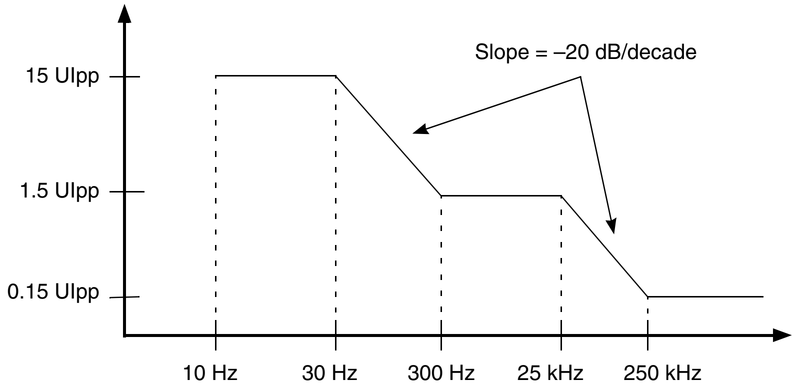
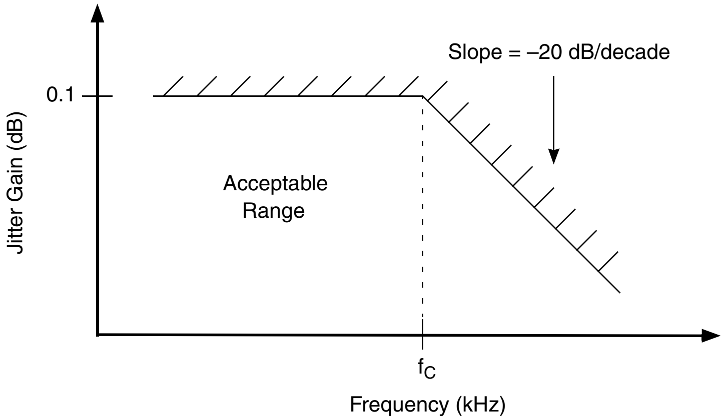


Figure 9. STS-12 SONET Jitter Tolerance Mask

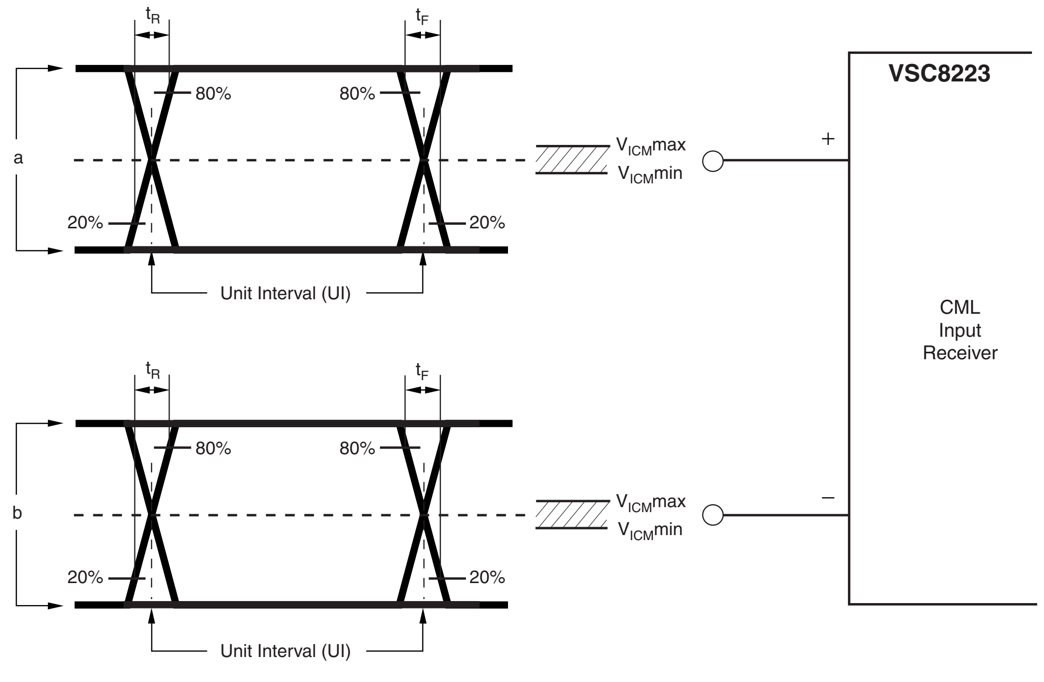


STS-n/STS-n Level	f_C (kHz)
3	130
12	500

Figure 10. SONET Jitter Transfer Mask

Table 21: LVPECL Inputs

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
f_{REFCLK}	REFCLK input frequency, normal CRU operation	14.8		169	MHz	Maximum is STS-12 FEC rate.
t_{REFCLK_R}, t_{REFCLK_F}	REFCLK rise time and fall times, normal CRU operation			250	ps	20% to 80%. See Figure 11. REFCLK = 155 MHz.
f_{REFCLK_TOL}	REFCLK frequency tolerance, normal CRU operation	–100		100	ppm	±20 ppm required to meet SONET/SDH specifications when in LOCK to REFCLK mode.
DC_{REFCLK}	REFCLK input duty cycle	40	50	60	%	Measured at 50% crossing of peak-to-peak voltage.
J_{REFCLK}	REFCLK input jitter			1.2	ps rms	



If used differentially (true and complement), each signal should meet the requirements for $a = b = V_{A\_DE}$.
If used single-ended (true only), the value required is $a = 2 \times V_{A\_DE}$.

Figure 11. Input Parametric Symbol Definitions

Operating Conditions

The following table shows the recommended operating conditions for the VSC8223 device.

Table 22. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Condition
V_{DD}	Power supply voltage	2.375	2.5	2.625	V	±5% tolerance
I_{DD_SDO}	Power supply current			181	mA	
I_{DD}	Power supply current			217	mA	
P_{TOT_SDO}	Power dissipation		315	475	mW	Clock disabled
P_{TOT}	Total power dissipation		400	570	mW	Clock enabled
T	Operating temperature(1)	–20		85	°C	

1. Lower limit of specification is ambient temperature, and upper limit is case temperature.

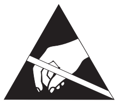
Stress Ratings

This section contains the stress ratings for the VSC8223 device.

Stresses listed in the following table may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 23. Stress Ratings

Symbol	Parameter	Minimum	Maximum	Unit
V_{DD}	Power supply voltage	–0.5	3.8	V
	DC input voltage (differential)	–0.5	$V_{CC} + 0.5$	V
	DC input voltage (TTL)	–0.5	5.5	V
	DC output voltage (TTL)	–0.5	$V_{CC} + 0.5$	V
	Output current (differential and TTL)	–50	50	mA
V_{ESD_CDM}	Electrostatic discharge voltage, charged device model	–500	500	V
V_{ESD_HBM}	Electrostatic discharge voltage, human body model	–250	250	V



ELECTROSTATIC DISCHARGE

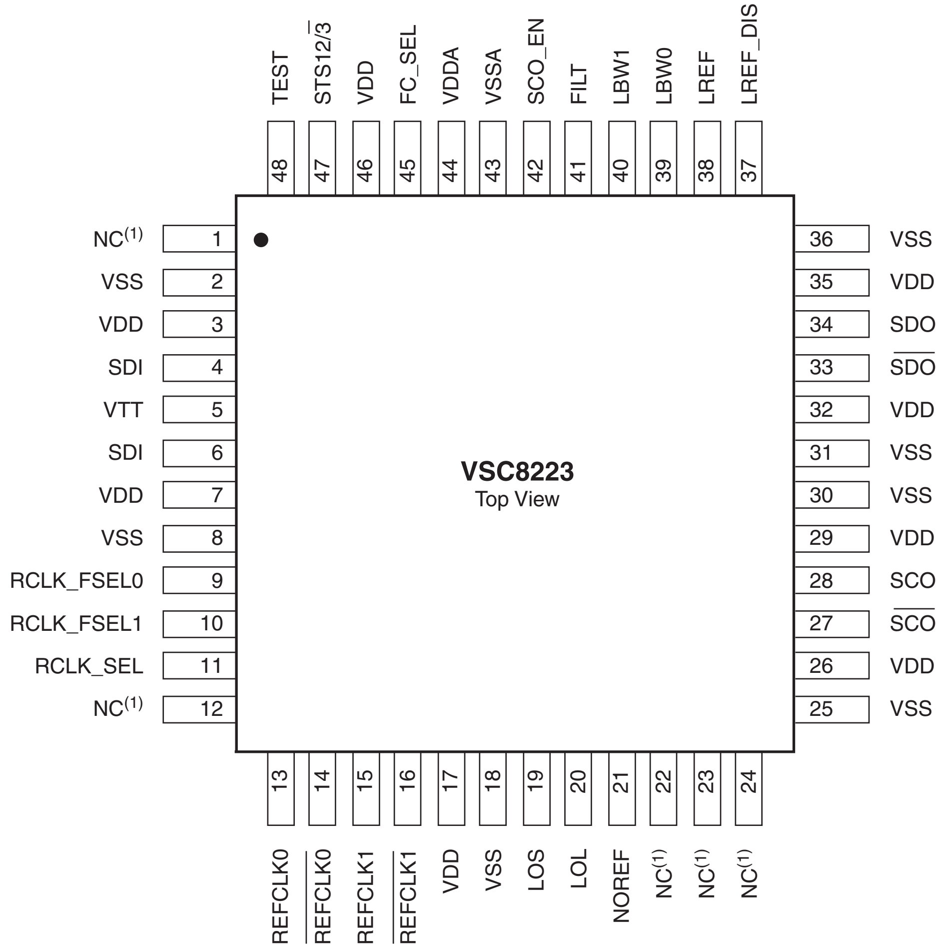
This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

PIN DESCRIPTIONS

This sections contains the pin diagram and pin descriptions for the VSC8223 device.

Pin Diagram

The VSC8223 device has 48 pins as shown in the following diagram.



(1) No Connect (NC) pins must be left unconnected, or floating. Connecting any of these pins to either the positive or negative supply rails or a logic level driver may cause improper operation or failure of the device; or in extreme cases, may cause permanent damage to the device.

Figure 12. Pin Diagram

Pin Identifications

This section contains detailed pin descriptions for the VSC8223 device.

Table 24: Pin Identification for 48-Pin LQFP

Pin Number	Signal Name	I/O	Level	Description
1	NC	I	LVTTL	No connect[1].
2	VSS		Power	Ground.
3	VDD		Power	2.5 V power supply
4	SDI	I	CML	High-speed serial input, true.
5	VTT		Analog/ Power	High-speed input data termination voltage. One option is to bypass to V_{DD} with a capacitor. Direct connection to a supply V_{SS} <= VTERM <= V_{DD} is also allowed as long as input common-mode levels are maintained within limits specified in Table 11, page 13.
6	$\overline{\text{SDI}}$	I	CML	High-speed serial input, complement.
7	VDD		Power	2.5 V power supply.
8	VSS		Power	Ground.
9	RCLK_FSEL0	I	LVTTL	Reference clock rate select pin. Default: LOW (0).
10	RCLK_FSEL1	I	LVTTL	Reference clock rate select pin. Default: LOW (0).
11	RCLK_SEL	I	LVTTL	Reference clock select pin. Default: LOW (0). When LOW (0), select REFCLK0/$\overline{\text{REFCLK0}}$; when HIGH (1), select REFCLK1/ $\overline{\text{REFCLK1}}$.
12	NC			Not connected[1].
13	REFCLK0	I	LVPECL	Reference clock 0, true.
14	$\overline{\text{REFCLK0}}$	I	LVPECL	Reference clock 0, complement.
15	REFCLK1	I	LVPECL	Reference clock 1, true.
16	$\overline{\text{REFCLK1}}$	I	LVPECL	Reference clock 1, complement.
17	VDD		Power	2.5 V power supply.
18	VSS		Power	Ground.
19	LOS	O	LVTTL	When HIGH, indicates no serial data input signals. It may trigger the automatic lock-to-reference clock based on LREF_DIS.
20	LOL	O	LVTTL	When HIGH, indicates the device lost lock-to-reference clock.
21	NOREF	O	LVTTL	When HIGH, indicates no reference clock is provided.
22	NC			No connect[1].
23	NC			No connect[1].
24	NC			No connect[1].
25	VSS		Power	Ground.
26	VDD		Power	2.5 V power supply.
27	$\overline{\text{SCO}}$	O		High-speed clock serial clock output, complement.
28	SCO	O		High-speed clock serial clock output, true.
29	VDD		Power	2.5 V power supply.
30	VSS		Power	Ground.
31	VSS		Power	Ground.

Table 24: Pin Identification for 48-Pin LQFP *(Continued)*

Pin Number	Signal Name	I/O	Level	Description
32	VDD		Power	2.5 V power supply.
33	$\overline{\text{SDO}}$	O	CML	High-speed serial data output, complement.
34	SDO	O	CML	High-speed serial data output, true.
35	VDD		Power	2.5 V power supply.
36	VSS		Power	Ground.
37	LREF_DIS	I	LVTTL	Default: LOW (0). When HIGH (1), disables the automatic lock to reference clock function. Manual lock-to-reference clock function using LREF is still enabled.
38	LREF	I	LVTTL	Default: LOW (0). When HIGH (1), enables the force lock-to-reference clock function.
39	LBW0			Default: Leave unconnected. Optional: Connect to V_{DD} for loop bandwidth control.
40	LBW1			Default: Leave unconnected. Optional: Connect to V_{DD} for loop bandwidth control.
41	FILT		Analog	Connected to an external PLL 1 µF capacitor.
42	SCO_EN	I	LVTTL	Default: HIGH (1). When LOW (0), clock output is disabled.
43	VSSA		Power	Ground for VCO.
44	VDDA		Power	Power supply for VCO.
45	FC_SEL	I	LVTTL	Default: LOW (0). When HIGH (1), PLL/VCO runs at 2.125 GHz (Fibre Channel rate). When LOW (0), runs at 2.488 GHz.
46	VDD		Power	2.5 V power supply.
47	STS12/$\overline{3}$	I	LVTTL	Input data rate select pin. Default: LOW(0). Selects between the STS-12 and STS-3 data rates.
48	TEST	I	LVTTL	Default: LOW (0), normal operation. When HIGH (1), enter test mode.

[1] *No connect (NC) pins must be left unconnected or floating. Connecting any of these pins to either the positive or negative power supply rails or a logic level driver may cause improper operation or failure of the device, or in extreme cases, cause permanent damage to the device.*

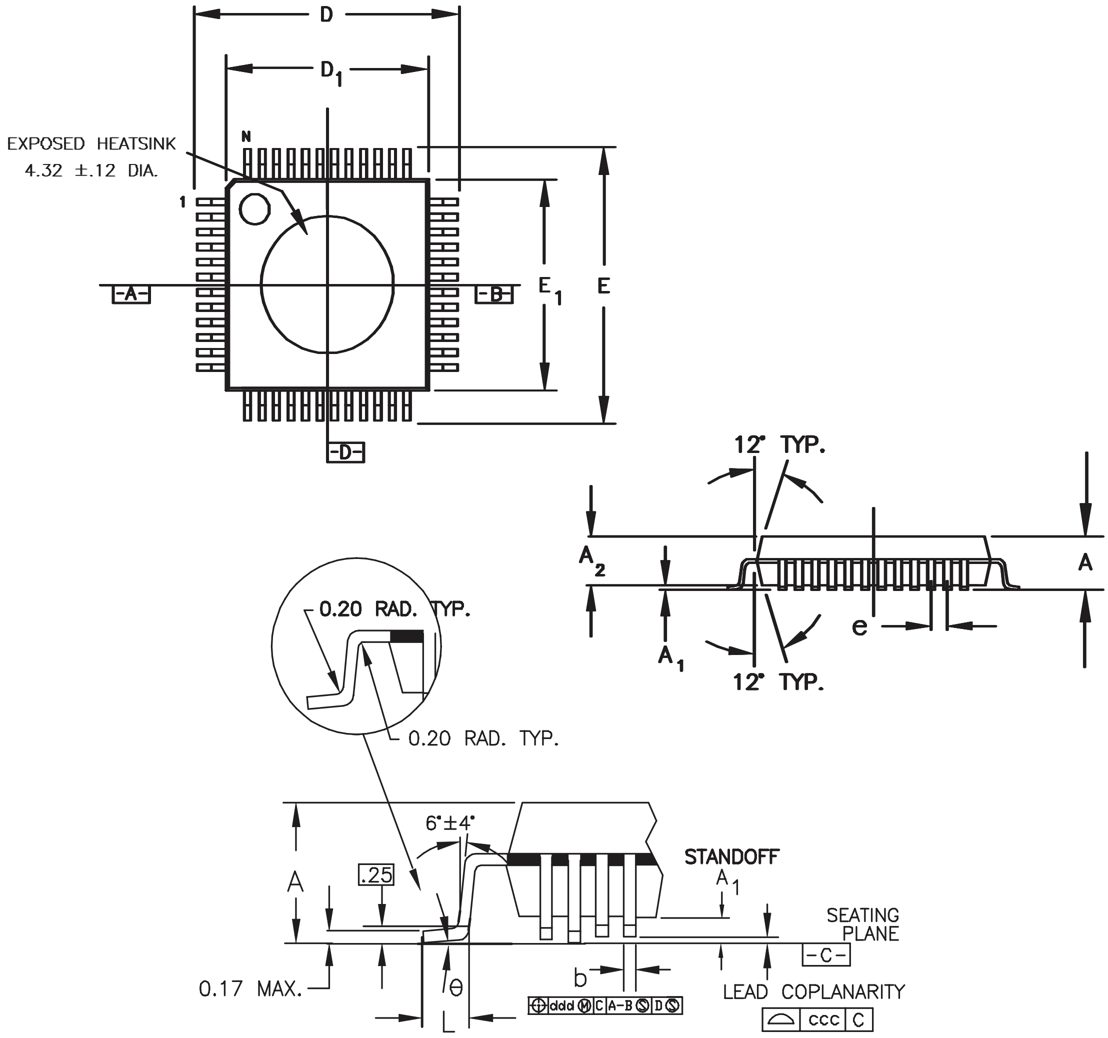
PACKAGE INFORMATION

The VSC8223 is available in two package types. VSC8223RV is a 48-pin, plastic low-profile quad flat package (LQFP) with an exposed pad, 7 mm × 7 mm body size, 1.4 mm body thickness, 0.5 mm pin pitch, and 1.60 mm maximum height. The device is also available in a lead(Pb)-free package, VSC8223XRV.

Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

This section provides the package drawing, thermal specifications, and moisture sensitivity rating for the VSC8223 device.

Package Drawing



LEAD COUNT		48L
DIMS.	TOL.	1.4 mm THICK
A	MAX.	1.60
A_1		.05 MIN./ .15 MAX.
A_2	±.05	1.40
D	±.20	9.00
D_1	±.10	7.00
E	±.20	9.00
E_1	±.10	7.00
L	+.15/−.10	.60
e	BASIC	.50
b	±.05	.22
θ		0°−7°
ddd	MAX.	.08
ccc	MAX.	.08

Notes:

1. All dimensions and tolerances are in millimeters (mm).
2. Dimensions shown are normal with tolerances as indicated.
3. Foot length “L” is measured at gage plane, at 0.25 above the seating plane.

Figure 13. Package Drawing

Thermal Specifications

Thermal specifications for this device are based on the JEDEC standard EIA/JESD51-2 and have been modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information, see the JEDEC standard.

Table 25. Thermal Resistances

Part Order Number	θ_{JC}	θ_{JB}	θ_{JA} **(°C/W) vs. Airflow (ft/min)**		
			0	**100**	**200**
VSC8223RV	3.6	28	46.5	43.5	40.2
VSC8223XRV	3.6	28	46.5	43.5	40.2

To achieve results similar to the modeled thermal resistance measurements, the guidelines for board design described in the JEDEC standard EIA/JESD51 series must be applied. For information about specific applications, see the following:

EIA/JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*

EIA/JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

EIA/JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

EIA/JESD51-10, *Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements*

EIA/JESD51-11, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements*

Moisture Sensitivity

Moisture sensitivity level ratings for Vitesse products comply with the joint IPC and JEDEC standard IPC/JEDEC J-STD-020.

VSC8223RV is rated moisture sensitivity level 3 or better.

VSC8223XRV is rated moisture sensitivity level 4.

For more information, see the IPC and JEDEC standard.

ORDERING INFORMATION

The VSC8223 is available in two package types. VSC8223RV is a 48-pin, plastic low-profile quad flat package (LQFP) with an exposed pad, 7 mm × 7 mm body size, 1.4 mm body thickness, 0.5 mm pin pitch, and 1.60 mm maximum height. The device is also available in a lead(Pb)-free package, VSC8223XRV.

Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

The following table lists the ordering information for the VSC8223 device.

VSC8223 Extended Multirate STS-12, STS-3, and FEC Clock and Data Recovery IC

Part Number	Description
VSC8223RV	48-pin, plastic LQFP with an exposed pad, 7 mm × 7 mm body size, 1.4 mm body thickness, 0.5 mm pin pitch and 1.60 mm maximum height
VSC8223XRV	Lead(Pb)-free, 48-pin, plastic LQFP with an exposed pad, 7 mm × 7 mm body size, 1.4 mm body thickness, 0.5 mm pin pitch, and 1.60 mm maximum height

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