ADVANCE INFORMATION

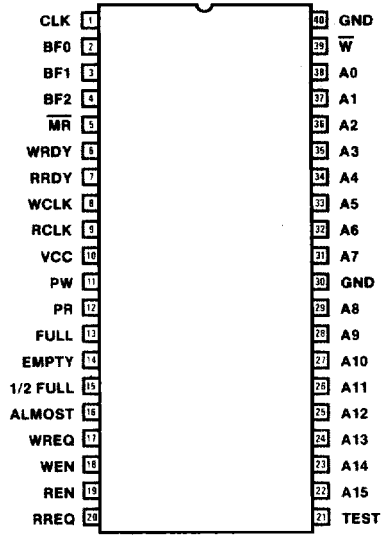
Features/Benefits

- High speed
- Deep FIFOs — 16 addresses for SRAM
- Arbitration read/write
- Control signals for data latching
- Full, half-full, empty and almost-full flags for any buffer size from 512 to 64K
- Expandable
- Three-state outputs

Typical Applications

- LAN equipment
- Data communication
- Disk/tape controllers
- Host to Dedicated Processor interface

Pin Configuration

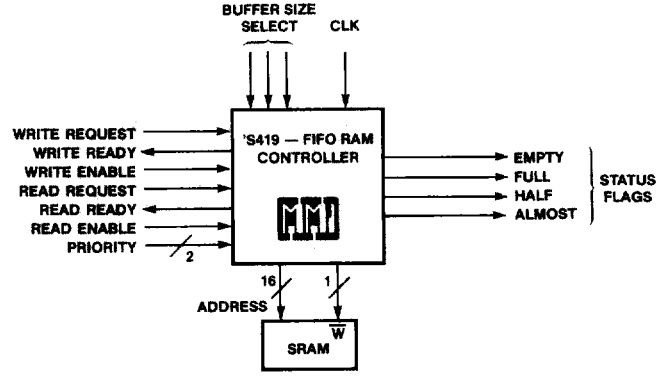


Description

The 54/74S419 FIFO Ram Controller provides addressing, control, status and arbitration for a shared SRAM used as a First-In-First-Out buffer. The 16 address lines can address up to 64K deep SRAM. Control signals include the $\overline{W}$ for SRAM, handshake signals for READ/WRITE ports, and strokes for external data latching.

The 'S419 allows single port SRAM to resolve read and write request conflicts according to a simple priority rule. If priority is selected on either read or write port, the operation requested is serviced with no delay. For no priority mode, read and write operations are alternated.

Block Diagram



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