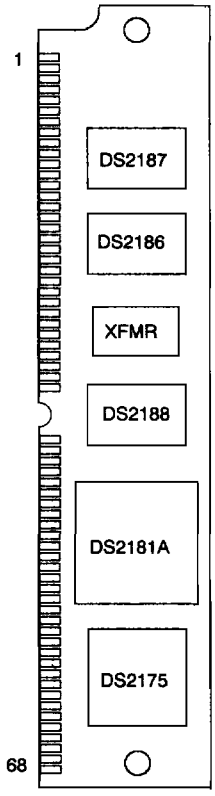
DALLAS SEMICONDUCTOR

# DS2284
## Enhanced CEPT Line Card Stik

### FEATURES

- Pretested, snap-in CEPT (E1) line card
- Consumes only 2 square inches of board space
- Performs five functions:
  - line interface
  - clock and data dejittering
  - framing
  - monitoring
  - buffering
- Includes line interface transformers and termination resistors
- Pin compatible with the DS2283 Enhanced T1 Line Card Stik
- Two separate loopback modes: line and local
- Connects to both 1.544 MHz and 2.048 MHz backplanes
- User programmable for either 75 ohm or 120 ohm interfaces
- Fully CMOS for low power consumption
- Operates off a single +5V supply

### PIN ASSIGNMENT




### DESCRIPTION

The DS2284 is a CEPT (E1) line card that consumes only 2 square inches of printed circuit board space. The card is designed to plug into standard 68-pin Single In-Line connectors. It has been arranged for maximum flexibility and contains all the necessary hardware to connect directly to either CEPT 2.048Mbps 75 or 120 ohm lines. The line interface function is performed by the DS2187 and DS2186. The dejittering of the clock and data is performed by the DS2188. The monitoring and framing functions are performed by the DS2181A. The buffering function is handled by the DS2175. The DS2284 provides all standard alarm indications as well as two different levels of carrier loss (32 zero and 192 zero). It also provides indication of frame errors, CRC errors, and bipolar violations.

## OVERVIEW

The DS2284 contains five of Dallas Semiconductor's CEPT (E1) integrated circuits: the DS2187 Receive Line Interface, the DS2186 Transmit Line Interface, the DS2181A CEPT Primary Rate Transceiver, the DS2188 Jitter Attenuator, and the DS2175 Elastic Store. The operational specifics of each of these devices can be found in their individual data sheets. On the DS2284, the DS2187 connects to the receive CEPT line through a 1:2 transformer. Both 120–ohm and 75–ohm CEPT lines can be properly terminated by the DS2284. On 75–ohm CEPT lines, pins 7 and 8 should be tied to ground. On 120–ohm CEPT lines, pins 7 and 8 should be left open circuited. The DS2187 recovers clock and data from the CEPT line. The recovered clock and data is passed to the DS2188 where it is dejittered (if enabled via the DJA pin). The dejittered clock and data is then provided to the DS2181A transceiver and it is also sent to pin 52 where it may be used as a source for the transmit clock. The transceiver frames to the incoming data stream and provides status information on the received data. An external controller is used to access a set of internal registers via a serial port. These registers are used to configure the device and to retrieve monitoring information.

The DS2284 also contains an elastic store, the DS2175. The DS2175 performs two functions. First, it is used to absorb clock rate and phase differences between the clock recovered by the DS2187 and a system backplane clock. Secondly, it can be used to connect the DS2284 to 1.544 MHz backplanes.

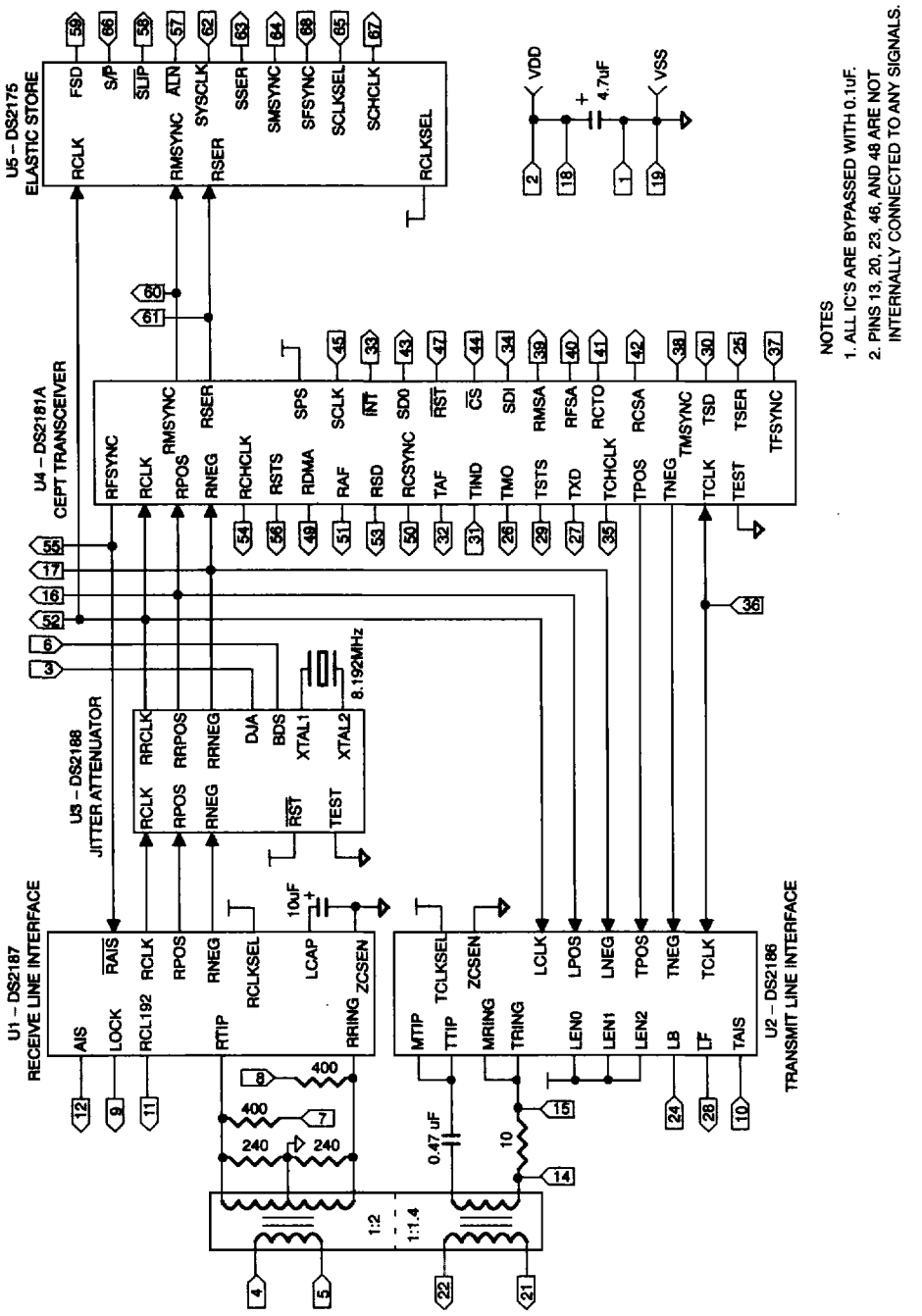
The DS2187, DS2188, DS2181A, and DS2175 form the receive section of the DS2284. The transmit section of the DS2284 is formed by the CEPT transceiver and the Transmit Line Interface, the DS2186. Data that is to be transmitted onto the transmit CEPT line is clocked into the DS2181A transceiver with a transmit clock (TCLK). The transceiver formats the data stream and adds any additional information (signaling, CRC-4, etc.) that might be necessary. The transceiver also transforms the data stream from a unipolar to a bipolar format and, if selected, it will perform HDB3 encoding. Bipolar data from the DS2181A is clocked into the DS2186 where it is level shifted and driven onto the transmit CEPT line twisted pair via a 1:1.4 transformer. The DS2284 can connect to both 75–ohm and 120–ohm CEPT lines. To connect to 75–ohm lines, pins 14 and 15 should be left open circuited. To connect to 120–ohm lines, pins 14 and 15 should be shorted together. A schematic of the DS2284 is shown in Figure 1.

The DS2284 is designed to connect into a standard 68-pin Single In-Line connector with a pin spacing pitch of 0.050 inches. Both inclined and vertical connectors are available from connector vendors such as AMP Incorporated. Table 1 lists a set of suitable connectors from AMP's MicroEdge™ Line. These connectors can also be obtained from Dallas Semiconductor.

**68-PIN CONNECTORS FOR DS2284** Table 1

| DESCRIPTION | AMP PART # | DALLAS PART # |
|---|---|---|
| Vertical | 821824-7 | DS9072-68V |
| Inclined | 821907-6 | DS9072-68I |
| Right Angle (high profile) | 6-382486-2 | DS9072H-68R |
| Right Angle (low profile) | 6-382480-8 | DS9072L-68R |

## DS2284 SCHEMATIC Figure 1



**PIN DESCRIPTION** Table 2

| PIN | SYMBOL | TYPE | DEVICE | DESCRIPTION |
|---|---|---|---|---|
| 1 | $V_{SS}$ | - | - | **Ground.** Connect to 0.0V. |
| 2 | $V_{DD}$ | - | - | **Positive Supply.** Connect to 5.0V. |
| 3 | DJA | I | DS2188 | **Disable Jitter Attenuation.** When strapped high, the jitter attenuation feature will be disabled and all of the jitter present at RTIP and RRING will be passed to RCLK, RPOS, and RNEG. |
| 4<br>5 | RTIP<br>RRING | I | DS2187 | **Receive Tip and Ring.** Connects directly to the receive CEPT (E1) line. |
| 6 | BDS | I | DS2188 | **Buffer Depth Select.**<br>0 = 128 bits<br>1 = 32 bits |
| 7<br>8 | RTERM1<br>RTERM2 | | | **Receive Termination Select.** Tie RTERM1 and RTERM2 to ground to set the receive termination at 75 ohms. Leave RTERM1 and RTERM2 open to set the receive termination at 120 ohms. |
| 9 | LOCK | O | DS2187 | **Frequency Lock Indication.** High state indicates that the DS2187 is phase– and frequency–locked to the incoming signal at RTIP and RRING. |
| 10 | TAIS | I | DS2186 | **Transmit Alarm Indication Signal.** When strapped high, an unframed all ones signal is transmitted at TTIP and TRING at the TCLK rate. |
| 11 | RCL192 | O | DS2187 | **Receive Carrier Loss.** High state indicates that at least 192 consecutive zeros have been received at RTIP and RRING. |
| 12 | AIS | O | DS2187 | **Receive Alarm Indication Signal.** High state indicates that the receive data stream at RTIP and RRING contains less than three zeros over two full frames of incoming data. |
| 13 | NC | | | **No Connect.** Does not connect to any internal signals. |
| 14<br>15 | XTERM1<br>XTERM2 | | | **Transmit Termination Select.** Connect XTERM1 and XTERM2 together to set the output pulse level to 3.0Vpeak (120 ohm). Leave XTERM1 and XTERM2 open to set the output pulse level to 2.37Vpeak (75 ohm). |
| 16<br>17 | RPOS<br>RNEG | O | DS2188 | **Receive Positive and Negative Data.** Data extracted from the CEPT line by the DS2187 and buffered by the DS2188. |
| 18 | $V_{DD}$ | - | - | **Positive Supply.** Connect to 5.0V. |
| 19 | $V_{SS}$ | - | - | **Ground.** Connect to 0.0V. |
| 20 | NC | | | **No Connect.** Does not connect to any internal signals. |
| 21<br>22 | TRING<br>TTIP | O | DS2186 | **Transmit Tip and Ring.** Connects directly to the transmit CEPT (E1) line. |
| 23 | NC | | | **No Connect.** Does not connect to any internal signals. |
| 24 | LB | I | DS2186 | **Line Loopback.** When strapped high, clock and data received at RTIP and RRING is looped back to TTIP and TRING. |
| 25 | TSER | I | DS2181A | **Transmit Serial Data**. NRZ data input, sampled on the falling edge of TCLK. |
| 26 | TMO | O | DS2181A | **Transmit Multiframe Out.** Output of the internal multiframe counter; indicates multiframe boundaries. |

| PIN | SYMBOL | TYPE | DEVICE | DESCRIPTION |
|---|---|---|---|---|
| 27 | TXD | I | DS2181A | **Transmit Extra Data.** Sampled on the falling edge of TCLK during bit times 5, 7, and 8 of timeslot 16 when CAS is enabled. |
| 28 | LF | O | DS2186 | **Line Fault.** Open collector; active low output. Held low during an output driver fault or failure; 3-stated otherwise. |
| 29 | TSTS | O | DS2181A | **Transmit Signaling Timeslot.** High during timeslot 16 of every frame, low otherwise. |
| 30 | TSD | I | DS2181A | **Transmit Signaling Data.** CAS signaling data input; sampled on the falling edge of TCLK for insertion into outgoing timeslot 16 when enabled. |
| 31 | TIND | I | DS2181A | **Transmit International and National Data.** Sampled on the falling edge of TCLK during bit 1 of timeslot 0 of every frame (international) and/or during bit times 4 through 8 of timeslot 0 during non-align frames (national) when enabled. |
| 32 | TAF | O | DS2181A | **Transmit Alignment Frame.** High during frames containing the frame alignment signal, low otherwise. |
| 33 | INT | O | DS2181A | **Receive Alarm Interrupt.** Flags host controller during alarm conditions. Active low, open drain output. |
| 34 | SDI | I | DS2181A | **Serial Data In.** Data for onboard registers. Sampled on the rising edge of SCLK. |
| 35 | TCHCLK | O | DS2181A | **Transmit Channel Clock.** 256 KHz clock which identifies timeslot (channel) boundaries. |
| 36 | TCLK | I | DS2186<br>DS2181A | **Transmit Clock.** A 2.048 MHz clock should be applied here. |
| 37 | TFSYNC | I | DS2181A | **Transmit Frame Sync.** Rising edge identifies frame boundary; may be pulsed every frame to reinforce internal frame counter, or tied low, allowing TMSYNC to establish multiframe and frame alignment. |
| 38 | TMSYNC | I | DS2181A | **Transmit Multiframe Sync.** May be pulsed high at multiframe boundaries to reinforce multiframe alignment, or tied low, which allows the internal multiframe counter to run free. |
| 39 | RMSA | O | DS2181A | **Receive Multiframe Sync Active.** This pin will transition high when the synchronizer searching for the CAS multiframe alignment word is active. |
| 40 | RFSA | O | DS2181A | **Receive Frame Sync Active.** This pin will transition high when the synchronizer searching for the frame alignment signal (FAS) is active. |
| 41 | RCTO | O | DS2181A | **Receive CRC4 Time Out.** This pin will transition high when the Stik cannot achieve sync at the CRC4 level. |
| 42 | RCSA | O | DS2181A | **Receive CRC4 Search Active.** This pin will transition high when the synchronizer searching for the CRC4 multiframe alignment word is active. |
| 43 | SDO | O | DS2181A | **Serial Data Out.** Control and status information from the onboard registers. Updated on falling edge of SCLK, 3-stated during serial port write or when $\overline{CS}$ is high. |
| 44 | CS | I | DS2181A | **Chip Select.** Must be low to write to or read from the serial port. |
| 45 | SCLK | I | DS2181A | **Serial Port Clock.** Used to read or write the serial port registers that control the DS2284. |

| PIN | SYMBOL | TYPE | DEVICE | DESCRIPTION |
|---|---|---|---|---|
| 46 | NC | | | **No Connect.** Does not connect to any internal signals. |
| 47 | RST | I | DS2181A | **Reset.** A high-low transition clears all internal registers and resets the receive side counters. A high-low transition will initiate a resync. |
| 48 | NC | | | **No Connect.** Does not connect to any internal signals. |
| 49 | RDMA | O | DS2181A | **Receive Distant Multiframe Alarm.** Transitions high when alarm detected; low when alarm cleared. |
| 50 | RCSYNC | O | DS2181A | **Receive CRC Sync.** Low-high transition indicates start of CRC4 multiframe; held high during CRC4 frame 0 through 7 and low during frames 8 through 15. |
| 51 | RAF | O | DS2181A | **Receive Alignment Frame.** High during frames containing the frame alignment signal, low otherwise. |
| 52 | RCLK | O | DS2188 | **Receive Clock.** A 2.048 MHz clock that is recovered from the incoming data stream at RTIP and RRING. |
| 53 | RSD | O | DS2181A | **Receive Signalling Data.** Extracted timeslot 16 data. |
| 54 | RCHCLK | O | DS2181A | **Receive Channel Clock.** 256 KHz clock which identifies channel boundaries. |
| 55 | RFSYNC | O | DS2181A | **Receive Frame Sync.** Extracted 8 KHz signal that indicates the beginning of each frame. |
| 56 | RSTS | O | DS2181A | **Receive Signalling Timeslot.** High during timeslot 16 of every frame, low otherwise. |
| 57 | ALN | I | DS2175 | **Align.** When forced low, $\overline{ALN}$ recenters the buffer on the next system side frame sync boundary as determined by SFSYNC. |
| 58 | SLIP | O | DS2175 | **Frame Slip.** Held low for 65 SYSCLK cycles when a slip occurs. Active low, open drain output. |
| 59 | FSD | O | DS2175 | **Frame Slip Direction.**<br>0 = buffer is empty; a frame was repeated.<br>1 = buffer is full; a frame was deleted. |
| 60 | RMSYNC | O | DS2181A | **Receive Multiframe Sync.** Extracted multiframe sync. rising edge indicates the start of a CAS multiframe. |
| 61 | RSER | O | DS2181A | **Receive Serial Data.** Received NRZ serial data, updated on the rising edge of RCLK. |
| 62 | SYSCLK | I | DS2175 | **System Clock.** A 1.544 MHz or 2.048 MHz data clock. |
| 63 | SSER | O | DS2175 | **System Serial Data.** Updated on the rising edge of SYSCLK. |
| 64 | SMSYNC | O | DS2175 | **System Multiframe Sync.** Slip-compensated multiframe output; used with RMSYNC to monitor depth of the DS2175 buffer real time. |
| 65 | SCLKSEL | I | DS2175 | **System Clock Select.** Tie to $V_{SS}$ for 1.544 MHz backplane applications; tie to $V_{DD}$ for 2.048 MHz backplane applications. |
| 66 | S/$\overline{P}$ | I | DS2175 | **Serial/Parallel Select.** Tie to $V_{SS}$ for parallel backplane applications; tie to $V_{DD}$ for serial backplane applications. |
| 67 | SCHCLK | O | DS2175 | **System Channel Clock.** Transitions high on channel boundaries. |
| 68 | SFSYNC | I | DS2175 | **System Frame Sync.** Rising edge establishes system side frame boundaries. |

## ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Voltage on Any Pin Relative to Ground | -1.0V to 7.0V |
| Operating Temperature | 0°C to +70°C |
| Storage Temperature | -55°C to +125°C |

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Logic 1 | $V_{IH}$ | 2.0 | | $V_{CC}$ +0.3 | V | 1 |
| Logic 0 | $V_{IL}$ | -0.3 | | +0.8 | V | 1 |
| Supply | $V_{DD}$ | 4.75 | | 5.25 | V | |

## CAPACITANCE

($t_A$ = 25°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | | | 20 | pF | 1 |
| Output Capacitance | $C_{OUT}$ | | | 40 | pF | 1 |

## DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; $V_{DD}$ = 5V ± 5%)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Supply Current | $I_{DD}$ | | 70 | 110 | mA | 2 |
| Input Leakage | $I_I$ | -10 | | +10 | µA | 3,5 |
| Output Leakage | $I_O$ | -1.0 | | +1.0 | µA | 4 |
| Output Current (2.4V) | $I_{OH}$ | -1.0 | | | mA | 6 |
| Output Current (0.4V) | $I_{OL}$ | +4.0 | | | mA | 6 |

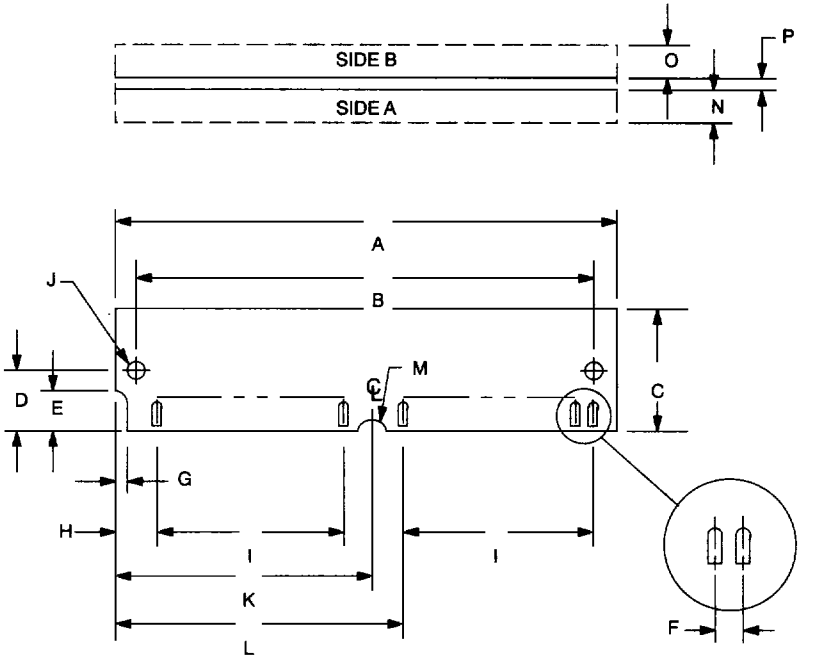
## NOTES:

1. Does not apply to RTIP, RRING, TTIP, or TRING.
2. $V_{DD}$ = 5.25V and TCLK = 2.048 MHz.
3. $V_{SS} < V_{IN} < V_{DD}$.
4. Applies to open collector outputs ($\overline{LF}$, $\overline{SLIP}$, $\overline{INT}$).
5. All inputs except RTIP and RRING.
6. All outputs except TTIP and TRING.

## NOTE:

All AC Electrical Parameters can be found in the individual data sheets on the DS2187, DS2186, DS2181A, DS2188, and DS2175.

## DS2284 ENHANCED CEPT LINE CARD STIK




| PKG | 68-PIN | |
|---|---|---|
| DIM | MIN | MAX |
| A IN. | 4.045 | 4.055 |
| B IN. | 3.779 | 3.789 |
| C IN. | 0.845 | 0.855 |
| D IN. | 0.395 | 0.405 |
| E IN. | 0.245 | 0.255 |
| F IN. | 0.050 BSC | |
| G IN. | 0.075 | 0.085 |
| H IN. | 0.245 | 0.255 |
| I IN. | 1.650 BSC | |
| J IN. | 0.120 | 0.130 |
| K IN. | 1.085 | 1.095 |
| L IN. | 2.020 | 2.030 |
| M IN. | 0.057 | 0.067 |
| N IN. | | 0.225 |
| O IN. | | 0.235 |
| P IN. | | 0.054 |