

## CT2 Front End IC

### Description

U7001BG is a monolithic GaAs transmit/ receive front end with power amplifier, low noise amplifier and antenna switch. It is specially designed for operation in CT2 band and suitable for a frequency range of 839 MHz to 952 MHz with external matching.

Electrostatic sensitive device.  
Observe precautions for handling.



### Features

- Low supply voltage 3.6 V typical (min. 2.7 V)
- High power added efficiency (typ. 40%)
- Low power consumption in receive mode
- Power down control pin for low noise amplifier
- Gain control of power amplifier
- Low noise amplifier
- Optional high output power 50 mW @ 5 V supply voltage
- SSO20 plastic package

### Benefits

- Extended talk time due to low power consumption and high PAE
- Few external components and very small package save space

### Block Diagram

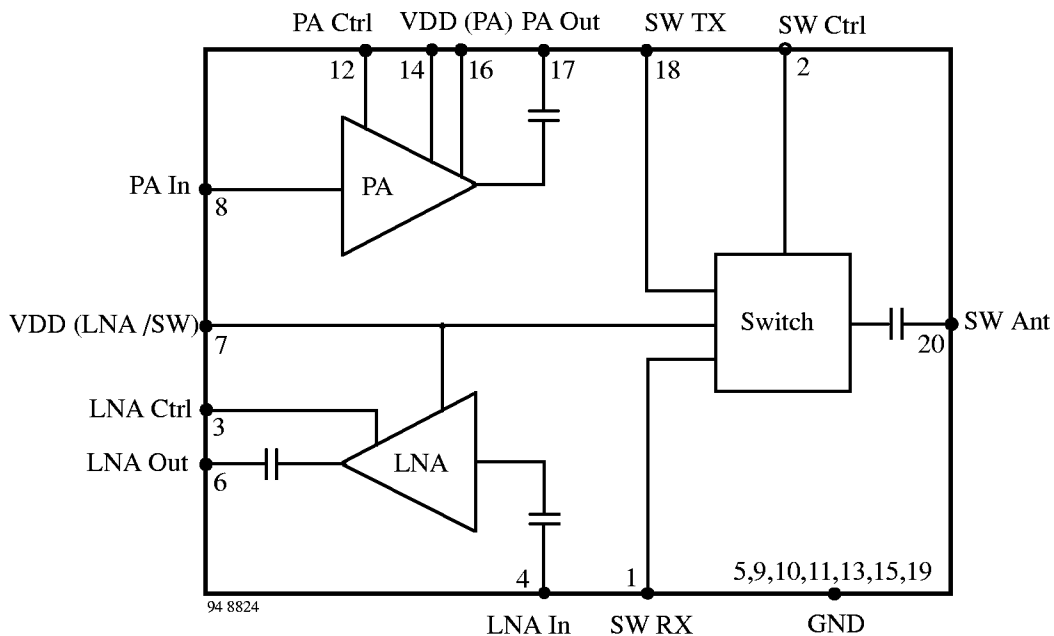
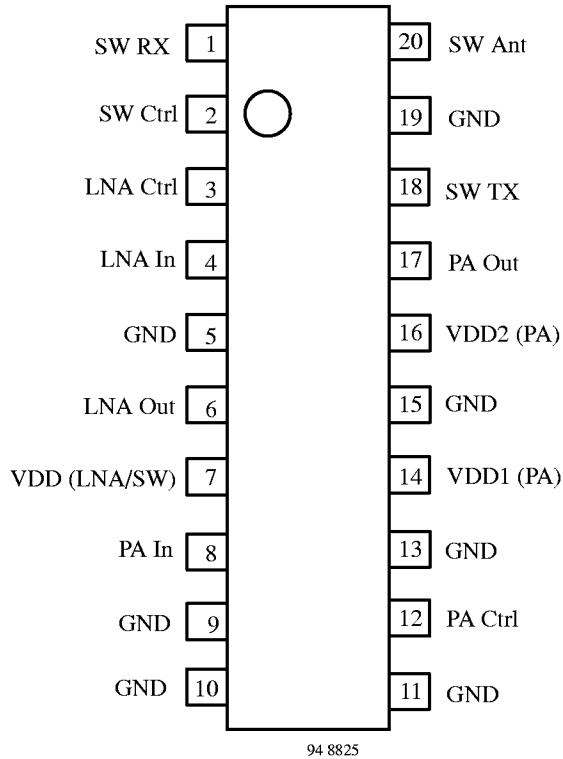


Figure 1. Block diagram

## Pin Description



Pin	Symbol	Function
1	SW RX	Switch RX output
2	SW Ctrl	Switch control input
3	LNA Ctrl	LNA control input
4	LNA In	Low noise amplifier input
5,9,10, 11,13 15,19	GND	Ground
6	LNA Out	LNA output
7	VDD (LNA/SW)	LNA & Switch power supply voltage
8	PA In	Power amplifier input
12	PA Ctrl	PA control input
14	VDD1(PA)	PA power supply voltage 1
16	VDD2(PA)	PA power supply voltage 2
17	PA Out	PA output
18	SW TX	Switch TX input
20	SW Ant	Switch antenna output

Figure 2. Pinning SSO20

## Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltages Pins 7, 14 and 16	$V_{DD}$	+ 7	V
Input voltages Pins 4, 8, 18 and 20	$V_i$	0 to VDD	V
Control voltages Pins 2, 3 and 12	$V_C$	0 to VDD	V
Channel temperature	$T_{ch}$	125	°C
Storage-temperature range	$T_{stg}$	- 40 to + 125	°C

## Thermal Resistance

Parameters	Symbol	Value	Unit
Channel ambient SSO20	$R_{thch}$	140	K/W

## Operating Range

Parameters	Symbol	Value	Unit
Supply voltages Pins 7, 14 and 16	$V_{DD}$	2.7 to 5.25	V
Ambient-temperature range	$T_{amb}$	- 40 to + 85	°C

## Electrical Characteristics Low Noise Amplifier (LNA)

Test conditions (unless otherwise specified):  $V_{DD} = 3.3\text{ V}$ ,  $T_{amb} = 25^{\circ}\text{C}$ , referred to test circuit.  
System impedance  $Z_o = 50\ \Omega$ ,  $f_{RF} = 866\text{ MHz}$

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply-voltage range	Pin 7	$V_{DD}$	2.9	3.6	5.25	V
Supply current	@ $V_{DD} = 2.9\text{ V}$ , Pin 7	$I_s$		3.5	5.0	mA
Supply current	@ $V_{DD} = 2.9\text{ V}$ , LNA Ctrl = 0 V: LNA "off" Pin 7	$I_s$		0.5		mA
Frequency range	Pin 4	f	839	866	952	MHz
Linear power gain	Pins 4 and 6	$G_p$		14		dB
Noise figure	Pins 4 and 6	NF		2.0	2.5	dB
Compression	Pins 4 and 6	P_1dB	-29	-27		dBm
Third-order input intercept point	Pins 4 and 6	IIP3	-19	-17		dBm
Isolation	Pins 6 and 4 (from output to input)	$Isol_{LNA}$	20	25		dB
Input impedance	Pin 4			50		$\Omega$
Output impedance	Pin 6		50	100		$\Omega$
LNA control voltage	LNA Mode "off" Pin 3 LNA Mode "on"	$V_{LNA\ Ctrl}$	$V_{DD}-0.5$	0.0 $V_{DD}$	0.5	V V

Test conditions (unless otherwise specified):  $V_{DD} = 2.9\text{ V}$ ,  $T_{amb} = 25^{\circ}\text{C}$ , referred to test circuit.  
System impedance  $Z_o = 50\ \Omega$ ;  $f_{RF} = 866\text{ MHz}$

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply-voltage range	Pin 7	$V_{DD}$	2.9	3.6	5.25	V
Supply current	@ $V_{DD} = 2.7\text{ V}$ , Pin 7	$I_s$		3.0	4.0	mA
Supply current	@ $V_{DD} = 2.7\text{ V}$ , LNA Ctrl = 0 V: LNA "off" Pin 7	$I_s$		0.5		mA
Frequency range	Pin 4	f	839	866	952	MHz
Linear power gain	Pins 4 and 6	$G_p$		12		dB
Noise figure	Pins 4 and 6	NF		2.0	2.5	dB
Compression	Pins 4 and 6	P_1dB	-29	-28		dBm
Third-order input intercept point	Pins 4 and 6	IIP3	-19	-18		dBm
Isolation	Pins 6 and 4 (from output to input)	$Isol_{LNA}$	20	25		dB
Input impedance	Pin 4			50		$\Omega$
Output impedance	Pin 6		50	100		$\Omega$
LNA control voltage	LNA Mode "off" Pin 3 LNA Mode "on"	$V_{LNA\ Ctrl}$	$V_{DD}-0.5$	0.0 $V_{DD}$	0.5	V V

## Electrical Characteristics Power Amplifier

Test conditions (unless otherwise specified);  $V_{DD} = 5.0\text{ V}$ , PA Ctrl = 5 V,  $T_{amb} = 25^\circ\text{C}$ , referred to test circuit.  
System Impedance  $Z_o = 50\ \Omega$ ;  $f_{RF} = 866\text{ MHz}$

Parameters	Test Conditions / Pins	Symbol	Min	Typ	Max.	Unit
Supply-voltage range	Pins 14 and 16	$V_{DD1,2}$	2.7	3.6	5.25	V
Supply current	Pins 14 and 16	$I_s$		33	40	mA
Supply current	Pin 12	$I_{Ctrl}$		5.0	6.0	mA
Frequency range	Pin 8	$f$	839	866	952	MHz
Linear power gain	Pins 8 and 17	$G_p$	34	36		dB
<b>Power response</b>	@ $P_{in} = -14\text{ dBm}$					
Output power	At 3 dB gain compression; Pin 17	$P_{out}$	17	18		dBm
Gain control range	Pins 17 and 12	$G_c$	30	33		dB
Gain control voltage	$P_{out} = P_{out_{max}}$	$V_{PA\ Ctrl}$		4.5	$V_{DD}$	V
Gain control voltage	$P_{out} = P_{out_{max}} - 16\text{ dB}$	$V_{PA\ Ctrl}$		1.2		V
Gain control voltage	$P_{out} = P_{out_{min}}$	$V_{PA\ Ctrl}$		0.0		V
<b>Switching time</b>	Pins 12 and 17					
Turn-on time	90% $P_{out_{max}}$	$t_{on}$		2		$\mu\text{s}$
Turn-off time	10% $P_{out_{max}}$	$t_{off}$		5		$\mu\text{s}$
Harmonic levels	At 3 dB gain compression		-18	-25		dBc
Isolation	Pins 17 and 8 (from output to input)	$Isol_{PA}$	42	45		dB
Input matching	Pin 8	$VSWR_{in}$	1.9 : 1	1.6 : 1		
Output matching	Pin 17	$VSWR_{out}$		2.0 : 1		
Power added efficiency	Pin 17	$\eta_{PAE}$		40		%
Input impedance	Pin 8	$Z_{in}$		50		$\Omega$
Output impedance	Pin 17	$Z_{out}$		50		$\Omega$

## Electrical Characteristics Power Amplifier

Test conditions (unless otherwise specified);  $V_{DD} = 3.6$  V, PA Ctrl = 3.6 V,  $T_{amb} = 25^{\circ}\text{C}$ , referred to test circuit.  
System impedance  $Z_o = 50 \Omega$ ;  $f_{RF} = 866$  MHz

Parameters	Test Conditions / Pins	Symbol	Min	Typ	Max	Unit
Supply-voltage range	Pins 14 and 16	$V_{DD1,2}$	2.7	3.6	5.25	V
Supply current	Pins 14 and 16	$I_s$		30	36	mA
Supply current	Pin 12	$I_{Ctrl}$		5.0	6.0	mA
Frequency range	Pin 8	$f$	839	866	952	MHz
Linear power gain	Pins 8 and 17	$G_p$	32	35		dB
<b>Power response</b>	@ $P_{in} = -14$ dBm					
Output power	At 3 dB gain compression; Pin 17	$P_{out}$	15	17		dBm
Gain control range	Pins 17 and 12	$G_c$	30	33		dB
Gain control voltage	$P_{out} = P_{out_{max}}$	$V_{PA\ Ctrl}$		2.9	$V_{DD}$	V
Gain control voltage	$P_{out} = P_{out_{max}} - 16$ dB	$V_{PA\ Ctrl}$		1.2		V
Gain control voltage	$P_{out} = P_{out_{min}}$	$V_{PA\ Ctrl}$		0.0		V
<b>Switching time</b>	Pins 12 and 17					
Turn-on time	90% $P_{out_{max}}$	$t_{on}$		2		$\mu\text{s}$
Turn-off time	10% $P_{out_{max}}$	$t_{off}$		5		$\mu\text{s}$
Harmonic levels	At 3 dB gain compression		-18	-25		dBc
Isolation	Pins 17 and 8 (from output to input)	$Isol_{PA}$	42	45		dB
Input matching	Pin 8	$VSWR_{in}$	1.9 : 1	1.6 : 1		
Output matching	Pin 17	$VSWR_{out}$		2.0 : 1		
Power added efficiency	Pin 17	$\eta_{PAE}$		45		%
Input impedance	Pin 8	$Z_{in}$		50		$\Omega$
Output impedance	Pin 17	$Z_{out}$		50		$\Omega$

## Electrical Characteristics Power Amplifier

Test conditions (unless otherwise specified);  $V_{DD} = 2.7\text{ V}$ , PA Ctrl = 2.7 V,  $T_{amb} = 25^{\circ}\text{C}$ , referred to test circuit.  
System impedance  $Z_o = 50\ \Omega$ ;  $f_{RF} = 866\text{ MHz}$

Parameters	Test Conditions / Pins	Symbol	Min	Typ	Max.	Unit
Supply-voltage range	Pins 14 and 16	$V_{DD1,2}$	2.7	3.6	5.25	V
Supply current	Pins 14 and 16	$I_s$		25	30	mA
Supply current	Pin 12	$I_{Ctrl}$		4.5	5.5	mA
Frequency range	Pin 8	$f$	839	866	952	MHz
Linear power gain	Pins 8 and 17	$G_p$	30	32		dB
<b>Power response</b>	@ $P_{in} = -15\text{ dBm}$					
Output power	At 3 dB gain compression; Pin 17	$P_{out}$	12	14		dBm
Gain control range	Pins 17 and 12	$G_c$	30	33		dB
Gain control voltage	$P_{out} = P_{out_{max}}$	$V_{PA\ Ctrl}$		2.7	$V_{DD}$	V
Gain control voltage	$P_{out} = P_{out_{max}} - 16\text{ dB}$	$V_{PA\ Ctrl}$		1.5		V
Gain control voltage	$P_{out} = P_{out_{min}}$	$V_{PA\ Ctrl}$		0.0		V
<b>Switching time</b>	Pins 12 and 17					
Turn-on time	90% $P_{out_{max}}$	$t_{on}$		2		$\mu\text{s}$
Turn-off time	10% $P_{out_{max}}$	$t_{off}$		5		$\mu\text{s}$
Harmonic levels	At 3 dB gain compression		-20	-25		dBc
Isolation	Pins 16 and 8 (from output to input)	$Isol_{PA}$	42	45		dB
Input matching	Pin 8	$V_{SWR_{in}}$	1.9 : 1	1.4 : 1		
Output matching	Pin 16	$V_{SWR_{out}}$		2.0 : 1		
Power added efficiency	Pin 16	$\eta_{PAE}$		35		%
Input impedance	Pin 8	$Z_{in}$		50		$\Omega$
Output impedance	Pin 16	$Z_{out}$		50		$\Omega$

## Electrical Characteristics Antenna Switch

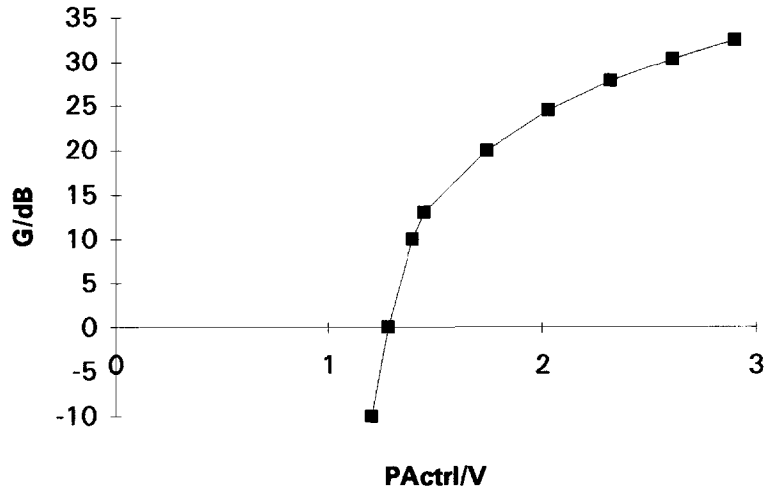
Test conditions (unless otherwise specified);  $V_{DD} = 3.6\text{ V}$ ,  $T_{amb} = 25^{\circ}\text{C}$ , referred to test circuit.  
System impedance  $Z_o = 50\ \Omega$ ;  $f_{RF} = 866\text{ MHz}$

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage range	Pin 7	$V_{DD}$	2.7	3.6	5.0	V
Frequency range	Pins 1, 18 and 20	f	839	866	952	MHz
Insertion loss	@ $P_{in} = +16\text{ dBm}$ ; Pin 18 to Pin 20; "TX Mode"	$IL_{TX}$		1.0	1.3	dB
Isolation	@ $P_{in} = +16\text{ dBm}$ ; Pin 18 to Pin 1; "TX Mode"	$Isol_{TX}$	12	15		dB
Insertion loss	@ $P_{in} = -26\text{ dBm}$ ; Pin 20 to Pin 1; "RX Mode"	$IL_{RX}$		1.0	1.3	dB
Isolation	@ $P_{in} = -26\text{ dBm}$ ; Pin 20 to Pin 18; "RX Mode"	$Isol_{TX}$	16	18		dB
Switch control	RX Mode; Pin 2	$V_{SW\ Ctrl}$	0	0	0.05	V
	TX Mode	$V_{SW\ Ctrl}$	$V_{DD} - 0.5$	$V_{DD}$	$V_{DD} + 0.5$	V
Input impedance	TX Mode; Pin 18	$Z_{in}$		50		$\Omega$
Input impedance	RX Mode; Pin 1	$Z_{in}$		50		$\Omega$
Output impedance	RX TX-Mode; Pin 20	$Z_{out}$		50		$\Omega$

Test conditions (unless otherwise specified);  $V_{DD} = 2.7\text{ V}$ ,  $T_{amb} = 25^{\circ}\text{C}$ , referred to test circuit.  
System impedance  $Z_o = 50\ \Omega$ ;  $f_{RF} = 866\text{ MHz}$

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply-voltage range	Pin 7	$V_{DD}$	2.7	3.6	5.0	V
Frequency range	Pins 1, 18 and 20	f	839	866	952	MHz
Insertion loss	@ $P_{in} = +14\text{ dBm}$ ; Pin 18 to Pin 20; "TX Mode"	$IL_{TX}$		1.0	1.3	dB
Isolation	@ $P_{in} = +14\text{ dBm}$ ; Pin 18 to Pin 1; "TX Mode"	$Isol_{TX}$	11	13		dB
Insertion loss	@ $P_{in} = -26\text{ dBm}$ ; Pin 20 to Pin 1; "RX Mode"	$IL_{RX}$		1.0	1.3	dB
Isolation	@ $P_{in} = -26\text{ dBm}$ ; Pin 20 to Pin 18; "RX-Mode"	$Isol_{TX}$	15			dB
Switch control	RX Mode; Pin 2	$V_{SW\ Ctrl}$	0	0	0.05	V
	TX Mode; Pin 2	$V_{SW\ Ctrl}$	$V_{DD} - 0.5$	$V_{DD}$	$V_{DD} + 0.5$	V
Input impedance	TX Mode; Pin 18	$Z_{in}$		50		$\Omega$
Input impedance	RX Mode; Pin 1	$Z_{in}$		50		$\Omega$
Output impedance	RX TX-Mode; Pin 20	$Z_{out}$		50		$\Omega$

### Gain Variation with Vctrl



94 8838

Figure 3. Gain variation of power amplifier with switch and filter. @  $V_{DD} = 3.6$  V (typical values)

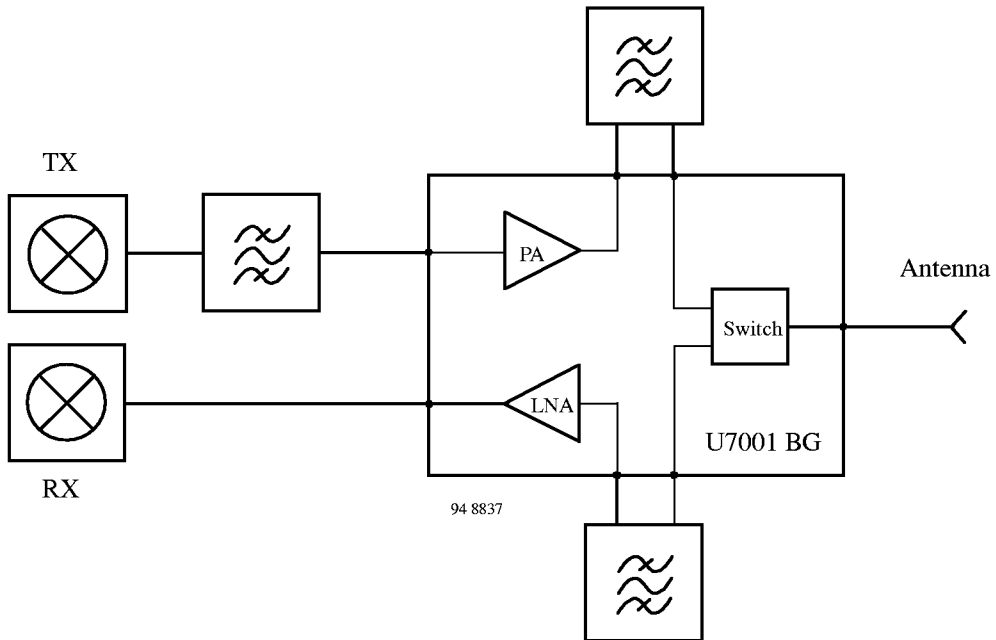


Figure 4. Application 1

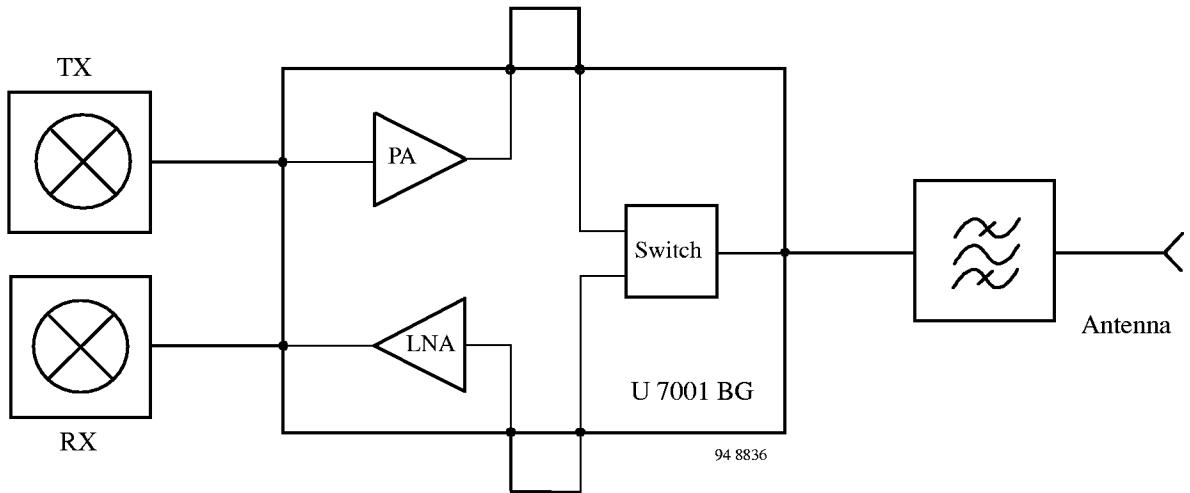


Figure 5. Application 2

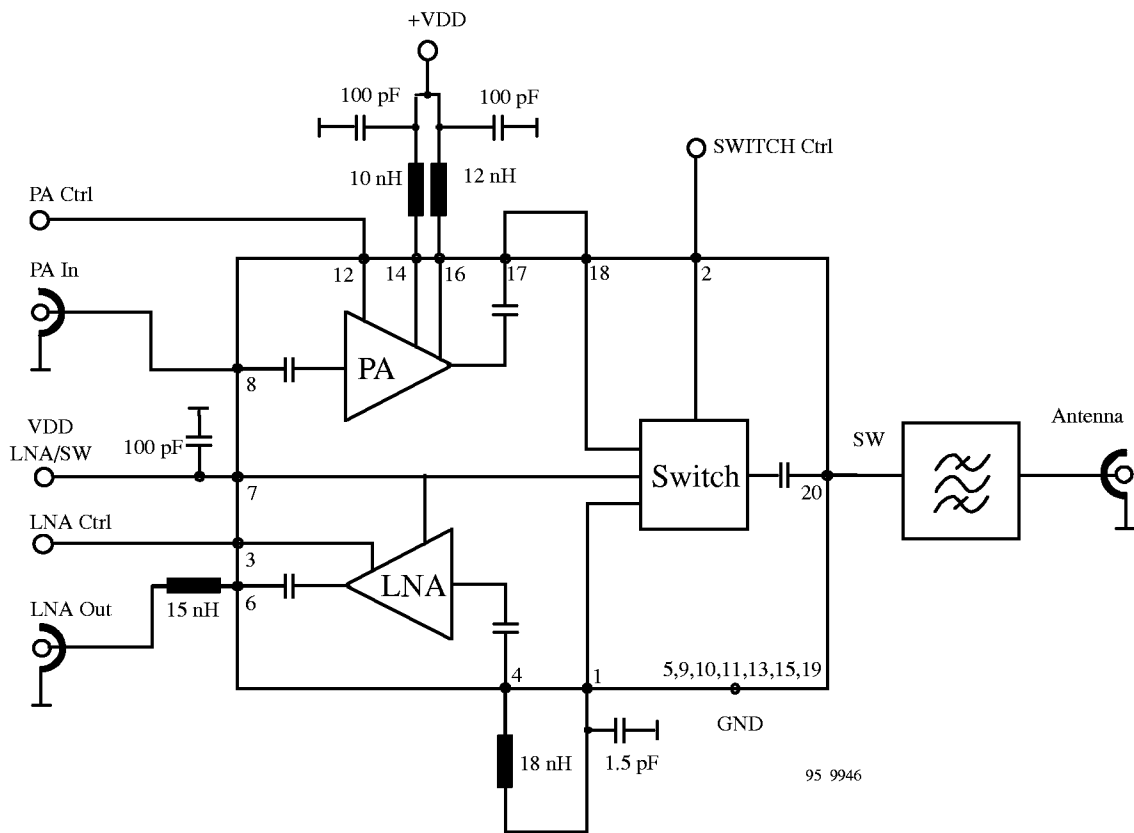


Figure 6. Application for minimal component count

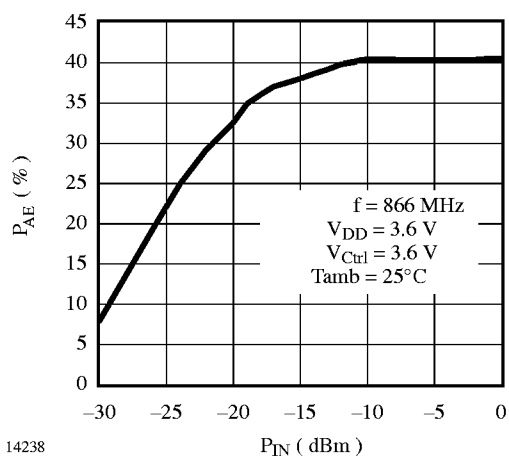


Figure 7.  $P_{AE}$  versus  $P_{IN}$

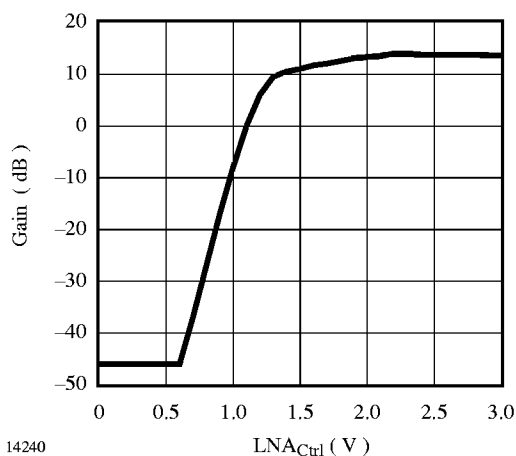


Figure 9. LNA gain versus control voltage

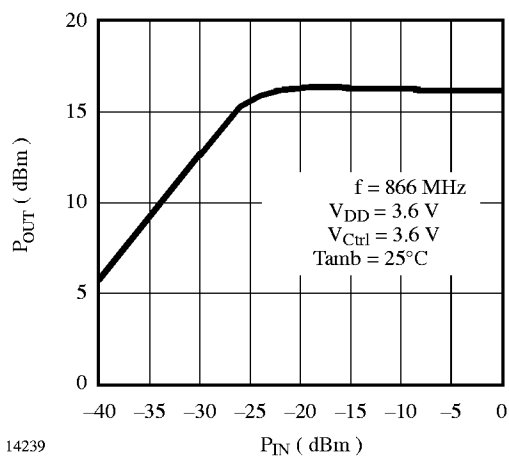


Figure 8.  $P_{OUT}$  versus  $P_{IN}$

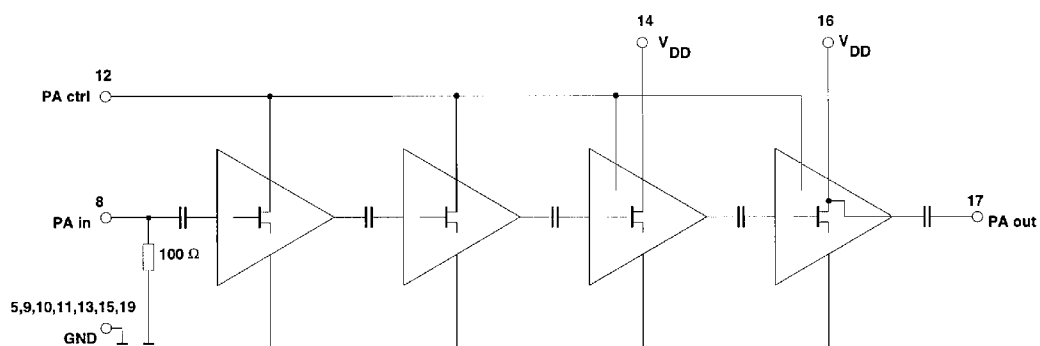
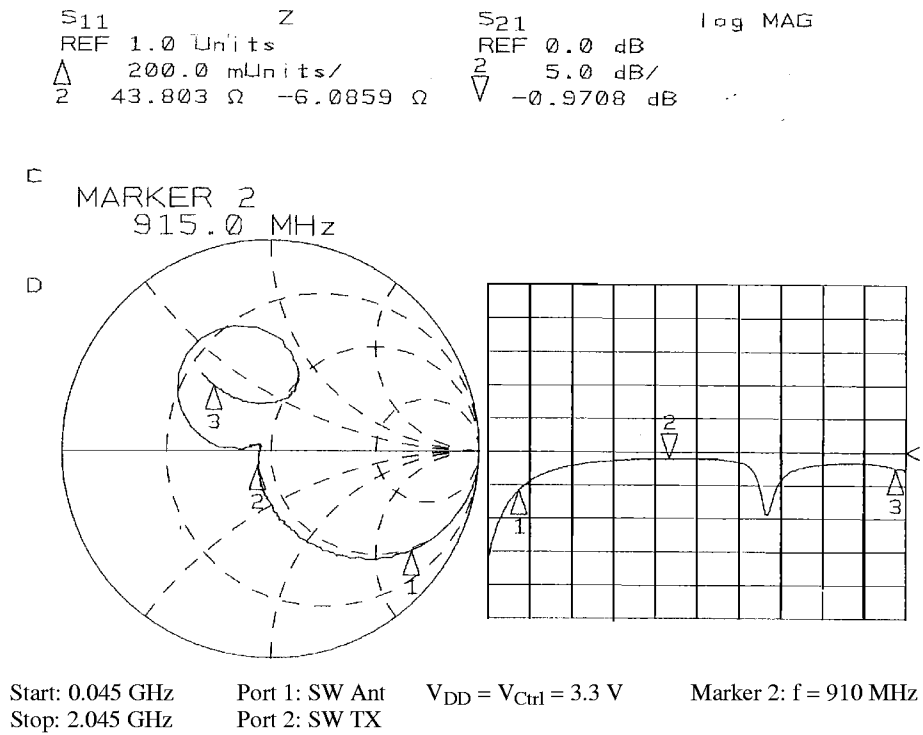
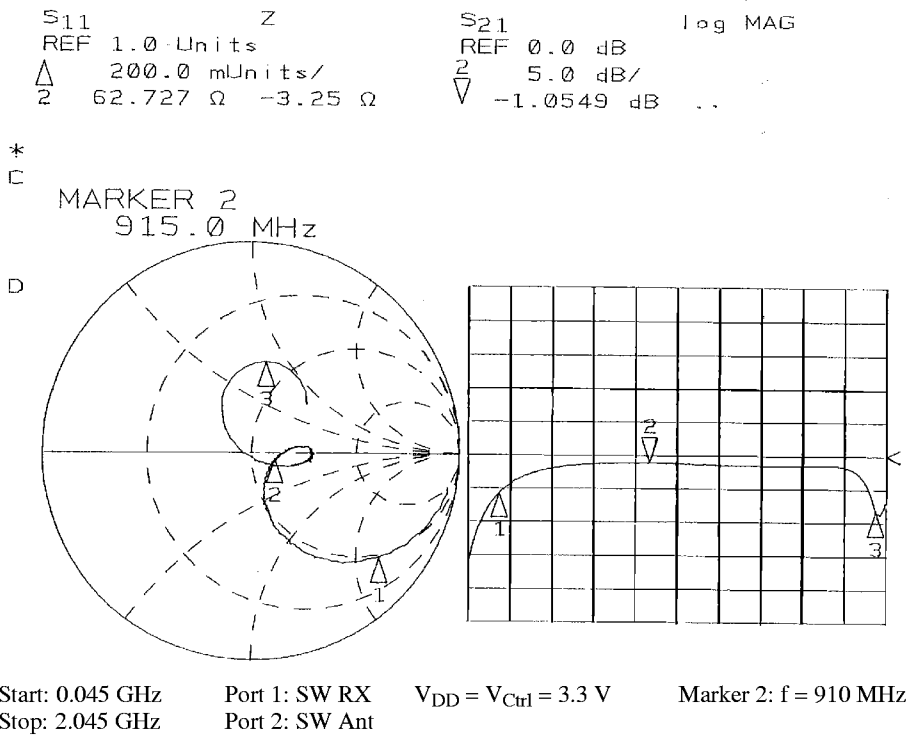


Figure 10. Power amplifier – circuit topology



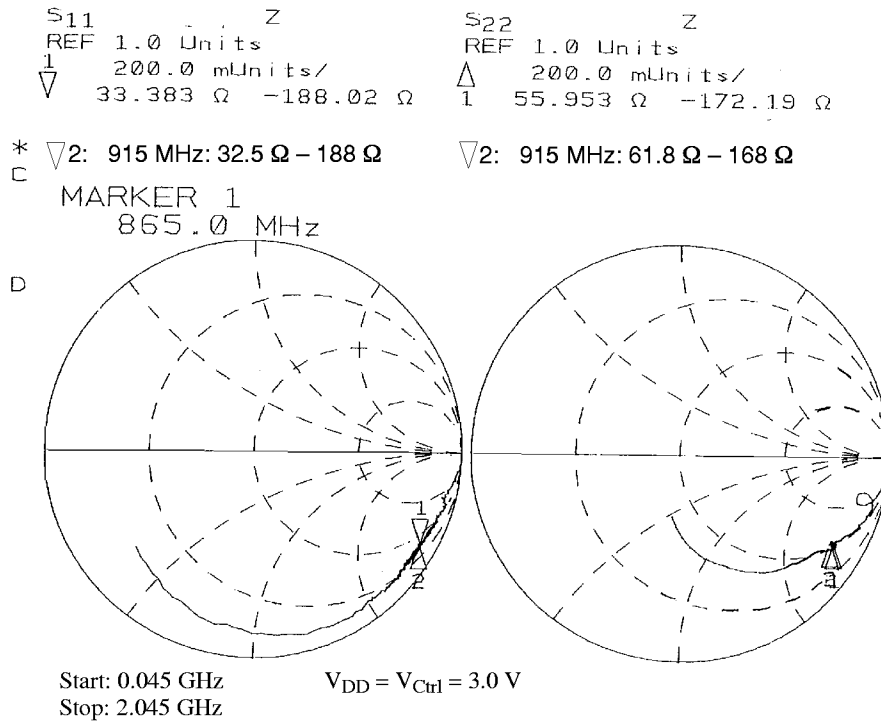
14241

Figure 11. Switch TX insertion loss



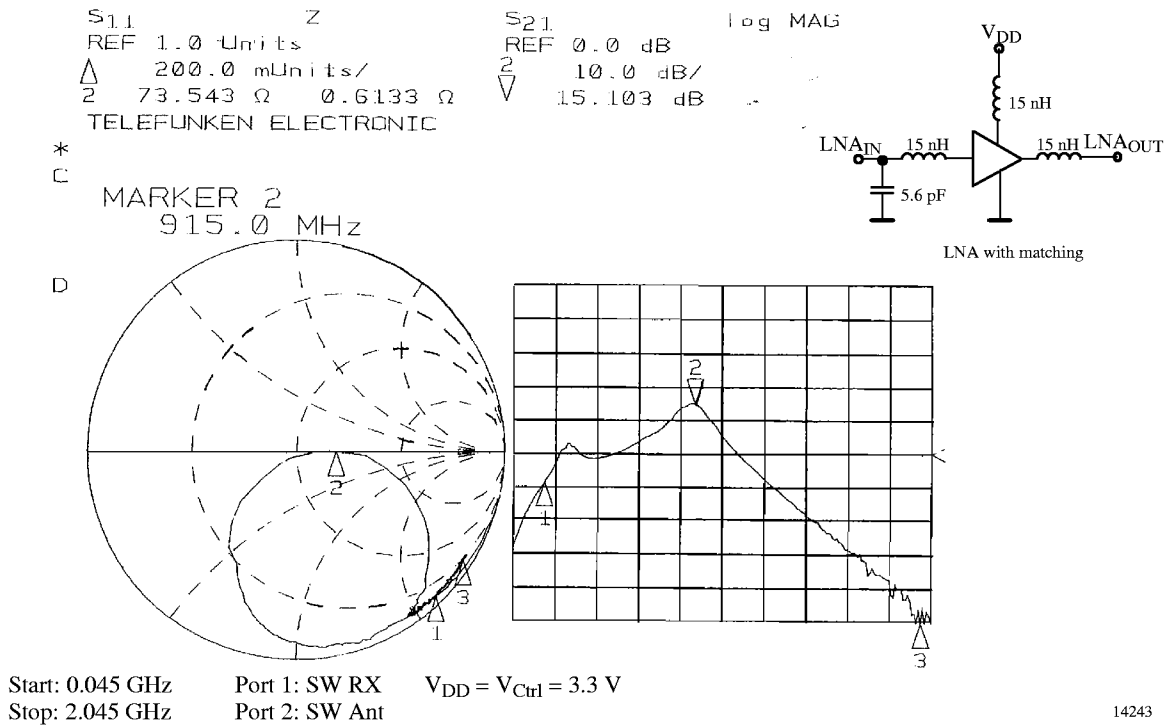
14242

Figure 12. Switch RX insertion loss



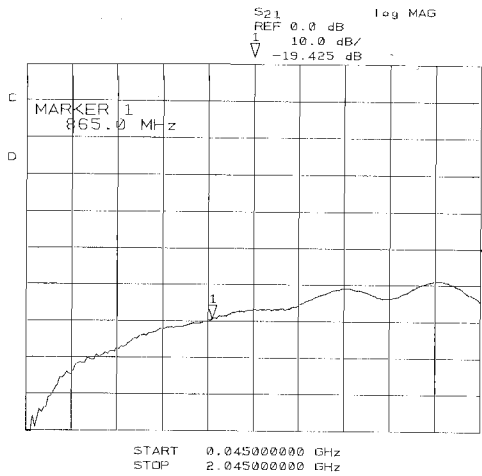
14244

Figure 13. LNA without matching



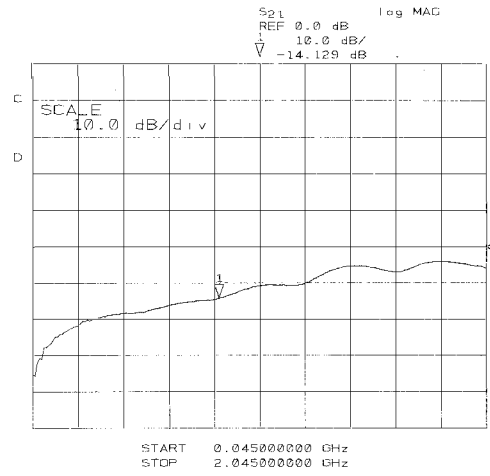
14243

Figure 14. LNA with external matching



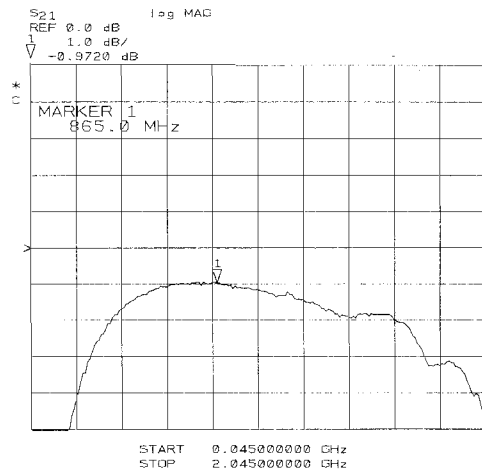
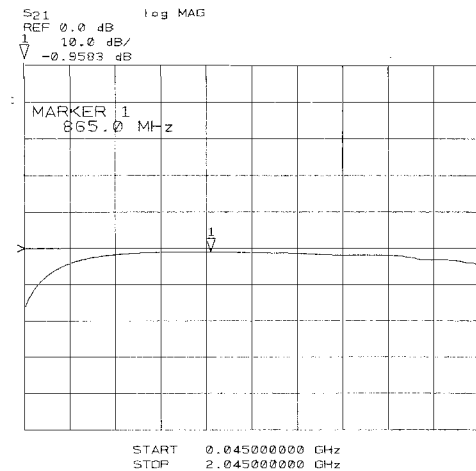
14245

Figure 15. Switch Ant – TX isolation  
 $V_{DD} = 3.0\text{ V}$ ,  $V_{Ctrl} = 0\text{ V}$



14246

Figure 16. Switch Ant – RX isolation  
 $V_{DD} = 3.0\text{ V}$ ,  $V_{Ctrl} = 3.0\text{ V}$



SW RX – Ant insertion loss

$V_{DD} = 3.0\text{ V}$

$V_{Ctrl} = 0\text{ V}$

14247

Figure 17. Matched on both sides

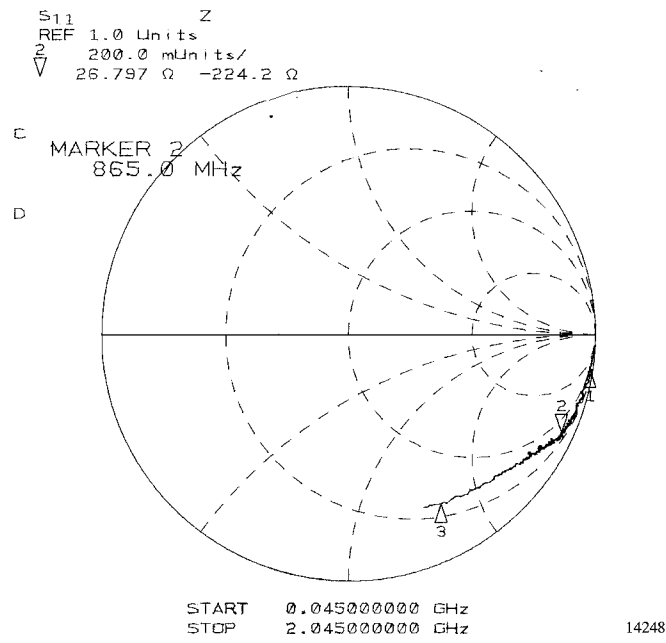
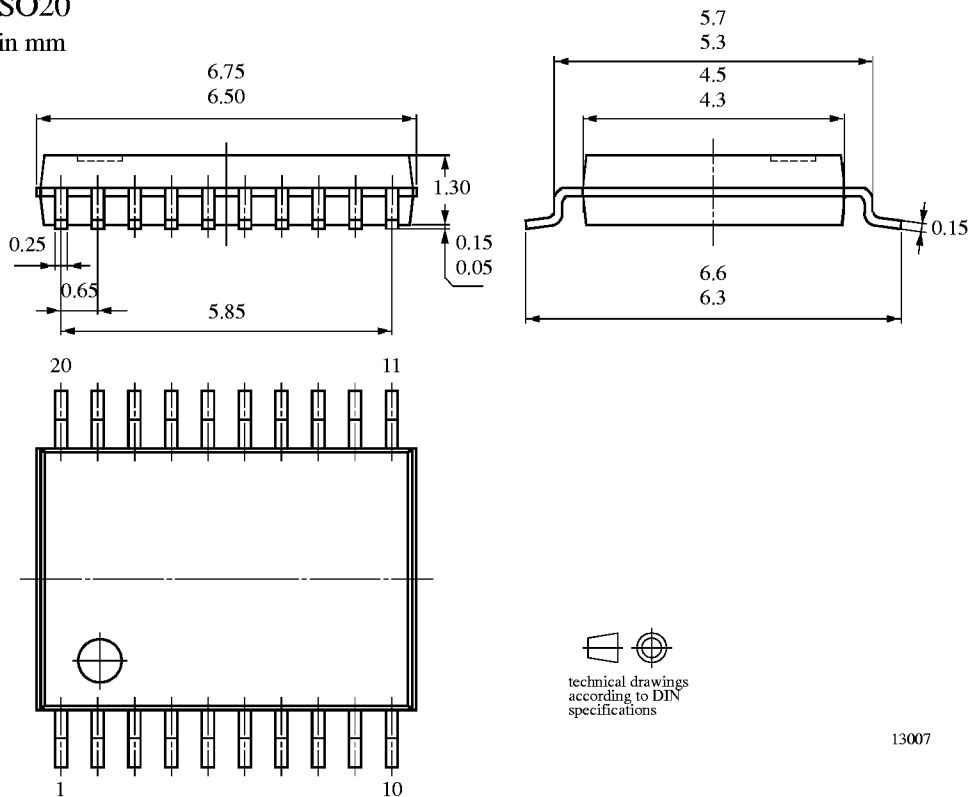


Figure 18. LNA switched off,  $V_{DD} = 3.0$  V

## Package Information

Package SSO20  
 Dimensions in mm



## Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

**TEMIC Semiconductor GmbH** has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

**TEMIC Semiconductor GmbH** can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

**We reserve the right to make changes to improve technical design and may do so without further notice.**

Parameters can vary in different applications. All operating parameters must be validated for each customer application by the customer. Should the buyer use TEMIC Semiconductors products for any unintended or unauthorized application, the buyer shall indemnify TEMIC Semiconductors against all claims, costs, damages, and expenses, arising out of, directly or indirectly, any claim of personal damage, injury or death associated with such unintended or unauthorized use.

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