HARRIS

HM-91M2-8

1M Bit Asynchronous CMOS Static RAM Module

June 1989

Features

- **Low Standby Current 900µA**
- **Low Operating Supply Current 10/20mA**
- **Fast Address Access Time 180ns**
- **Low Data Retention Supply Voltage.................................. 2.0V**
- **CMOS/TTL Compatible Inputs/Outputs**
- **Buffered Address and Control Lines**
- **48 Pin DIP Pinout ....2.66 x 1.3 x 0.3"**
- **Operating Temperature Range .... -55°C to +125°C**

Description

The HM-91M2-8 is a fully buffered 1,048,572 bit CMOS RAM module consisting of sixteen HM-65642 8K x 8 CMOS RAMs, two 82C82 CMOS octal buffers, and two HCT-138 CMOS 3:8 decoders in leadless chip carriers mounted on a multi-layer, co-fired, ceramic substrate. The HM-91M2-8 CMOS RAM module is organized as two 64K x 8 RAM arrays sharing a common address bus and write enable input. Separate data input/output buses allow the user to format the HM-91M2-8 as either a 64K x 16 or 128K x 8 bit array.

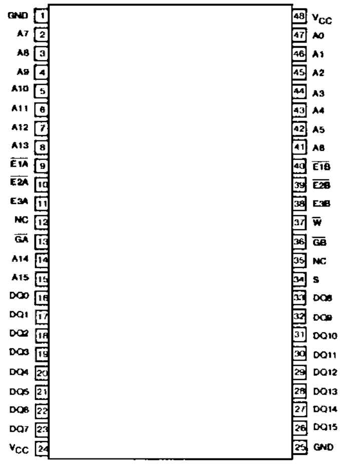
The on-substrate CMOS buffers and decoders on the HM-91M2-8 reduce the system package count and minimize the capacitive load on the system address and control buses. In addition to this, the HM-91M2-8 has on-substrate decoupling capacitors mounted in leadless chip carriers to reduce power supply noise and minimize the need for external decoupling while ensuring high reliability, even in harsh environments.

The HM-91M2-8 is physically constructed as an extra wide 48 pin dual-in-line package with standard 0.1" centers between pins to combine the high density of CMOS and leadless chip carriers with the ease of use of DIP packaging.

The HM-65642 RAMs used on the HM-91M2-8 module are full CMOS devices, utilizing arrays of six-transistor (6T) memory cells for the most stable and lowest possible standby and data retention supply current over full military operating temperature range. In addition to this, the high stability of the 6T cell provides excellent protection against soft errors due to power supply noise and alpha particles. This stability also improves the radiation tolerance of the module over that of RAMs utilizing four transistor (4T) Mix-MOS memory cells.

Pinout

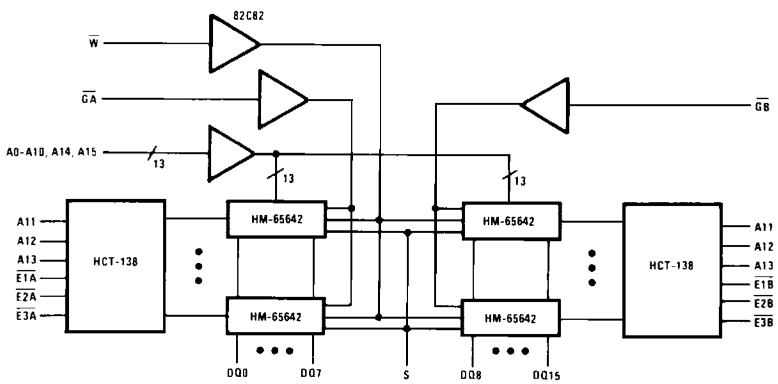
TOP VIEW



PIN NAMES

PIN	DESCRIPTION
A	Address Input
DQ	Data Input/Output
$\overline{GX}$	Output Enable
$\overline{EXX}$	Chip Enable
$\overline{W}$	Write Enable
NC	No Connection
S	Module Select

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage .... +7.0V
Input, Output or I/O Voltage Applied .... GND-0.3V to VCC +0.3V
Storage Temperature Range .... -65°C to +150°C
Gate Count .... 1619000 Gates
Junction Temperature .... +175°C
Lead Temperature (Soldering, Ten Seconds) .... +300°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range .... -55°C to +125°C

D.C. Electrical Specifications VCC = 5V ± 10%; T_A = -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB1	Standby Supply Current (CMOS)	-	900	µA	IO = 0, E3 = S = 0.3V, VCC = 5.5V, VIN = VCC or GND
ICCSB	Standby Supply Current (TTL)	-	2.0	mA	IO = 0, $\overline{E1}$ = $\overline{E2}$ = VIH, E3 = S = VIL, VCC = 5.5V, VIN = VCC or GND
ICCEN	Enabled Supply Current 128K x 8 64K x 16	-	5.0 10	mA mA	IO = 0, $\overline{E1}$ = $\overline{E2}$ = VIL, E3 = VIH, S = VCC -0.3V, VCC = 5.5V, VIN = VCC or GND
ICCOP	Operating Supply Current 128K x 8 (Note 2) 64K x 16	-	10 20	mA mA	IO = 0, f = 1MHz, $\overline{E1}$ = $\overline{E2}$ = VIL, S = VCC E3 = VIH, VCC = 5.5V, VIN = VCC or GND
ICCDR	Data Retention Supply Current	-	750	µA	E3 = S = 0.3V, VCC = 2.0V, VIN = VCC or GND
II	Input Leakage Current (Except S)	-1.0	+1.0	µA	VIN = VCC or GND, VCC = 5.5V
IIS	Module Select Input Current	-5	+5	µA	VIN = VCC or GND, VCC = 5.5V
IIOZ	I/O Leakage Current	-5	+5	µA	VIO = VCC or GND, VCC = 5.5V
VCCDR	Data Retention Supply Voltage	2.0	-	V	
VOL	Output Voltage Low	-	0.4	V	IOL = 4.0mA, VCC = 4.5V
VOH1	Output Voltage High	2.4	-	V	IOH = -1.0mA, VCC = 4.5V
VOH2	Output Voltage High (Note 3)	VCC-0.4		V	IOH = -100µA, VCC = 4.5V
VIL	Input Voltage Low	-0.3	0.8	V	
VIH	Input Voltage High	2.4	VCC+0.3	V	

Capacitance (Note 3)

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Except S)	25	pF	f = 1MHz, VA = VCC or GND
CDQ	Data I/O Capacitance	150	pF	f = 1MHz, VDQ and VG = VCC or GND
CIS	Module Select Input Capacitance	150	pF	f =1MHz, VEN = VCC or GND

NOTES:

1. All devices tested at worst case temperature and supply voltage limits.
2. Typical derating: 128K x 8: 5mA/MHz increase in ICCOP; 64K x 16: 10mA/MHz.
3. Guaranteed but not tested.
4. Input pulse levels: 0 to 3.0V; Input rise and fall times: 10ns max; Input and output timing reference level: 1.5V; Output load: 1TTL gate equivalent and CL = 100pF min including scope and jig - for CL greater than 100pF, access time is derated by 0.15ns/pF.
5. Enable valid (EV) in a parameter is determined the last transition that results in the combination of $\overline{E1}$ low, $\overline{E2}$ low and E3 high. Enable invalid (EX) in a parameter is determined by the first transition that results in any other combination than $\overline{E1}$ low, $\overline{E2}$ low and E3 high.

A.C. Electrical Specifications (Notes 1, 4) VCC = 5V ±10%; T_A = -55°C to +125°C

PIN NO.	SYMBOL		PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
READ CYCLE								
(1)	TAVAX	tRC	Read Cycle Time		200	-	ns	
(2)	TAVQV	tAA	Address Access Time		-	200	ns	
(3)	TEVQV	tCE1	Chip Enable Access Time		-	200	ns	(Note 5)
(4)	TSHQV	tCE2	Module Select Access Time		-	180	ns	
(5)	TGLQV	tOE	Output Enable Access Time		-	120	ns	
(6)	TEVQX	tLZ1	Chip Enable Output Enable Time		30	-	ns	(Notes 3, 5)
(7)	TSHQX	tLZ2	Module Select Output Enable Time		5	-	ns	(Note 3)
(8)	TGLQX	tOLZ	Output Enable Time		5	-	ns	(Note 3)
(9)	TAXQX	tOH	Address Output Hold Time		30	-	ns	(Note 3)
(10)	TEXQZ	tHZ1	Chip Disable Output Disable Time		0	85	ns	(Notes 3, 5)
(11)	TSLQZ	tHZ2	Module Select Output Disable Time		0	60	ns	(Note 3)
(12)	TGHQZ	tOZ	Output Disable Time		0	70	ns	(Note 3)
WRITE CYCLE								
(13)	TAVAX	tWC	Write Cycle Time		200	-	ns	
(14)	TWLWH	tWP	Write Pulse Width		100	-	ns	
(15)	TEVWH	tCW	Chip Enable to End of Write	$\overline{W}$ Controlled	145	-	ns	(Note 5)
(16)	TEVEX	tCW	Chip Enable to End of Write	E Controlled	120	-	ns	(Notes 3, 5)
(17)	TSHSL	tCW	Chip Enable to End of Write	S Controlled	120	-	ns	(Note 3)
(18)	TAVWL	tAS	Address Setup Time	$\overline{W}$ Controlled	50	-	ns	
(19)	TAVEV	tAS	Address Setup Time	E Controlled	20	-	ns	(Notes 3, 5)
(20)	TAVSH	tAS	Address Setup Time	S Controlled	40	-	ns	(Note 3)
(21)	TWHAX	tWR	Write Recovery Time	$\overline{W}$ Controlled	10	-	ns	
(22)	TEXAX	tWR	Write Recovery Time	E Controlled	10	-	ns	(Notes 3, 5)
(23)	TSLAX	tWR	Write Recovery Time	S Controlled	10	-	ns	(Note 3)
(24)	TDVWH	tDW	Data Setup Time	$\overline{W}$ Controlled	60	-	ns	
(25)	TDVEX	tDW	Data Setup Time	E Controlled	55	-	ns	(Note 3, 5)
(26)	TDVSL	tDW	Data Setup Time	S Controlled	55	-	ns	(Note 3)
(27)	TWHDX	tDH	Data Hold Time	$\overline{W}$ Controlled	35	-	ns	
(28)	TEXDX	tDH	Data Hold Time	E Controlled	35	-	ns	(Notes 3, 5)
(29)	TSLDX	tDH	Data Hold Time	S Controlled	35	-	ns	(Note 3)
(30)	TWLQZ	tWZ	Write Enable Output Disable Time		-	95	ns	(Note 3)
(31)	TWHQX	tOW	Write Disable Output Enable Time		10	-	ns	(Note 3)

NOTES:

1. All devices tested at worst case temperature and supply voltage limits.
2. Typical derating: 128K x 8: 5mA/MHz increase in ICCOP; 64K x 16: 10mA/MHz.
3. Guaranteed but not tested.
4. Input pulse levels: 0 to 3.0V; Input rise and fall times: 10ns max; Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent and CL = 100pF min including scope and jig - for CL greater than 100pF, access time is derated by 0.15ns/pF.
5. Enable valid (EV) in a parameter is determined the last transition that results in the combination of $\overline{E1}$ low, $\overline{E2}$ low and E3 high. Enable invalid (EX) in a parameter is determined by the first transition that results in any other combination than $\overline{E1}$ low, $\overline{E2}$ low and E3 high.

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Supply Voltage	+7.0V
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Operating Voltage Range	+4.5V to +5.5V
Operating Temperature Range	-55°C to +125°C

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ICCOP	Operating Supply Current 128K x 8 (Note 2) 64K x 16	-	10 20	mA mA	IO = 0, f = 1MHz, $\overline{E1}$ = $\overline{E2}$ = VIL, S = VCC E3 = VIH, VCC = 5.5V, VIN = VCC or GND
ICCDR	Data Retention Supply Current	-	750	μA	E3 = S = 0.3V, VCC = 2.0V
II	Input Leakage Current (Except S)	-1.0	+1.0	μA	VIN = VCC or GND, VCC = 5.5V
IIS	Module Select Input Current	-5	+5	μA	VIN = VCC or GND, VCC = 5.5V
IIOZ	I/O Leakage Current	-5	+5	μA	VIO = VCC or GND, VCC = 5.5V
VCCDR	Data Retention Supply Voltage	2.0	-	V	
VOL	Output Voltage Low	-	0.4	V	IOL = 4.0mA, VCC = 4.5V
VOH1	Output Voltage High	2.4	-	V	IOH = -1.0mA, VCC = 4.5V
VOH2	Output Voltage High (Note 3)	VCC-0.4	-	V	IOH = -100μA, VCC = 4.5V
VIL	Input Voltage Low	-0.3	0.8	V	
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(2)	TAVQV	tAA	Address Access Time		-	180	ns	
(3)	TEVQV	tCE1	Chip Enable Access Time		-	180	ns	(Note 5)
(4)	TSHQV	tCE2	Module Select Access Time		-	160	ns	
(5)	TGLQV	tOE	Output Enable Access Time		-	120	ns	
(6)	TEVQX	tLZ1	Chip Enable Output Enable Time		25	-	ns	(Notes 3, 5)
(7)	TSHQX	tLZ2	Module Select Output Enable Time		5	-	ns	(Note 3)
(8)	TGLQX	tOLZ	Output Enable Time		5	-	ns	(Note 3)
(9)	TAXQX	tOH	Address Output Hold Time		30	-	ns	(Note 3)
(10)	TEXQZ	tHZ1	Chip Disable Output Disable Time		0	75	ns	(Notes 3, 5)
(11)	TSLQZ	tHZ2	Module Select Output Disable Time		0	50	ns	(Note 3)
(12)	TGHQZ	tOZ	Output Disable Time		0	60	ns	(Note 3)
WRITE CYCLE								
(13)	TAVAX	tWC	Write Cycle Time		180	-	ns	
(14)	TWLWH	tWP	Write Pulse Width		100	-	ns	
(15)	TEVWH	tCW	Chip Enable to End of Write	$\overline{W}$ Controlled	140	-	ns	(Note 5)
(16)	TEVEX	tCW	Chip Enable to End of Write	E Controlled	120	-	ns	(Notes 3, 5)
(17)	TSHSL	tCW	Chip Enable to End of Write	S Controlled	120	-	ns	(Note 3)
(18)	TAVWL	tAS	Address Setup Time	$\overline{W}$ Controlled	40	-	ns	
(19)	TAVEV	tAS	Address Setup Time	E Controlled	0	-	ns	(Notes 3, 5)
(20)	TAVSH	tAS	Address Setup Time	S Controlled	40	-	ns	(Note 3)
(21)	TWHAX	tWR	Write Recovery Time	$\overline{W}$ Controlled	10	-	ns	
(22)	TEXAX	tWR	Write Recovery Time	E Controlled	10	-	ns	(Notes 3, 5)
(23)	TSLAX	tWR	Write Recovery Time	S Controlled	10	-	ns	(Note 3)
(24)	TDVWH	tDW	Data Setup Time	$\overline{W}$ Controlled	60	-	ns	
(25)	TDVEX	tDW	Data Setup Time	E Controlled	55	-	ns	(Note 3,5)
(26)	TDVSL	tDW	Data Setup Time	S Controlled	55	-	ns	(Note 3)
(27)	TWHDX	tDH	Data Hold Time	$\overline{W}$ Controlled	35	-	ns	
(28)	TEXDX	tDH	Data Hold Time	E Controlled	35	-	ns	(Notes 3, 5)
(29)	TSLDX	tDH	Data Hold Time	S Controlled	35	-	ns	(Note 3)
(30)	TWLQZ	tWZ	Write Enable Output Disable Time		-	95	ns	(Note 3)
(31)	TWHQX	tOW	Write Disable Output Enable Time		10	-	ns	(Note 3)

NOTES:

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2. Typical derating: 128K x 8: 5mA/MHz increase in ICCOP; 64K x 16: 10mA/MHz.
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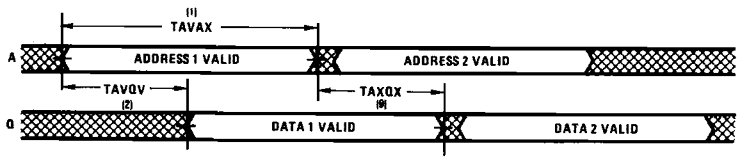
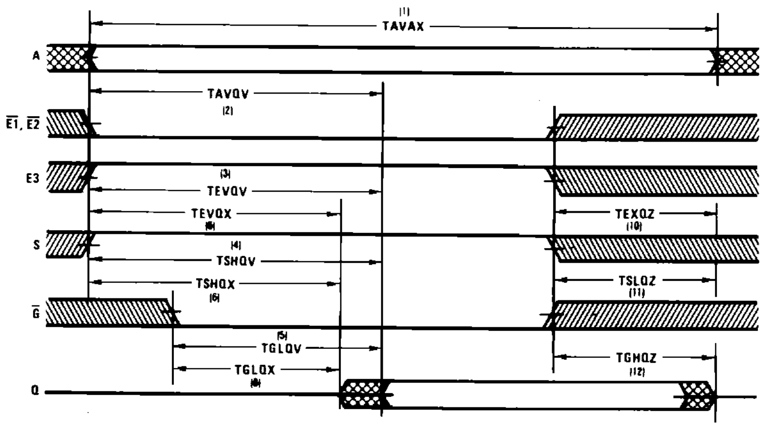
4. Input pulse levels: 0 to 3.0V; Input rise and fall times: 10ns max; Input and output timing reference level: 1.5V; Output load: 1TTL gate equivalent and CL = 100pF min including scope and jig - for CL greater than 100pF, access time is derated by 0.15ns/pF.
5. Enable valid (EV) in a parameter is determined the last transition that results in the combination of $\overline{E1}$ low, $\overline{E2}$ low and E3 high. Enable invalid (EX) in a parameter is determined by the first transition that results in any other combination than $\overline{E1}$ low, $\overline{E2}$ low and E3 high.

Timing Diagrams

READ CYCLE 1: ADDRESS CONTROLLED (NOTES 1, 2)



READ CYCLE 2: E, S, or $\overline{G}$ CONTROLLED (NOTE 1)

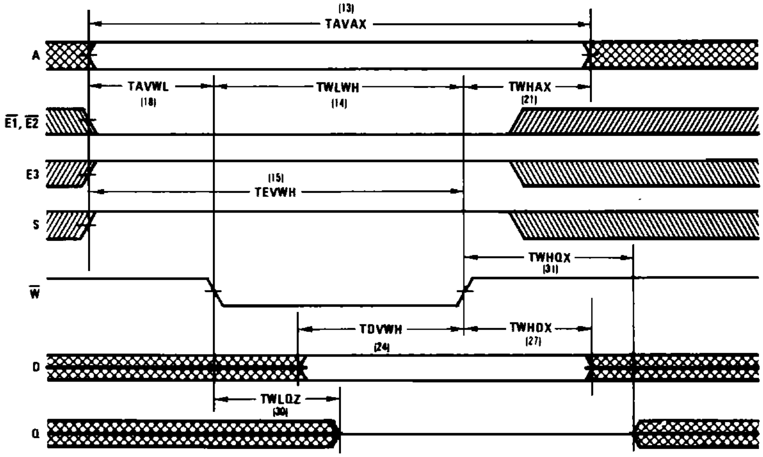


READ CYCLE NOTES: 1. In a read cycle, $\overline{W}$ is held high.

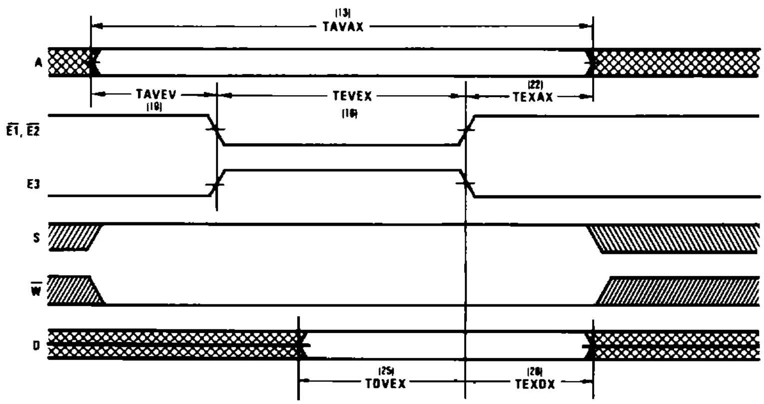
2. In read cycle 1, the module is kept continuously enabled: $\overline{E1}$, $\overline{E2}$ and $\overline{G}$ are held low; E3 and S are held high.

Timing Diagrams

WRITE CYCLE 1: $\overline{W}$ CONTROLLED (NOTE 1)

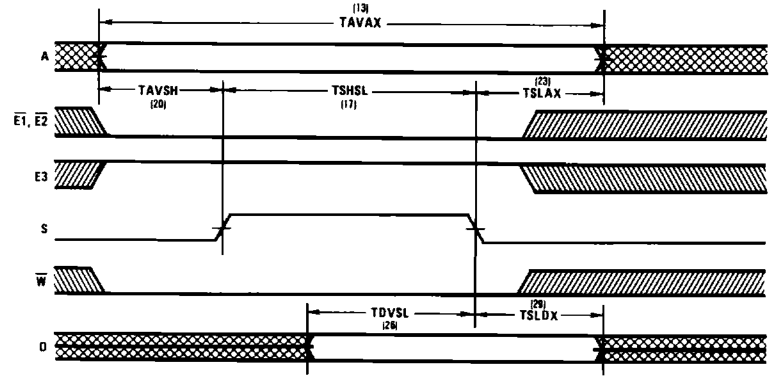


WRITE CYCLE 2: $\overline{E1}$, $\overline{E2}$, or E3 CONTROLLED (NOTE 2)



Timing Diagrams

WRITE CYCLE 3: S CONTROLLED (NOTE 3)



WRITE CYCLE NOTES:

1. In Write Cycle 1, the module is first enabled, and then data is strobed into the RAM with a pulse on $\overline{W}$. If $\overline{G}$ is held high for the entire cycle, the outputs will remain in the high impedance state. If $\overline{G}$ is held low, it may be necessary to lengthen the cycle to prevent bus contention. This would occur if TWLQZ and TDVWH overlapped.
2. In Write Cycle 2, Address (A) and Write Enable ($\overline{W}$) are first set up and then data is strobed into the RAM with a pulse on E.
3. In Write Cycle 3, Addresses (A), Write Enable ($\overline{W}$) and the Chip Enable inputs ($\overline{E1}$, $\overline{E2}$ and E3) are first set up and data is then strobed into the RAM with the Module Select (S) input.

TRUTH TABLE

INPUTS										MODE
S	$\overline{E1A}$	$\overline{E2A}$	E3A	$\overline{E1B}$	$\overline{E2B}$	E3B	$\overline{GA}$	$\overline{GB}$	$\overline{W}$	
GND	X	X	GND	X	X	GND	X	X	X	Standby (CMOS) Sides A and B
VIL	X	X	X	X	X	X	X	X	X	Standby (TTL) Sides A and B
X	VIH	X	X	X	X	X	X	X	X	Standby (TTL) Side A
X	X	VIH	X	X	X	X	X	X	X	Standby (TTL) Side A
X	X	X	VIL	X	X	X	X	X	X	Standby (TTL) Side A
X	X	X	X	VIH	X	X	X	X	X	Standby (TTL) Side B
X	X	X	X	X	VIH	X	X	X	X	Standby (TTL) Side B
X	X	X	X	X	X	VIL	X	X	X	Standby (TTL) Side B
VIH	VIL	VIL	VIH	X	X	X	VIH	X	VIH	Side A Enabled, Outputs High Impedance
VIH	X	X	X	VIL	VIL	VIH	X	VIH	VIH	Side B Enabled, Outputs High Impedance
VIH	VIL	VIL	VIH	X	X	X	VIL	X	VIH	Read Side A
VIH	X	X	X	VIL	VIL	VIH	X	VIL	VIH	Read Side B
VIH	VIL	VIL	VIH	X	X	X	X	X	VIL	Write Side A
VIH	X	X	X	VIL	VIL	VIH	X	X	VIL	Write Side B

NOTE:
Side A refers to the half of the module that connects to DQ0 through DQ7 and side B refers to the half of the module that connects to DQ8 through DQ15. When the module is configured as a 64K x 16 array, side A and side B may be enabled either simultaneously or separately. When the array is configured as a 128K x 8 array, side A and B should not be enabled simultaneously, as bus contention could result.

Organizational Guide

FOR 128K X 8 CONFIGURATION

CONNECT: PIN 16 (DQ0) to PIN 33 (DQ8)
PIN 17 (DQ1) to PIN 32 (DQ9)
PIN 18 (DQ2) to PIN 31 (DQ10)
PIN 19 (DQ3) to PIN 30 (DQ11)
PIN 20 (DQ4) to PIN 29 (DQ12)
PIN 21 (DQ5) to PIN 28 (DQ13)
PIN 22 (DQ6) to PIN 27 (DQ14)
PIN 23 (DQ7) to PIN 26 (DQ15)

FOR 64K X 16 CONFIGURATION

CONNECT: PIN 9 ($\overline{E1A}$) to PIN 40 ($\overline{E1B}$)
PIN 10 ($\overline{E2A}$) to PIN 39 ($\overline{E2B}$)
PIN 11 (E3A) to PIN 38 (E3B)
PIN 13 ($\overline{GA}$) to PIN 36 ($\overline{GB}$)

Concerns for Proper Operation of Chip Enables:

The transition between blocks of RAM requires a change in the chip enable being used. When operating in the 64K x 16 mode use the chip enables as if there were only three, E1 thru E3. In the 128K x 8 mode all chip enables must be treated separately. Transitions between chip enables must be treated with the same constraints that apply to any one chip enable. More than one (internal) chip enable low simultaneously, for devices whose outputs are tied together either internally or externally, is an illegal input condition and must be avoided.

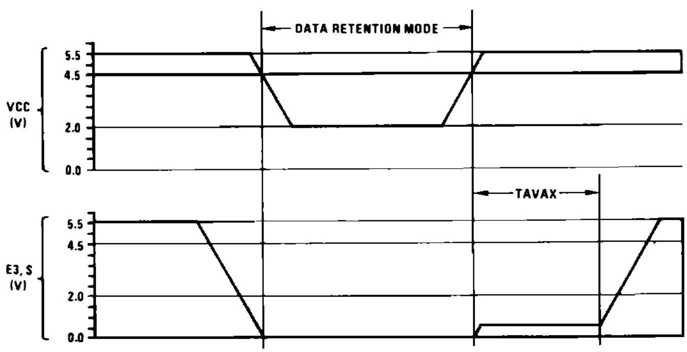
Printed Circuit Board Mounting:

The leadless chip carrier packages used in the HM-91M2 have conductive lids. These lids are electrically connected to GND.The system designer should be aware that the carriers on the bottom side could short conductors below if pressed completely down against the surface of the circuit board. The pins on the package are designed with a standoff feature to help prevent the leadless carriers from touching the circuit board surface.

Low Voltage Data Retention

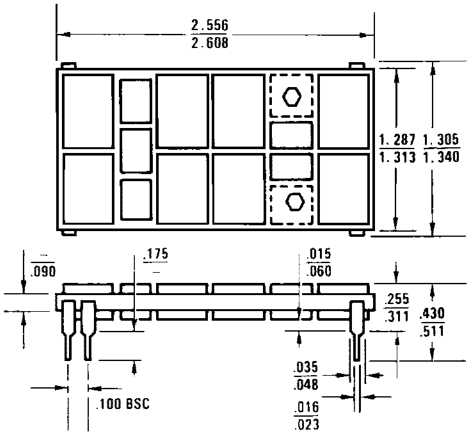
Harris CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. The module must be kept disabled during data retention. The Chip Enable (E3A and E3B) and module select (S) must be between -0.3V and +0.3V.
2. During power-up and power-down transitions. S must be held between -0.3V and 10% of VCC.
3. The RAM module can begin operation one TAVAX after VCC reaches the minimum operating voltage (4.5V).



Packaging

HM-91M2-8 48 PIN MODULE



NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.