TELTONE®

M-993 Region 1 MF Tone Generator

The Teltone® M-993 is a monolithic CMOS integrated circuit designed to generate multifrequency (MF) tone pairs for use in trunk signaling. The tones generated conform to CCITT R1 signal recommendations and to AT&T MF standards. The M-993 permits design engineers to implement a highly accurate MF sender with a minimum of space, power, and added components. The accuracy of the tone frequencies is assured through use of an easily obtained 3.58-MHz color burst crystal or an external 3.58-MHz clock source.

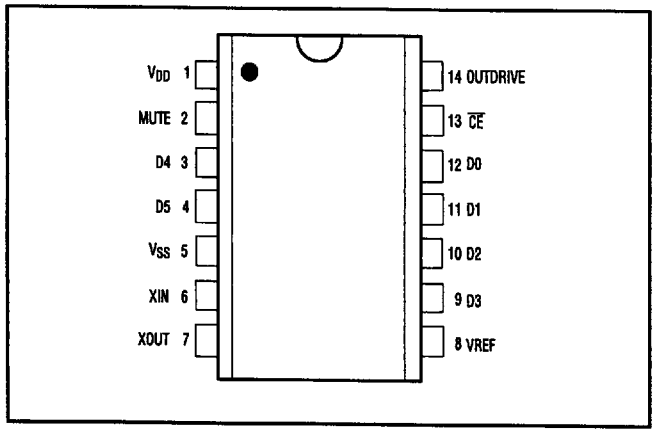

Figure 1 Pin Diagram

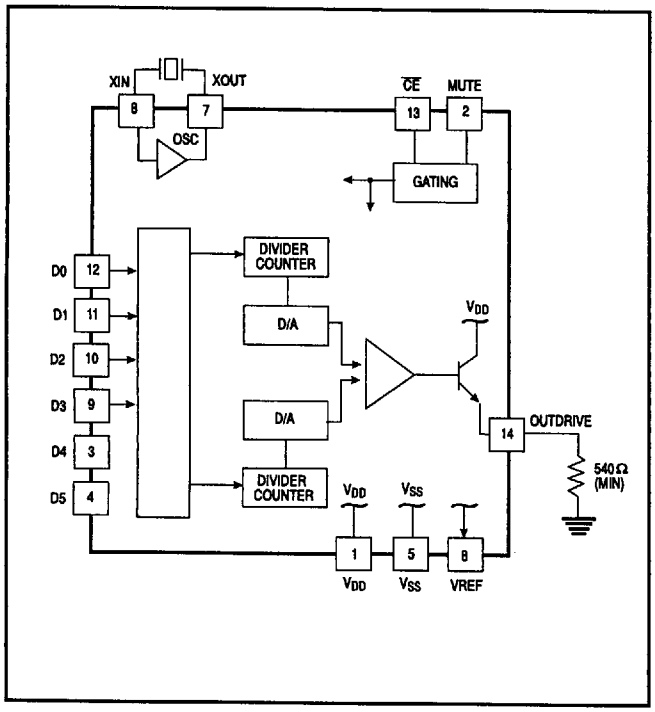

Figure 2 Block Diagram

Features

- Generates standard CCITT R1 MF tones
- Digital input control
- Linear (analog) output
- Power output capable of driving standard line
- 14-pin DIP
- Single 5-Volt supply
- Inexpensive 3.58-MHz time base

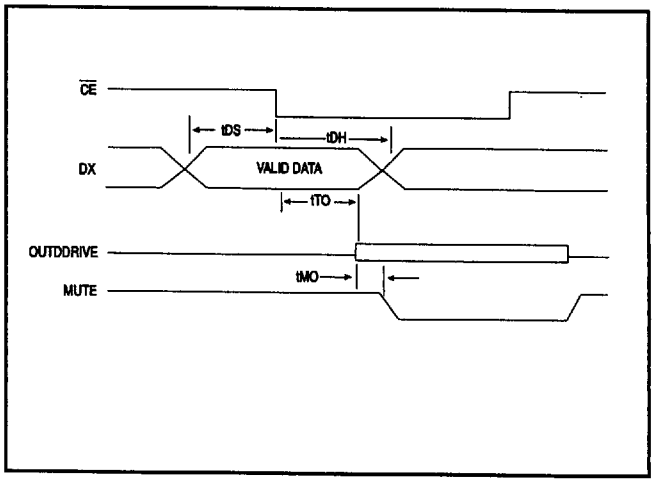

Figure 3 Timing Diagram

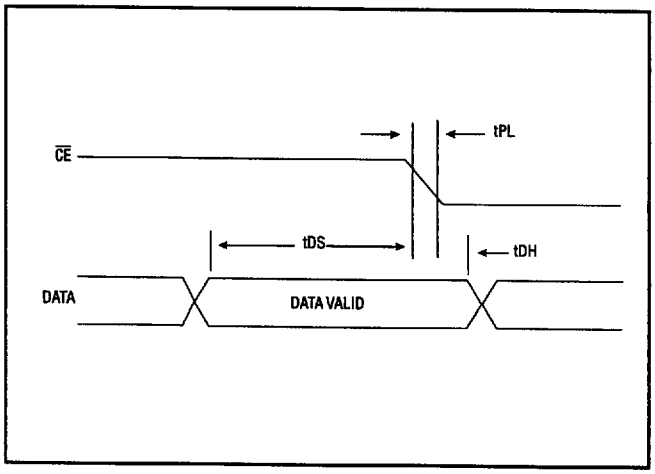

Figure 4 Expanded Timing Diagram

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40-406-00005, Rev. B, June 1997

Applications

- Telephone systems
- Test equipment

R1 MF Tone Generation

MF tones are used to signal between telephone offices and between telephone company central switching equipment and customer equipment.

Table 1 Pin Functions

PIN	FUNCTION
$\overline{CE}$	Latches data and enables output (active low input).
D0 - D5	Data input pins. (See Table 2.)
MUTE	Output indicates that a signal is being generated at OUTDRIVE.
OUTDRIVE	Linear buffered tone output.
V_{DD}	Most positive power supply input pin.
VREF	Internally generated mid-power supply voltage (output).
V_{SS}	Most negative power supply input pin.
XIN	Crystal oscillator or digital clock input.
XOUT	Crystal oscillator output.

The M-993 is a highly linear tone generator that produces the tone pairs required for R1 MF signaling. Duration and frequency selection are digitally controlled (see Table 2 for data settings for a particular tone pair output).

A typical control sequence for the M-993 is: (1) set data lines to desired frequency selection, (2) wait for data lines to settle,

Table 2 Data/Tone Selection

D3	D2	D1	D0	FREQUENCY (Hz)		USE
				1	2	
0	0	0	0	1100	1700	Key Pulse (KP)
0	0	0	1	700	900	Digit 1
0	0	1	0	700	1100	Digit 2
0	0	1	1	900	1100	Digit 3
0	1	0	0	700	1300	Digit 4
0	1	0	1	900	1300	Digit 5
0	1	1	0	1100	1300	Digit 6
0	1	1	1	700	1500	Digit 7
1	0	0	0	900	1500	Digit 8
1	0	0	1	1100	1500	Digit 9
1	0	1	0	1300	1500	Digit 0
1	0	1	1	1500	1700	ST
1	1	0	0	900	1700	ST1
1	1	0	1	1300	1700	ST2
1	1	1	0	700	1700	ST3

Table 3 Absolute Maximum Ratings (Note 1)

Storage Temperature	-55 to 125° C
Operating Ambient Temperature	-25 to 70 ° C
V_{DD}	7.0V
Any Input Voltage	V_{SS} - 0.6 to V_{DD} + 0.6V
Note 1: Exceeding these ratings may permanently damage the M-993.	

(3) drive the chip enable ($\overline{CE}$) low, (4) maintain $\overline{CE}$ low for desired tone duration (Note: data lines may be changed after data hold time), and (5) return $\overline{CE}$ to a logic high.

In a bus-oriented system, noise on the data lines may propagate through the device and appear at the output. To safeguard against this, use an external latch to clock the data into the device. In addition, it is good practice to bypass the V_{ref} pin to ground with a small capacitor (~0.01µF) to reduce power supply noise. The designer should be aware of device timing requirements and design accordingly. Beware of hardwiring the data input pins for dedicated tone generation. An RC network like that shown in Figure 5 should be used to momentarily reset the device immediately following a power-up to ensure reliable operation.

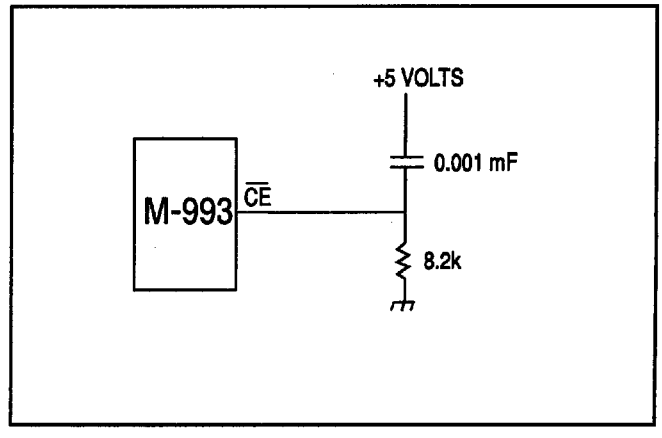

Figure 5 Power-On Reset Circuit

Table 4 Specification

PARAMETER		MIN	TYP	MAX	UNITS	NOTES
Power Supply and Reference	V_{DD}				V	1
	Current Drain, IDD	—			mA	8
	VREF PIN:					
	Deviation from (V_{DD} + V_{SS})/2	—2	—	+2	%	
	Internal Resistance from VREF to V_{DD}, V_{SS}	3.25	—	6.75	Kohms	
Oscillator	Frequency Deviation	-0.01	—	+0.01	%	7
	External CLock: (XOUT open)					
	VIL	0	—	0.2	V	
	VIH	V_{DD}- 0.2	—	V_{DD}	V	
	Duty Cycle	40	—	60	%	
	XIN, XOUT Loading:					
	Capacitance	—	—	10	pF	10
	Resistance	20	—	—	Mohms	
Tone Output	Frequency Deviation	-1.5	—			
	Level	110	—			2
	Distorting Components	-35	—			3
	Idle	—	—	-60	dBm	4
	OUTDRIVE Envelope Rise Time	—	—	4	ms	5
Control	DX, $\overline{CE}$ Pins:					
	VIL	—	—	0.5	V	6
	VIH	2.5	—	—	V	
	Mute Pins:					
	VOL (ISINK = -100 µA)	—	—	1.5	V	
	VOH (ISOURCE = 100 µ A)	V_{DD}- 1.5	—	—	V	
Timing	Data Setup (tDS)	200	—	—	ns	11
	Data Hold (tDH)	10	—	—	ns	
	Chip Enable Fall (tPL)	—	—	90	ns	
	Tone On Delay (tTO)	—	—	5	ms	
	Tone Off Delay (tTD)	—	—	5	ms	
	Mute Delay from Outdrive (tMO)	—	—	200	ns	

Unless otherwise noted, VDD - VSS = 5 VDC, Ta - 25° C

Notes: (unless otherwise specified)

1. All DC voltages are referenced to V_{SS}.
2. Vrms per tone, 540 ohm load.
3. Anyone frequency relative to the lowest level output tone (f<4000 Hz).
4. 0 dBm = 0.775 Vrms.
5. To 90% maximum amplitude.
6. For all supply voltages in the operating range.
7. At XOUT pin as compared to 3.579545 MHz.
8. OUTDRIVE with load >5 kohm/OUTDRIVE with 540 ohm load.
9. Resistance at VREF to V_{DD} or V_{SS} > 1Mohm.
10. Crystal oscilaltor active.
11. Measured 90% to 10%.

Ordering Information

M-993	14-pin plastic DIP
M-993-C	14-pin CERDIP

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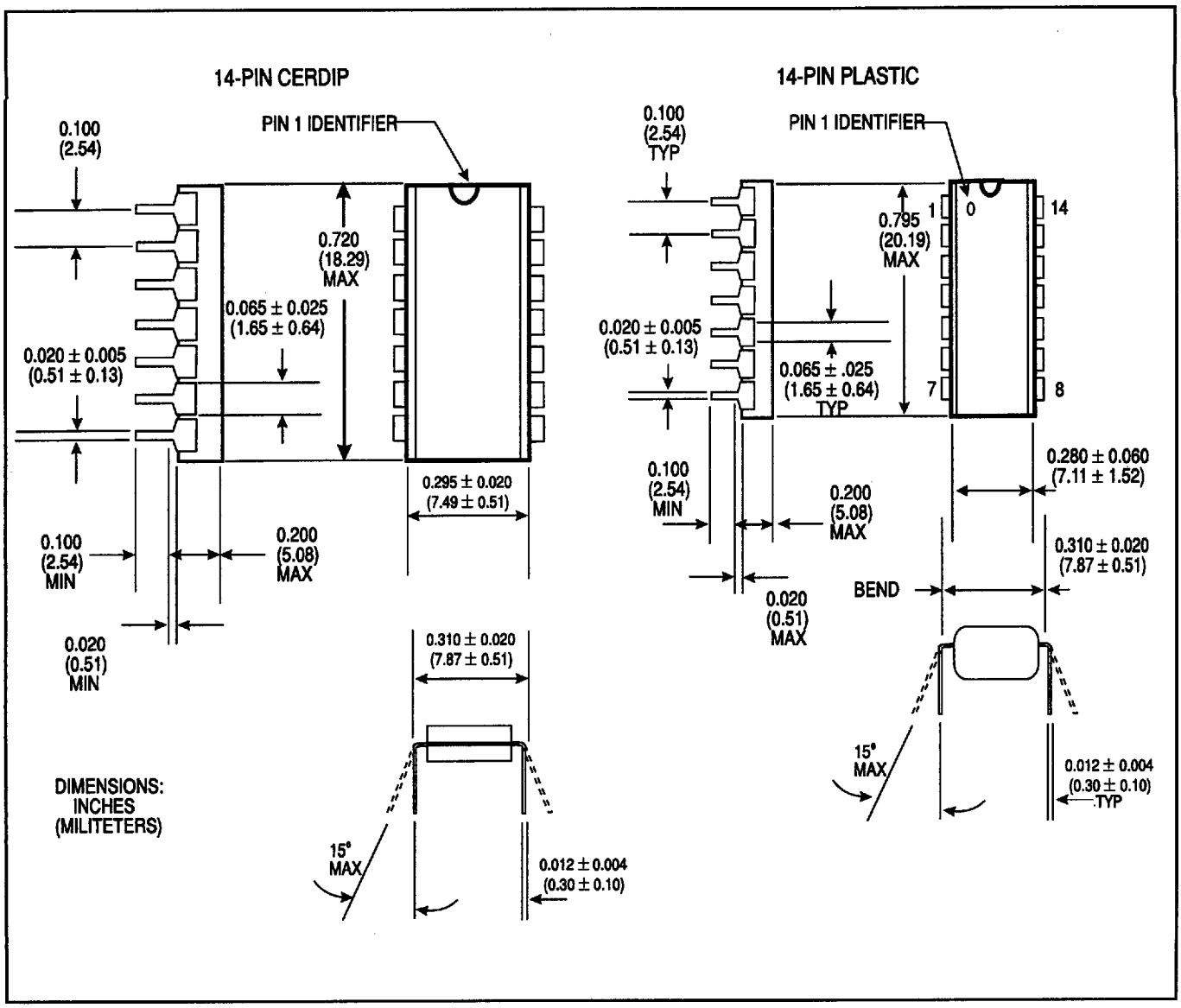

Figure 6 Package Dimensions

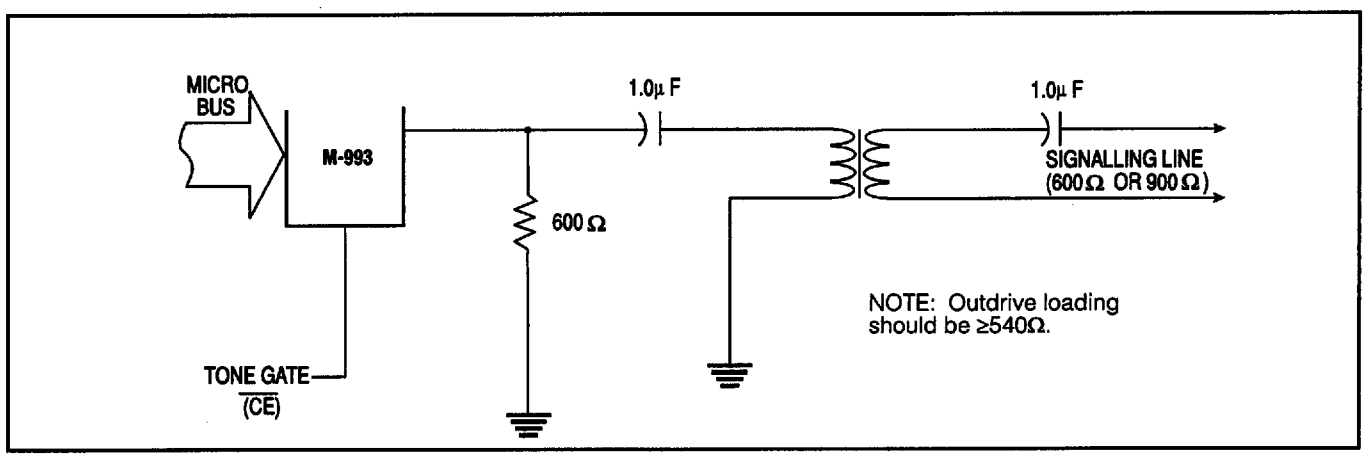

Figure 7 Typical Application