MTC-20278 ILTQ
MTC-20279 ILTT

Quad Integrated LT (ILT)
ISDN Standard Products

Advance Information

Key Features

- **Quad ISDN LT 'U' interface functions in a single monolithic integrated circuit**
- **Pin compatible 2B1Q and 4B3T line code versions**
  - **MTC-20278 ILTQ for 2B1Q**
  - **MTC-20279 ILTT for 4B3T**
- **Full compliance with the applicable ETSI, ANSI, ITU and FTZ requirements**
- **Digital, 5V compatible interface bus using industry-standard GCI**
- **Minimal external components**
- **3.3V operating voltage for low power operation**
- **Advanced 0.5µ CMOS mixed analog/digital process technology**
- **64 pin Plastic Quad Flat Pack package**

General Description

The MTC-20278/9 chip contains all the functions necessary to make 4 'U' interfaces in an ISDN Line Termination card. It comprises 4, fully integrated echo-canceling 'U' interfaces, conformant to the 'Uk0' interface point, plus the necessary support and test functions. The general block diagram is shown in Figure 1. Two versions of the device are available - the MTC-20278 offering the 2B1Q line code, and the MTC-20279 which has 4B3T line coding. Both devices are pin compatible, and are fully compliant with the relevant parts of ANSI, ETSI and FTZ and ITU requirements for ISDN connection.

The MTC-20278/9 devices offer a user transport rate of 144kbit/s full duplex (2B + D) per channel, as well as fully automatic control of activate/deactivate protocols and line supply, and full support of the maintenance channel.

The digital interface on the 'exchange' side uses the industry-standard GCI interface in 2 Mbit burst mode. This mode allows for 8 channels to be multiplexed onto the same interface. The MTC-20278/9 can be set to respond to either the first 4 or the last 4 timeslots in the GCI frame. This allows two devices, totalling 8 ISDN lines, to be multiplexed onto the same GCI interface.

The MTC-20278/9 takes all timing information from the GCI clocks, and so does not require a separate clock oscillator.

Figure 2 shows the typical circuit configuration of the MTC-20278/9.

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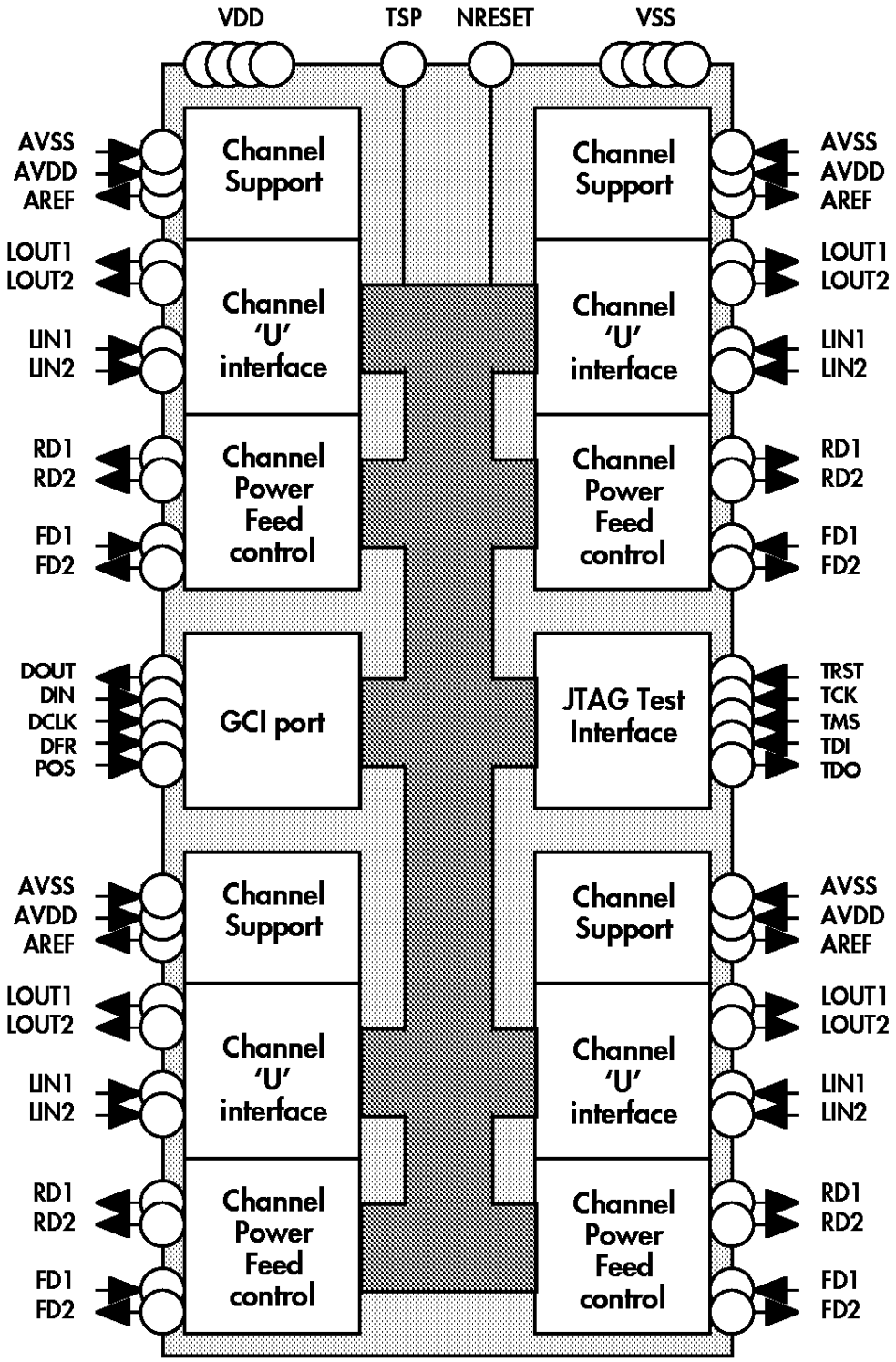

Fig. 1: MTC-20278/9 ILT General block diagram

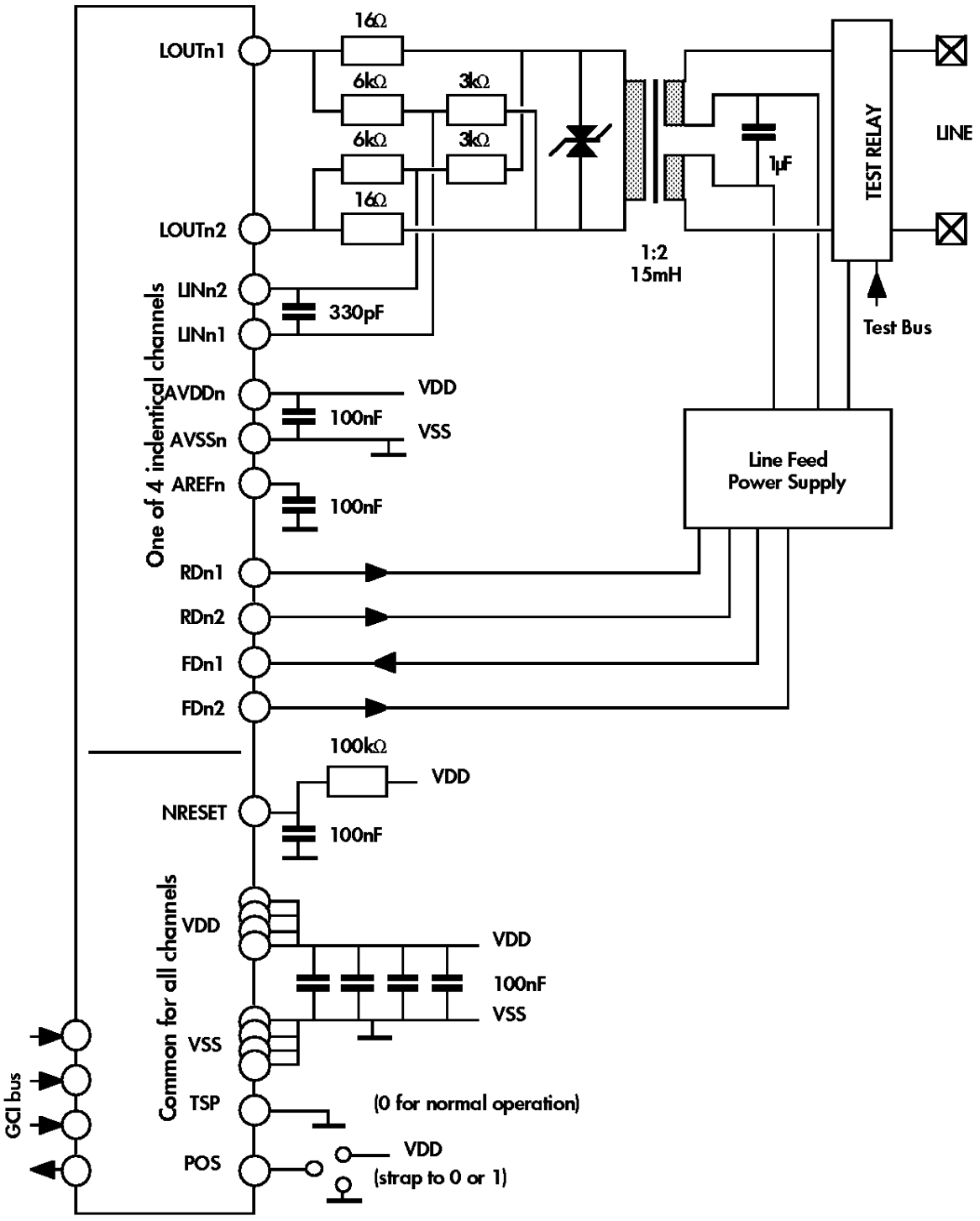

Fig. 2: MTC-20278/9 ILT - typical component configuration

GCI bus ILT channel allocation

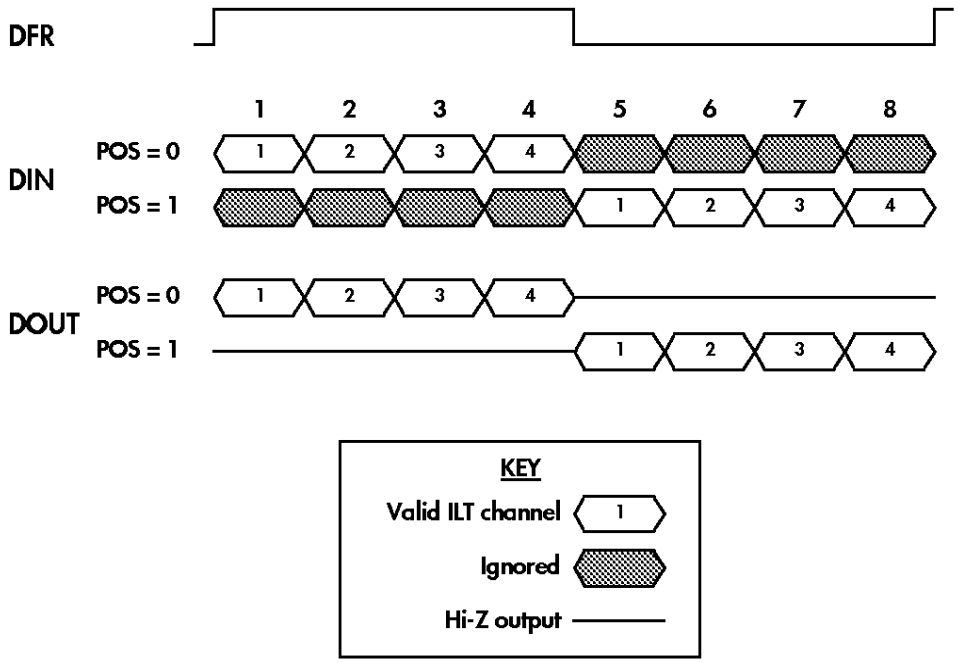

Fig. 3: GCI bus multiplexing timing diagram

Pin Description

Nr.	Function	Name	Dir.	Description
64, 16, 32, 48	U	LOUTn1	O	U interface analog outputs. The connections LOUTn1 and LOUTn2 interface the U driver outputs, via termination resistors and the line coupling transformer, to the UK0 reference point.
1, 17, 33, 49		LOUTn2	O	See LOUTn1
3, 19, 35, 51	Int.	LINn1	I	LINn1 and LINn2 are the U interface analog inputs to the INT from the analog 'hybrid'
4, 20, 36, 52		LINn2	I	See LINn1
2, 18, 34, 50		AREFn	O	Analog ground (1.65V). Used as reference voltage for analog functions

63, 15, 31, 47		AVDDn	P	VDD for analog U interface functions
62, 14, 30, 46		AVSSn	P	VSS (0V ground) for U interface analog functions
61, 13, 37, 53	Pow. Feed Cntrl.	RDn1	O	Relay drivers
5, 12, 38, 45		RDn2	O	Relay drivers
6, 11, 39, 44		FDn1	I	Power Feed control input
7, 10, 40, 43		FDn2	O	Power Feed control output
23 27 25 28 29	GCI Int.	DOUT DIN DCLK DFR POS	O I O O I	GCI interface Data Out GCI interface Data In GCI interface Data Clock GCI interface Frame Clock Select GCI burst group: 0 = first 4, 1 = last 4
60 59 58 54 56	JTAG INT.	TRST TCK TMS TDI TDO	I I I I O	TAP controller reset, active low TAP controller clock, maximum 10 MHz TAP controller mode selection TAP controller input TAP controller output
21 22		NRESET TSP	I I	Hardware reset, active low. Schmitt trigger input for connection to external RC or logic device. Reset pulse min. 10ms. Test Single Pulses. ILT transmits alternate positive and negative pulses to act as test and search-tone on the line.
8 24 42 57		VDD VDD VDD VDD	P P P P	Positive supply for digital functions
9 26 41 55		VSS VSS VSS VSS	P P P P	0V ground for digital functions

MTC-20278 ILTQ
MTC-20279 ILTT

Key circuit characteristics (preliminary values)

'U' interface characteristics - MTC-20278 (2B1Q)		
BER / loop range	$<10^{-7}$	Exceeds ANSI and ETSI requirements.
TSP pulses	666	Hz
'U' interface characteristics - MTC-20279 (4B3T)		
BER / loop range	<10-7	Exceeds FTZ and ETSI requirements.
TSP pulses	1000	Hz
GCI interface characteristics		
Nominal bit-rate, DIN and DOUT	2048	kbit/s
Nominal frequency of clock (CL)	4096	kHz
Peak-peak output jitter of clock (CL)	≤ 166	ns, NT modes
Nominal frequency of frame clock (FR)	8	kHz
Duty-cycle of FR (output)	40 to 60	%
DC characteristics, logic interfaces (all pins, except where noted)		
VIH (input high-level voltage)	VDD * 0.7	V min
VIL (input low level voltage)	VDD * 0.3	V max
VOH1 (high level output voltage)	VDD * 0.9	V min at IOH1 = 0.4mA, except pin DOUT
VOL1 (low level output voltage)	VDD * 0.1	V max at IOL1 = 0.4mA, except pin DOUT
CIN (input capacitance)	10	pF max
COUT (capacitive load on outputs)	25	pF max
Iin (input leakage current)	1	µA
Test modes		
TBD		

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