DOLBY* B & C TYPE NOISE REDUCTION CIRCUITS

GENERAL DESCRIPTION

The TEA0651/TEA0652 and TEA0654 provide both, Dolby B and Dolby C type audio Noise Reduction (NR). The TEA0651/TEA0652 are NR signal processing ICs in 18-lead DIL packages. They can be used either as a stereo Dolby B NR circuit or as one channel of a switchable Dolby B & C NR circuit. In addition they provide NR ON/OFF switching.
The TEA0654 is a switching IC in a 24-lead DIL package. It contains the switching, the pre-amplifiers for playback and recording functions and a multiplex filter buffer amplifier.
The circuits are pin compatible to Signetics NE651, NE652 and NE654 respectively.

Features

TEA0651/TEA0652

- Dual purpose IC for Dolby B & C NR systems:
  switchable B/C type NR systems, B-type NR systems (stereo without preamplifiers), automotive entertainment systems (playback only) and portable applications
- Dual version for better matching between HIGH and LOW level stages in C-type NR or better channel matching for stereo B-type NR applications
- Full-wave rectifier
- No capacitive divider for side-chain filter needed
- Electronic switching for NR ON/OFF, B and C-type NR
- Dolby level 0 dB = −6 dBm (387,5 mV) offers line output level option of 0 dBm (775 mV)

TEA0654

- Electronic switching for playback/record
- Electronic switching for NR ON/OFF and B/C type NR
- No internal/external matching required for filter networks:
  only one network for spectral skewing and deskewing necessary; only one network for anti-saturation necessary
- Excellent matching between record and playback
- Line output (monitor) level externally set by resistor ratio independent of internal Dolby level
- Playback and record preamplifier and multiplex filter buffer amplifier included

PACKAGE OUTLINES

TEA0651/TEA0652: 18-lead DIL; plastic (SOT102H).
TEA0654: 24-lead DIL; plastic (SOT101A).

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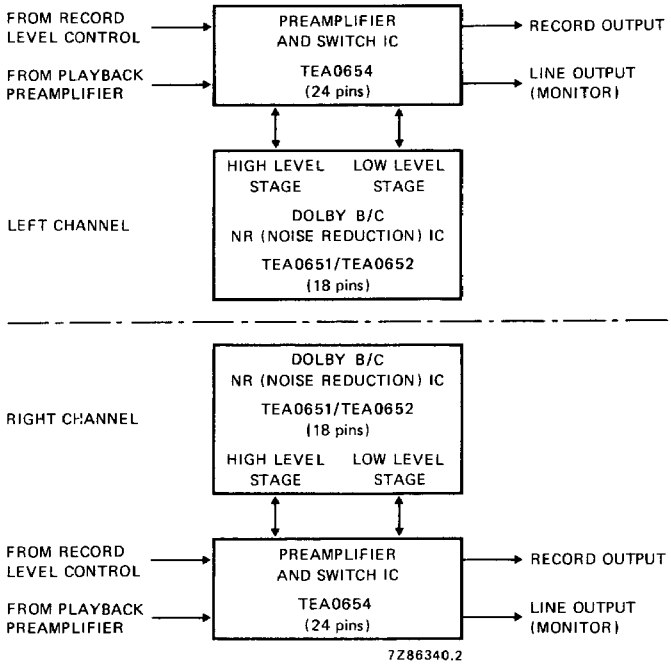
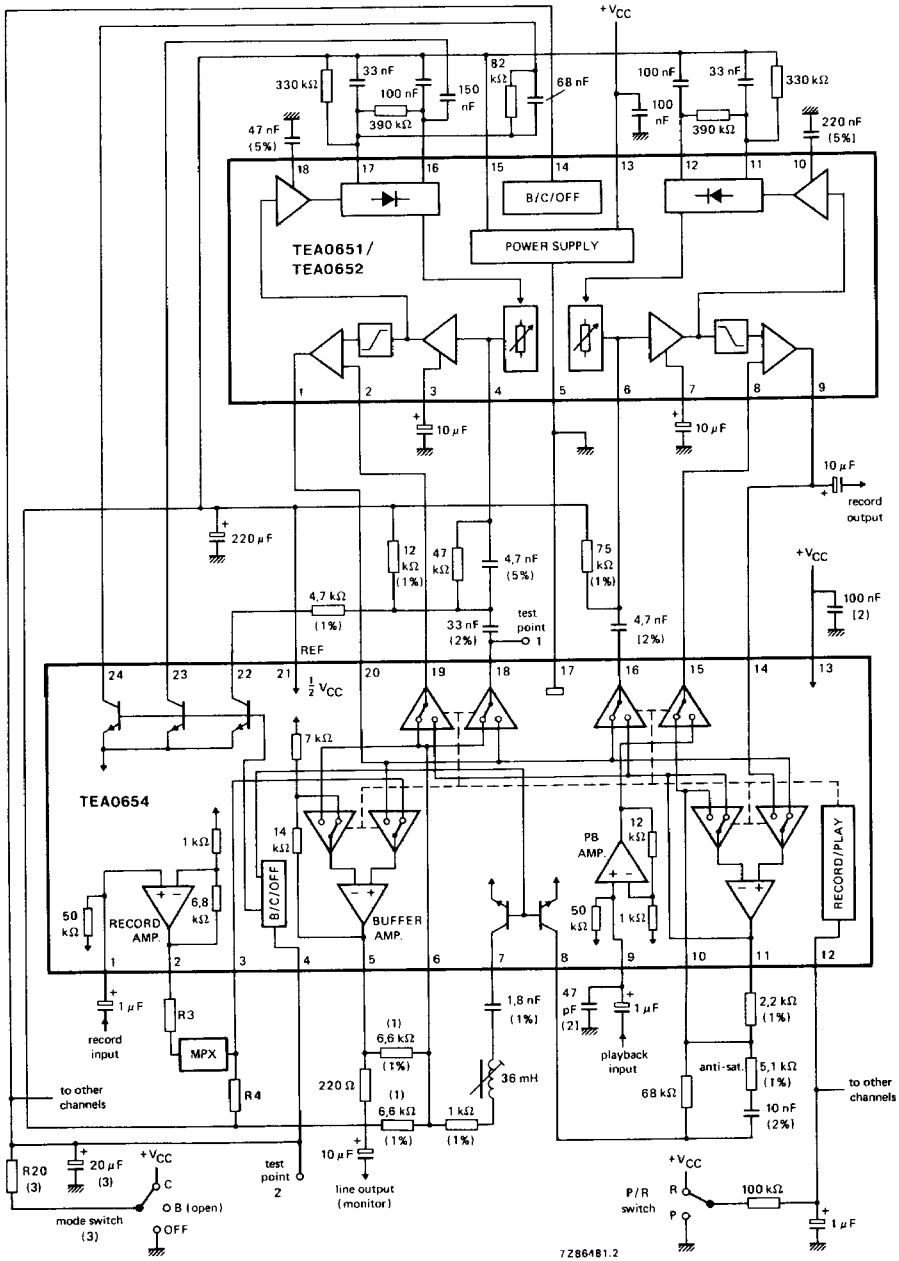


Fig. 1 System block diagram.

Switching levels; see Fig. 2.

pin condition (test point 2)	functions switched for TEA0654 (pin 4)	functions switched for TEA0651/TEA0652 (pin 14)
$+V_{CC}$	Dolby-C, open collector transistors at pins 7 and 8 switched on, at pins 22, 23, 24 switched off	Dolby-C
$\frac{1}{2}V_{CC}$	not applicable	stereo Dolby B, both channels active (Figs 15 and 16)
open (internally pulled to $\frac{1}{4}V_{CC}$)	Dolby-B, open collector transistors at pins 7 and 8 switched off, at pins 22, 23, 24 switched on	Dolby-B, low level stage side chain muted
ground	as pin condition 'open'	NR-OFF both side chains muted



(1) Line output and record input programming resistors.
(2) Optional capacitors.
(3) Time constant for mode switch is optional, R20 is equal to 6,8 kΩ divided by number of switched channels.

Fig. 2 Dolby B/C NR system; switches shown in record position.

SYSTEM RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{CC}	max.	23	V
Storage temperature range	T_{stg}	−55 to + 150		°C
Operating ambient temperature range	T_{amb}	−30 to + 85		°C
Total power dissipation				
TEA0651/TEA0652	P_{tot}	max.	600	mW
TEA0654	P_{tot}	max.	800	mW

SYSTEM CHARACTERISTICS

V_{CC} = 14 V; f = 20 Hz to 20 kHz; T_{amb} = 25 °C; all levels with reference to 387,5 mV = 0 dB = −6 dBm at test point 1 in Fig. 2; record mode; unless otherwise specified; for graphs see Figs 10 to 16.

parameter	conditions			min.	typ.	max.	unit
	mode	f(kHz)					
Supply voltage range	C	–	V_{CC}; note 1	8	14	20	V
Input sensitivity	C	–	record mode	–	50	–	mV
			playback mode note 2	–	30	–	mV
Signal handling at record output note 3	C	–	V_{CC} = 8 V line output is −6 dBm	12	–	–	dB
	C	1	V_{CC} = 14 V THD - 1% line output is −6 dBm	–	18	–	dB
	–	1	V_{CC} = 14 V line output is 0 dB,	12	–	–	dB
Signal-to-noise ratio (S/N)	C	–	R_S = 10 kΩ CCIR/ARM weighted	60	66	–	dB
Switching thresholds note 4	OFF	–	voltage at test point 2	–	–	0,065 x V_{CC}	V
	B	–	voltage at test point 2; note 5	0,2 x V_{CC}	0,25 x V_{CC}	0,3 x V_{CC}	V
	C	–	voltage at test point 2	0,85 x V_{CC}	–	–	V

Notes to system characteristics

1. Operation with minimum of 12 dB headroom; system remains functional to 6 V.
2. Attenuation between pins 2 and 3 of TEA0654 is 4 dB;
3. System headroom is determined by programmable monitor output level (pin 5 of TEA0654).
4. For a typical application see Fig. 10. Worst case considerations for the V_{CC} range from 8 V to 20 V limit the optional external resistor to maximum 6,8 kΩ, divided by number of switched channels.
5. In the open position (B) of the mode switch pin 14 of TEA0651/TEA0652 is pulled to typical 0,25 x V_{CC} by pin 4 of TEA0654.

SYSTEM GRAPHS

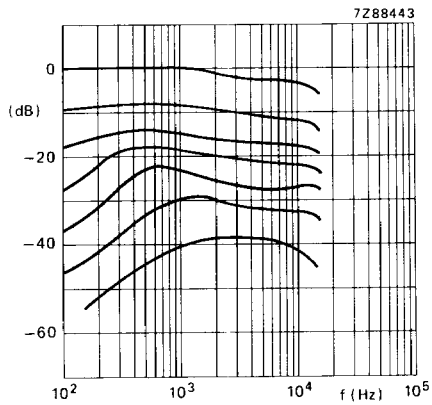


Fig. 3 Encoder frequency response for C-mode.

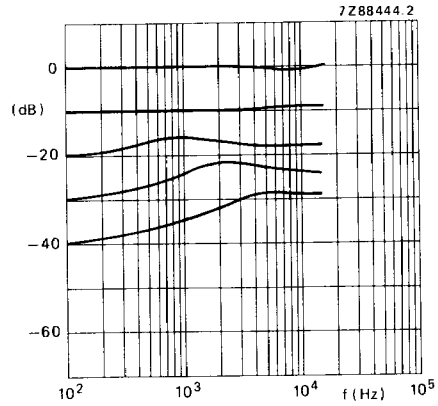


Fig. 4 Encoder frequency response for B-mode.

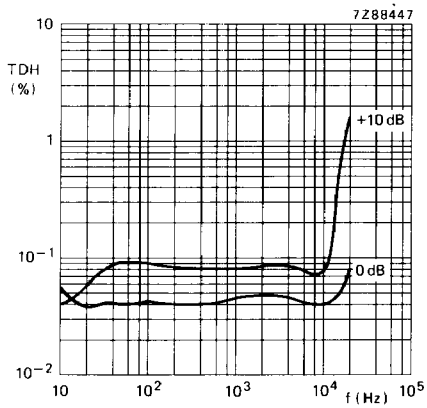


Fig. 5 Total harmonic distortion as a function of frequency for B-mode.

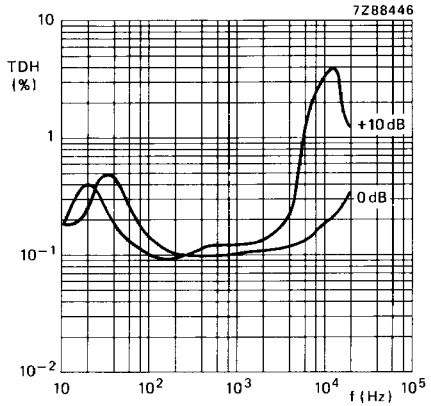


Fig. 6 Total harmonic distortion as a function of frequency for C-mode.

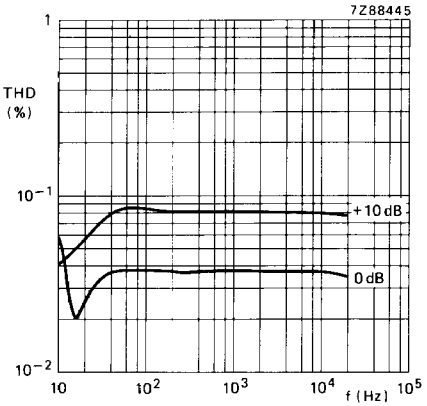


Fig. 7 Total harmonic distortion as a function of frequency for NR OFF-mode.

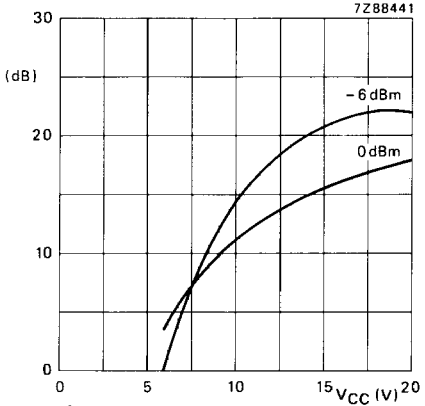


Fig. 8 Headroom at record output and line output (pins 14 and 5 of TEA0654); THD = 1%; f = 1 kHz, at line output levels 0 and −6 dB.

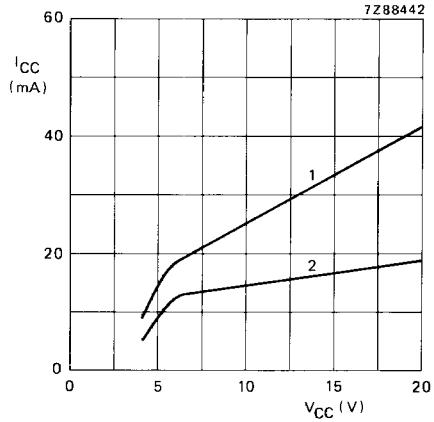


Fig. 9 Supply current as a function of supply voltage. 1: TEA0651/TEA0652 and TEA0654; 2: TEA0651/TEA0652 only.

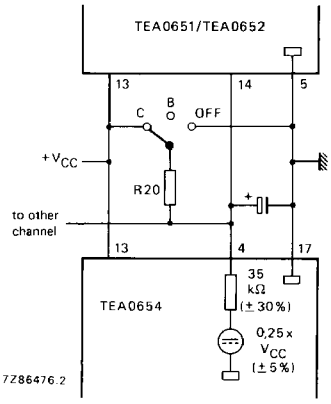


Fig. 10 Optional external time constant for mode switch.

TEA0651/TEA0652: DOLBY B/C TYPE NOISE REDUCTION PROCESSING CIRCUITS

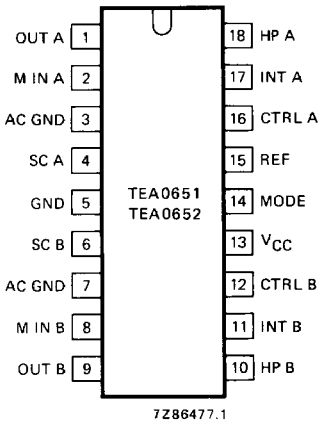


Fig. 11 Pinning diagram of TEA0651/TEA0652.

PINNING

1	OUT A	output channel A
2	M IN A	main chain input channel A
3	AC GND	a.c. ground channel A
4	SC A	side chain channel A
5	GND	ground
6	SC B	side chain channel B
7	AC GND	a.c. ground channel B
8	M IN B	main chain input channel B
9	OUT B	output channel B
10	HP B	high-pass filter channel B
11	INT B	integrating filter channel B
12	CTRL B	control voltage channel B
13	V_{CC}	positive supply voltage
14	MODE	mode B/C/NR OFF switch input
15	REF	reference voltage
16	CTRL A	control voltage channel A
17	INT A	integration filter channel A
18	HP A	high-pass filter channel A

Note

For Dolby-C type application channel A is the HIGH level stage and channel B is the LOW level stage.

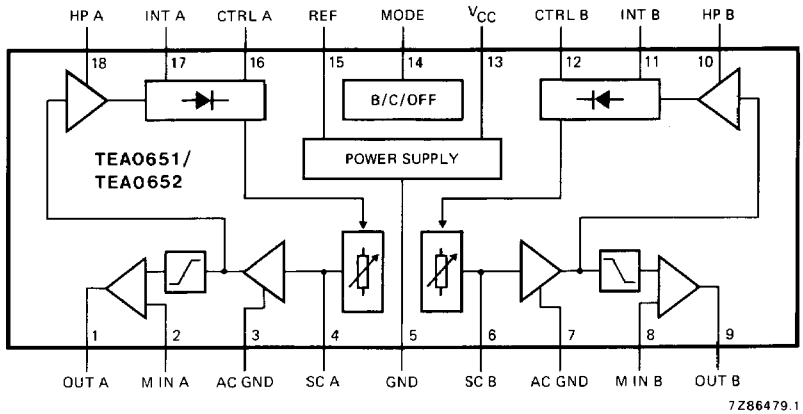


Fig. 12 Block diagram of TEA0651 and TEA0652.

CHARACTERISTICS FOR TEA0651/TEA0652

V_{CC} = 14 V; f = 20 Hz to 20 kHz; T_{amb} = 25 °C; all levels with reference to 387,5 mV = 0 dB = −6 dBm at test point 1; test circuit Fig. 13; record mode; unless otherwise specified.

parameter	conditions			min.	typ.	max.	unit
	mode	f(kHz)					
Supply voltage range	B	–	V_{CC}	8	14	20	V
Supply current I_{CC}	OFF	–	no input signal	–	17	25	mA
Power supply ripple rejection ratio	B	1	test circuit Fig. 14	–	60	–	dB
Voltage gain	OFF	1	note 1	−0,5	–	+ 0,5	dB
Signal handling at record output (note 4)	B	1	V_{CC} = 14 V THD = 1%	–	20	–	dB
		1	V_{CC} = 8 V THD = 1%	12	14	–	dB
		1	V_{CC} = 6 V THD = 1%	–	11	–	dB
Signal-to-noise ratio (S/N)	B	–	R_S = 10 kΩ, internal CCIR/ARM weighted	–	90	–	dB
Switching thresholds	OFF	–	voltage at pin 14	–	–	0,065 x V_{CC}	V
	B	–	voltage at pin 14	0,2 x V_{CC}	0,25 x V_{CC}	0,3 x V_{CC}	V
	C	–	voltage at pin 14	0,85 x V_{CC}	–	–	V
Switching threshold for stereo B appl.	B	–	voltage at pin 14	–	0,5 x V_{CC}	–	V
Channel matching	OFF	1	TPL = 0 dB notes 2, 3	−0,5	–	+ 0,5	dB
Channel separation	B	1	TPL = + 10 dB notes 2, 3	60	70	–	dB

Notes

1. Voltage gain is 20 log $\frac{\text{voltage at pin 1 (9)}}{\text{voltage at pin 2 (8)}}$.
2. TPL is Test Point Level.
3. Test circuit Fig. 15, reference level at channel A and channel B test point.
4. Operation with minimum of 12 dB headroom; system remains functional to 6 V.

CHARACTERISTICS TEA0651 ONLY

parameter	conditions			min.	typ.	max.	unit
	mode	f(kHz)					
Offset voltage	C	–	$\lvert V_{9\text{-}15} \rvert$	–	3	6	mV
Signal-to-noise ratio (S/N)	C	–	R_S = 10 kΩ (internal) CCIR/ARM weighted; pin 9	77	80	–	dB
Total harmonic distortion (THD)	B	10	TPL = 0 dB	–	–	0,1	%
			TPL = + 10 dB	–	0,05	0,1	%
Total harmonic distortion (THD)	C	10	TPL = 0 dB	–	–	0,1	%
		1	TPL = + 10 dB	–	0,15	0,5	%
B-mode frequency response	B	1	TPL = −20 dB	−17,3	−15,8	−14,3	dB
		2	TPL = −25 dB	−19,5	−18,0	−16,5	dB
		5	TPL = −40 dB	−30,2	−29,7	−28,2	dB
		10	TPL = −30 dB	−25,0	−23,5	−22,0	dB
C-mode frequency response	C	0,2	TPL = −40 dB	−32,9	−31,9	−30,9	dB
		0,5	TPL = −20 dB	−14,2	−13,7	−13,2	dB
		0,5	TPL = −30 dB	−18,7	−18,2	−17,7	dB
		1	TPL = −20 dB	−14,6	−14,1	−13,6	dB
		1	TPL = −30 dB	−19,1	−18,6	−18,1	dB
		1	TPL = −40 dB	−25,3	−23,8	−22,3	dB
		5	TPL = 0 dB	−3,3	−2,3	−1,3	dB
		5	TPL = −20 dB	−18,1	−17,1	−16,1	dB
		5	TPL = −30 dB	−22,6	−21,6	−20,6	dB
		5	TPL = −40 dB	−28,0	−26,5	−25,0	dB

CHARACTERISTICS TEA0652 ONLY

parameter	conditions			min.	typ.	max.	unit
	mode	f(kHz)					
Offset voltage	C	–	$\lvert V_{9\text{-}15}\rvert$	–	10	–	mV
Signal-to-noise ratio (S/N)	C	–	R_S = 10 kΩ (internal) CCIR/ARM weighted; pin 9	72	80	–	dB
Total harmonic distortion (THD)	B	10	TPL = 0 dB	–	0,05	0,1	%
			TPL = + 10 dB	–	0,08	0,3	%
Total harmonic distortion (THD)	C	10	TPL = 0 dB	–	0,1	0,3	%
		1	TPL = + 10 dB	–	0,15	0,5	%
B-mode frequency response	B	1	TPL = −20 dB	−17,3	−15,8	−14,3	dB
		2	TPL = −25 dB	−19,5	−18,0	−16,5	dB
		5	TPL = −40 dB	−30,2	−29,7	−28,2	dB
		10	TPL = −30 dB	−25,0	−23,5	−22,0	dB
C-mode frequency response	C	0,2	TPL = −40 dB	−33,4	−31,9	−30,4	dB
		0,5	TPL = −20 dB	−15,7	−13,7	−11,7	dB
		0,5	TPL = −30 dB	−20,2	−18,2	−16,2	dB
		1	TPL = −20 dB	−16,1	−14,1	−12,1	dB
		1	TPL = −30 dB	−20,1	−18,6	−17,1	dB
		1	TPL = −40 dB	−25,8	−23,8	−21,8	dB
		5	TPL = 0 dB	−3,8	−2,3	−0,8	dB
		5	TPL = −20 dB	−19,1	−17,1	−15,1	dB
		5	TPL = −30 dB	−23,6	−21,6	−19,6	dB
		5	TPL = −40 dB	−28,5	−26,5	−24,5	dB

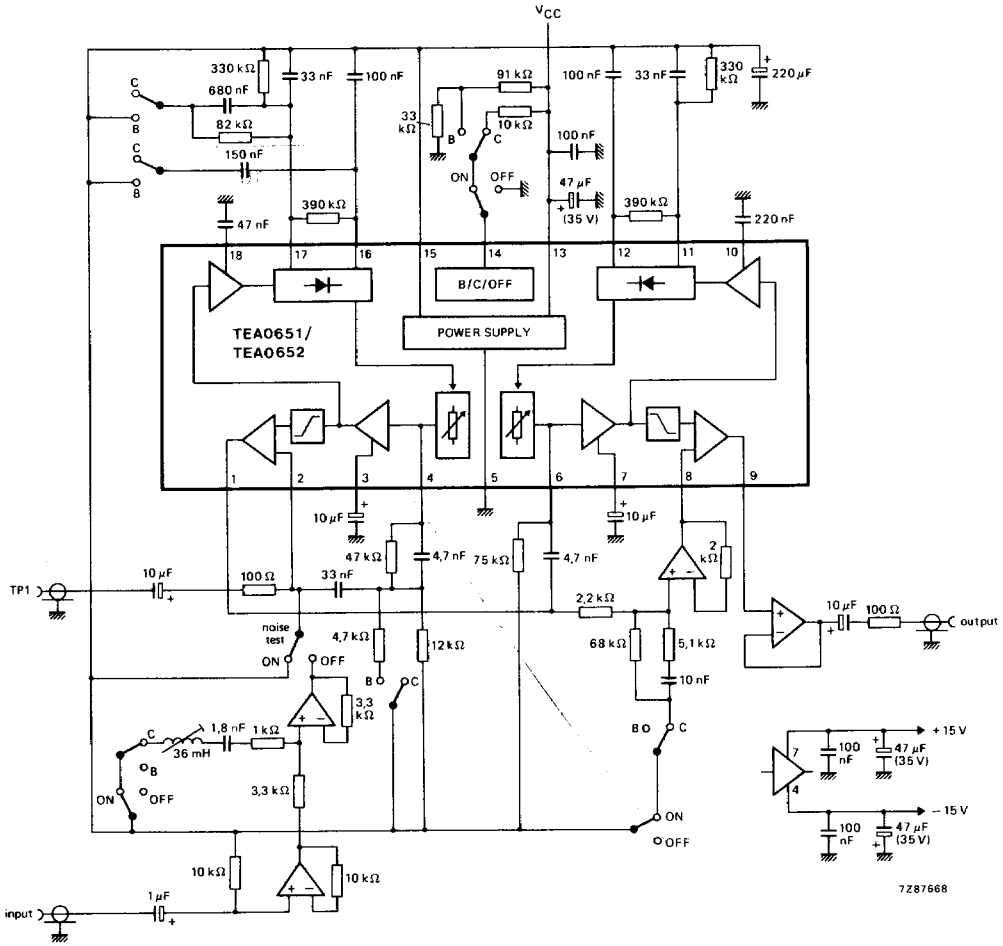


Fig. 13 Test circuit for TEA0651/0652. Encode mode.
Operational amplifiers are NE5535.

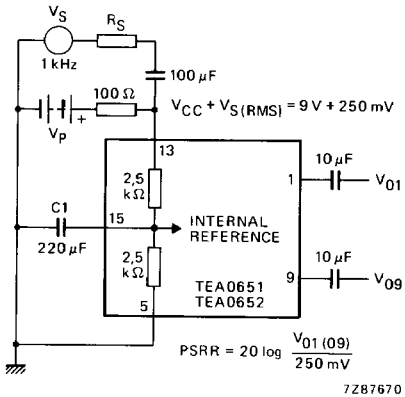


Fig. 14 Test circuit for PSRR for TEA0651/TEA0652.

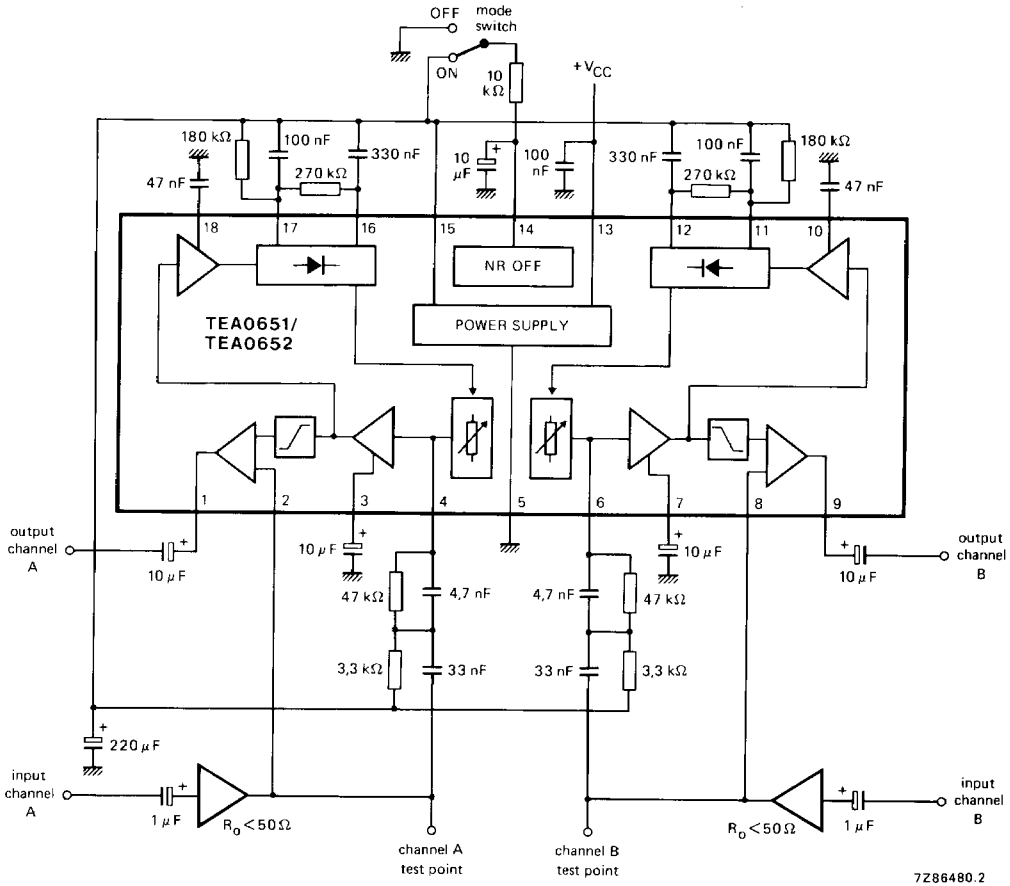


Fig. 15 Test and application circuit of TEA0651/TEA0652 for stereo Dolby B application, shown in encode mode.

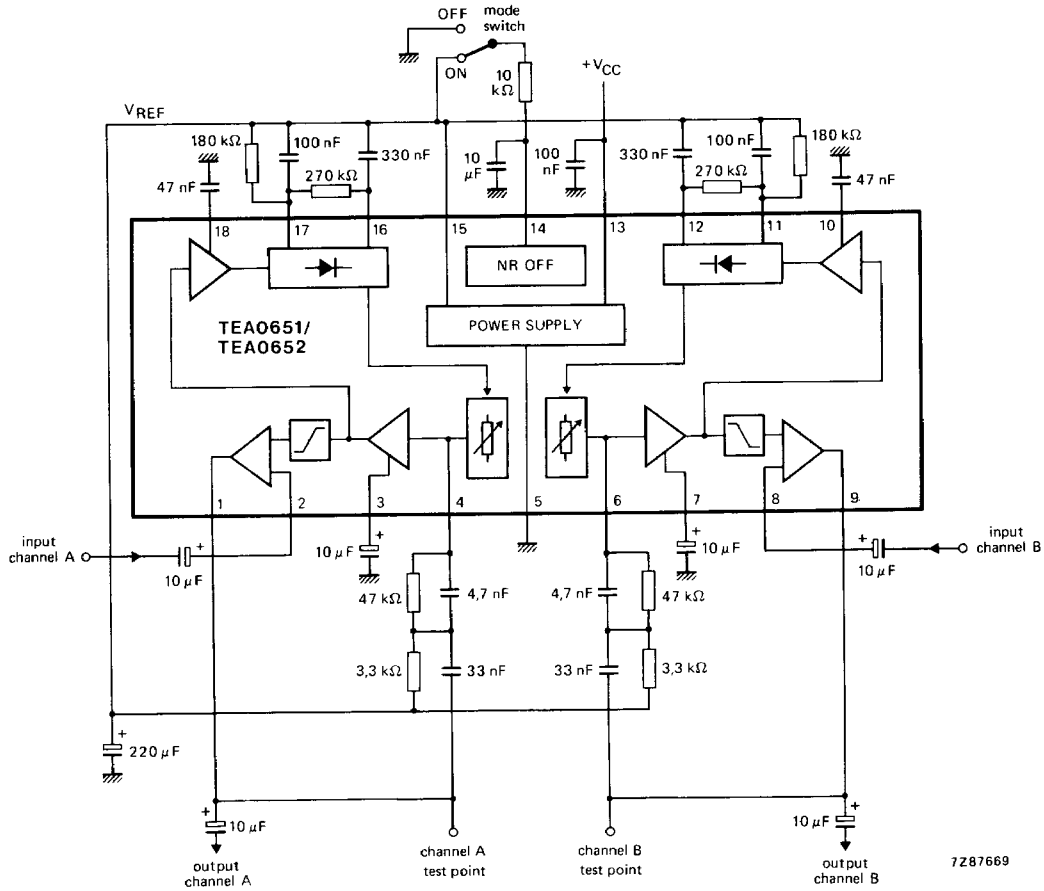


Fig. 16 Typical application circuit for stereo Dolby B noise reduction shown in decode mode.

DATA OF TEA0654 DOLBY B & C TYPE NR SWITCHING CIRCUIT

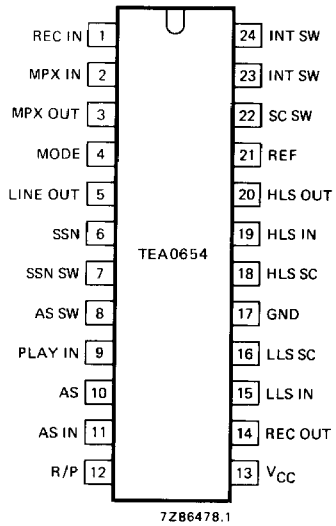


Fig. 17 Pinning diagram of TEA0654.

PINNING

1	REC IN	record input
2	MPX IN	multiplex filter input
3	MPX OUT	multiplex filter output
4	MODE	mode B/C/NR OFF switch input
5	LINE OUT	line output
6	SSN	spectral skewing network
7	SSN SW	spectral skewing network switch
8	AS SW	anti-saturation filter switch
9	PLAY IN	playback input
10	AS	anti-saturation filter
11	AS IN	anti-saturation filter input
12	R/P	record/playback switch input
13	V_{CC}	positive supply voltage
14	REC OUT	record output
15	LLS IN	low level stage main chain input
16	LLS SC	low level stage side chain input
17	GND	d.c. ground
18	HLS SC	high level stage side chain input
19	HLS IN	high level stage main chain input
20	HLS OUT	high level stage output
21	REF	reference voltage
22	SC SW	side chain filter switch
23	INT SW	integrating filter switch
24	INT SW	integrating filter switch

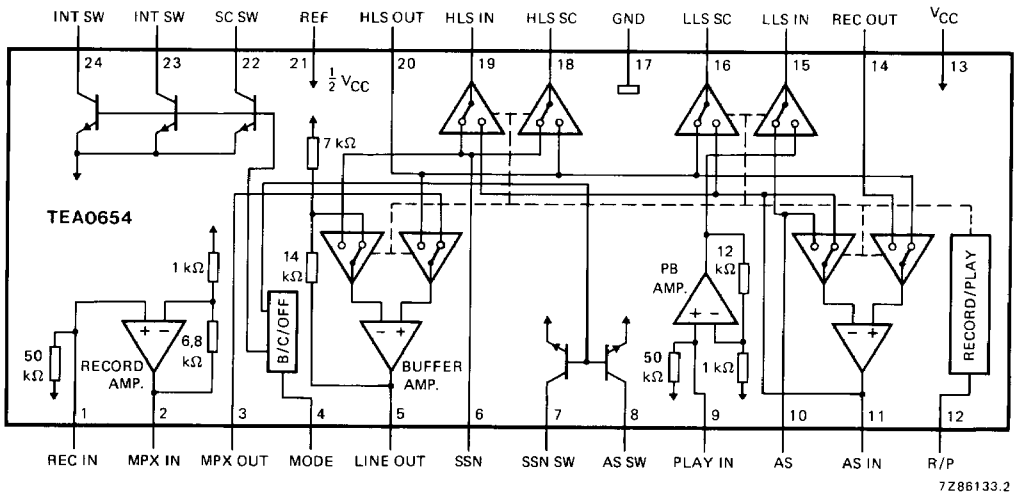


Fig. 18 Block diagram of TEA0654.

CHARACTERISTICS FOR TEA0654

V_{CC} = 14 V; f = 10 kHz; T_{amb} = 25 °C; test circuit Fig. 20; signals referenced to REF (pin 21); d.c. levels with reference to GND (pin 17); unless otherwise specified.

parameter	conditions	min.	typ.	max.	unit
Supply voltage range	V_{CC} (output level at buffer amplifier is + 6 dBm; Dolby level is −6 dBm)	8	14	20	V
Supply current	I_{CC}	11	17	23	mA
Voltage gain of record amplifier	pins 1 to 2	–	17,85	–	dB
Input sensitivity of record amplifier (pin 1)	buffer amplifier output level (pin 5) is 775 mV r.m.s.; MPX filter insertion loss is 4 dB	43	50	58	mV
Voltage gain of playback amplifier	pins 9 to 5	–	22,25	–	dB
Input sensitivity of playback amplifier	buffer amplifier output level (pin 5) is 775 mV r.m.s.	25	30	35	mV
Input resistance	pin 1 and 9	35	50	65	kΩ
Output noise at record output pin 14	R_S = 10 kΩ at pin 1; CCIR/ARM weighted; record mode	–	20	40	μV
Signal handling record and buffer amplifier; pins 2 and 5 (r.m.s. value)	THD = 1%; record mode input level at pin 1	4	–	–	V
Voltage gain of signal switches	record: pins 6 to 14	–	0	–	dB
	playback: pins 14 to 20	–	0	–	dB
Output noise at buffer amplifier pin 5 (r.m.s. value)	R_S = 10 kΩ at pin 9; CCIR/ARM weighted; playback mode	–	65	130	μV
Voltage gain difference between main and side chain op-amp	main chain op-amp output: pins 19 and 15; side chain op-amp output: pins 18 and 16; adjacent op-amps: pins 19 and 18, pins 15 and 16	−0,3	0	+ 0,3	dB
Output noise of signal switches pins 11, 15, 16, 18, 19	R_S = 1 kΩ at pins 6, 14, 20; CCIR/ARM weighted; Fig. 19	–	2,5	–	μV
Signal handling of switches (pin 14) (r.m.s. value)	THD = 1% at pin 14; input level at pin 1	2	–	–	V
Voltage gain of buffer amplifier	pins 3 to 5	–	10	–	dB

parameter	conditions	min.	typ.	max.	unit
Input noise of buffer amplifier pin 3 (r.m.s. value)	R_S = 2,2 kΩ at pin 3; CCIR/ARM weighted; Fig. 19	–	2	–	μV
Signal handling buffer amplifier pin 5 (r.m.s. value)	THD = 1% at pin 5; playback mode; input level at pin 9	4	–	–	V
Output impedance at buffer amplifier pin 5		–	–	100	Ω
Load resistance at buffer amplifier pin 5		10	–	–	kΩ
Load capacitance at buffer amplifier pin 5	For large capacitive loads a series resistor of about 220 Ω is necessary (see Fig. 2)	–	–	200	pF
D.C. switch control levels	playback: pin 12	0	–	1	V
	record: pin 12	$V_{CC}-1$	–	V_{CC}	V
	Dolby-C: pin 4	$¾V_{CC}+1$	–	V_{CC}	V
	Dolby-B: pin 4	0	–	$¾V_{CC}-1$	V

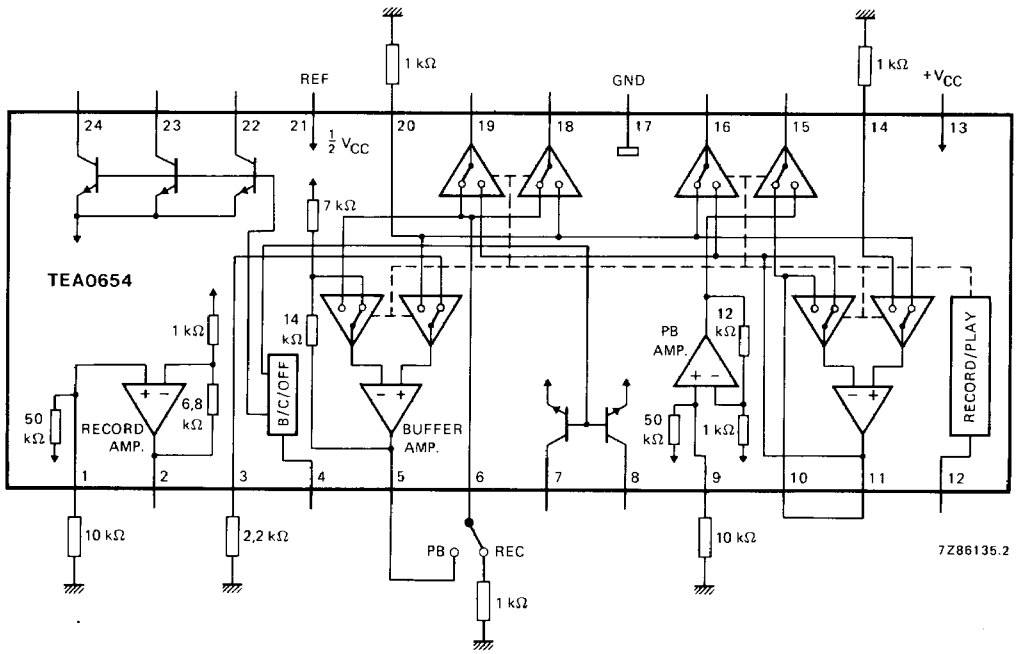


Fig. 19 Test circuit for noise measurements; switch in record position.

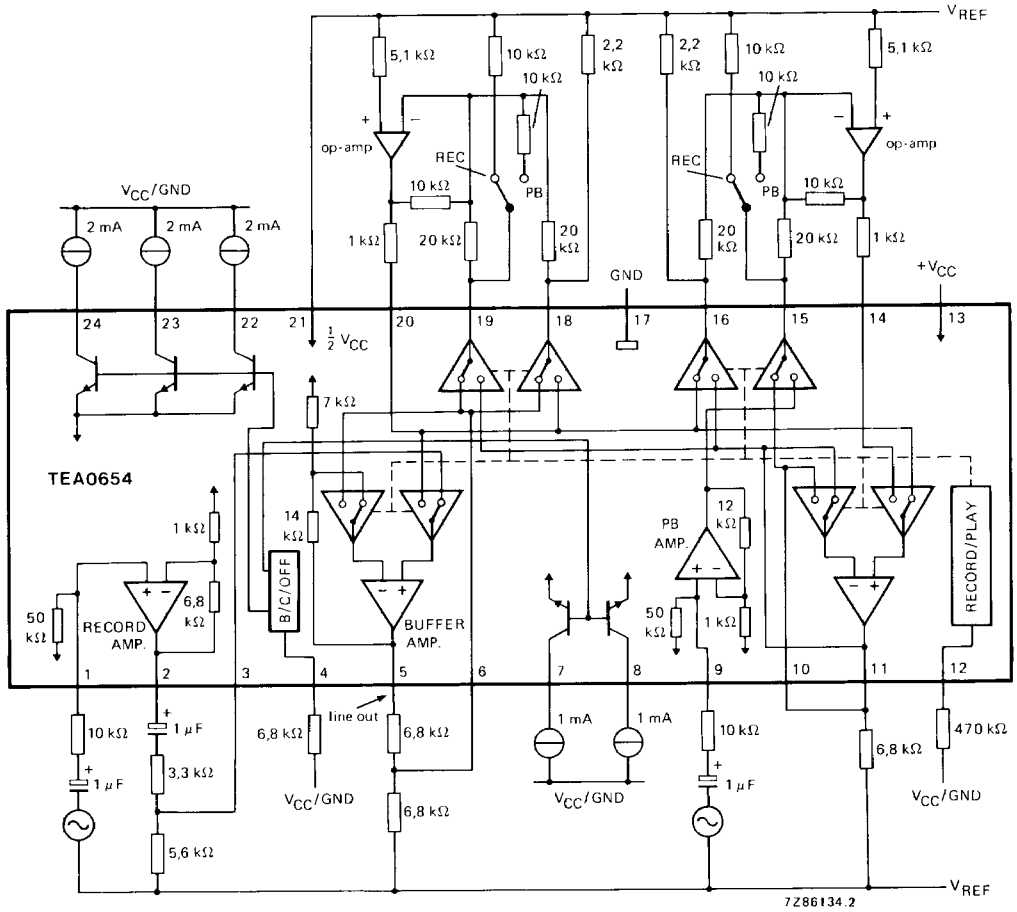


Fig. 20 Test circuit for $V_{CC} \geqslant 11{,}5$ V; switches in record position; external operational amplifier e.g. AD506LH.

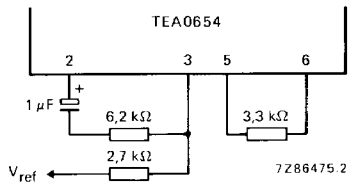


Fig. 21 Modification of Fig. 20 for $V_{CC} \leqslant 11{,}5$ V.