



## DS16149/DS36149, DS16179/DS36179 Hex MOS Drivers

### General Description

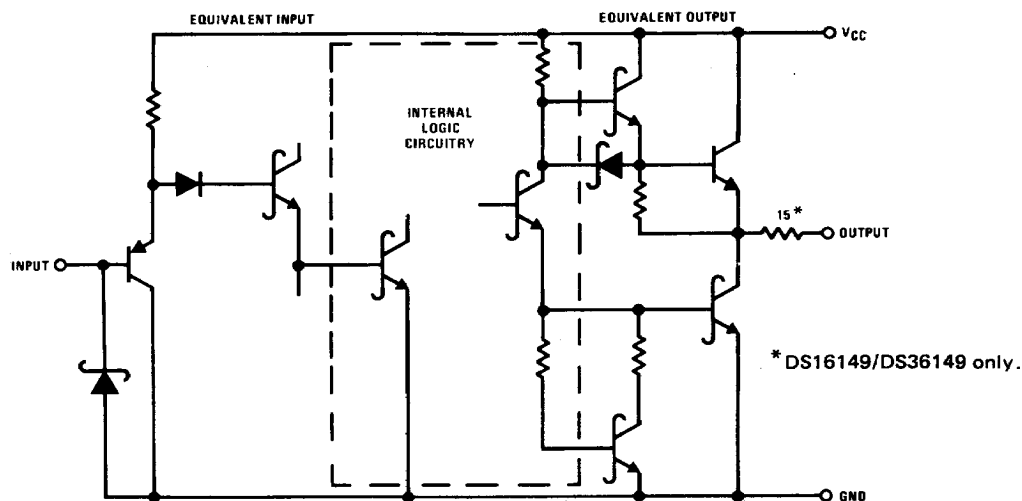
The DS16149/DS36149 and DS16179/DS36179 are Hex MOS drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input currents allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and a disable control that places the outputs in the logic "1" state (see truth table). This is especially useful in MOS RAM applications where a set of address lines has to be in the logic "1" state during refresh.

The DS16149/DS36149 has a 15  $\Omega$  resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS16179/DS36179 has a direct low impedance output for use with or without an external resistor.

### Features

- High speed capabilities
  - Typ 9 ns driving 50 pF
  - Typ 29 ns driving 500 pF
- Built-in 15  $\Omega$  damping resistor (DS16149/DS36149)
- Same pin-out as DM8096 and DM74366

### Schematic Diagram



**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7.0V
Logical "1" Input Voltage	7.0V
Logical "0" Input Voltage	-1.5V
Storage Temperature Range	-65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1371 mW
Molded Package	1280 mW
Lead Temperature (Soldering 10 seconds)	300°C

\*Derate cavity package 9.1 mW/°C above 25°C; derate molded package 10.2 mW/°C above 25°C.

**Operating Conditions**

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	4.5	5.5	V
Temperature ( $T_A$ )			
DS16149, DS16179	-55	+125	°C
DS36149, DS36179	0	+70	°C

**DC Electrical Characteristics** (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
V <sub>IN</sub> (1)	Logical "1" Input Voltage		2.0			V	
V <sub>IN</sub> (0)	Logical "0" Input Voltage				0.8	V	
I <sub>IN</sub> (1)	Logical "1" Input Current	V <sub>CC</sub> = 5.5V, V <sub>IN</sub> = 5.5V		0.1	40	μA	
I <sub>IN</sub> (0)	Logical "0" Input Current	V <sub>CC</sub> = 5.5V, V <sub>IN</sub> = 0.5V		−50	−250	μA	
V <sub>CLAMP</sub>	Input Clamp Voltage	V <sub>CC</sub> = 4.5V, I <sub>IN</sub> = −18 mA		−0.75	−1.2	V	
V <sub>OH</sub>	Logical "1" Output Voltage (No Load)	V <sub>CC</sub> = 4.5V, I <sub>OH</sub> = −10 μA	DS16149/DS16179	3.4	4.3	V	
			DS36149/DS36179	3.5	4.3	V	
V <sub>OL</sub>	Logical "0" Output Voltage (No Load)	V <sub>CC</sub> = 4.5V, I <sub>OL</sub> = 10 μA	DS16149/DS16179		0.25	0.4	V
			DS36149/DS36179		0.25	0.35	V
V <sub>OH</sub>	Logical "1" Output Voltage (With Load)	V <sub>CC</sub> = 4.5V, I <sub>OH</sub> = −1.0 mA	DS16149	2.4	3.5	V	
			DS16179	2.5	3.5	V	
			DS36149	2.6	3.5	V	
			DS36179	2.7	3.5	V	
V <sub>OL</sub>	Logical "0" Output Voltage (With Load)	V <sub>CC</sub> = 4.5V, I <sub>OL</sub> = 20 mA	DS16149		0.6	1.1	V
			DS16179		0.4	0.5	V
			DS36149		0.6	1.0	V
			DS36179		0.4	0.5	V
I <sub>ID</sub>	Logical "1" Drive Current	V <sub>CC</sub> = 4.5V, V <sub>OUT</sub> = 0V, (Note 4)		−250		mA	
I <sub>OD</sub>	Logical "0" Drive Current	V <sub>CC</sub> = 4.5V, V <sub>OUT</sub> = 4.5V, (Note 4)		150		mA	
I <sub>CC</sub>	Power Supply Current	V <sub>CC</sub> = 5.5V	Disable Inputs = 0V All Other Inputs = 3V		33	60	mA
			All Inputs = 0V	14		20	mA

**Switching Characteristics** ( $V_{CC} = 5V, T_A = 25^\circ C$ ) (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{s\pm}$	Storage Delay Negative Edge	(Figure 1) $C_L = 50 pF$		4.5	7	ns
		$C_L = 500 pF$		7.5	12	ns
$t_{s\mp}$	Storage Delay Positive Edge	(Figure 1) $C_L = 50 pF$		5	8	ns
		$C_L = 500 pF$		8	13	ns
$t_F$	Fall Time	(Figure 1) $C_L = 50 pF$		5	8	ns
		$C_L = 500 pF$		22	35	ns

## Switching Characteristics ( $V_{CC} = 5V$ , $T_A = 25^\circ C$ ) (Note 4) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_R$	Rise Time	(Figure 1) $C_L = 50 \text{ pF}$		6	9	ns
		$C_L = 500 \text{ pF}$		26	35	ns
$t_{LH}$	Delay from Disable Input to Logical "1"	$R_L = 2 \text{ k}\Omega$ to Gnd, $C_L = 50 \text{ pF}$ , (Figure 2)		15	22	ns
$t_{HL}$	Delay from Disable Input to Logical "0"	$R_L = 2 \text{ k}\Omega$ to $V_{CC}$ , $C_L = 50 \text{ pF}$ , (Figure 3)		11	18	ns

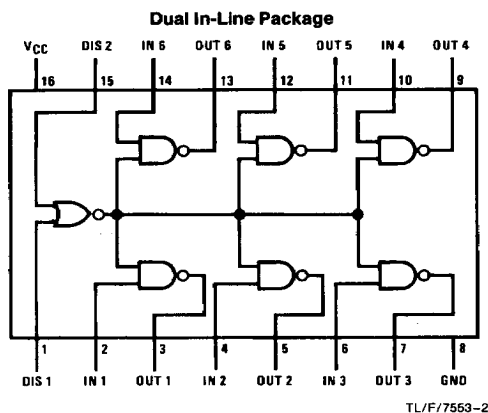
**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** Unless otherwise specified min/max limits apply across the  $-55^\circ C$  to  $+125^\circ C$  temperature range for the DS16149 and DS16179 and across the  $0^\circ C$  to  $+70^\circ C$  range for the DS36149 and DS36179. All typical values are for  $T_A = 25^\circ C$  and  $V_{CC} = 5V$ .

**Note 3:** All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

**Note 4:** When measuring output drive current and switching response for the DS16179 and DS36179 a  $15 \Omega$  resistor should be placed in series with each output. This resistor is internal to the DS16149/DS36149 and need not be added.

## Connection Diagram



Top View

Order Number DS16149J, DS36149J, DS16179J,  
DS36179J, DS36149N or DS36179N  
See NS Package Number J16A or N16A

## Truth Table

Disable Input		Input	Output
DIS 1	DIS2		
0	0	0	1
0	0	1	0
0	1	X	1
1	0	X	1
1	1	X	1

X = Don't care

## AC Test Circuits and Switching Time Waveforms

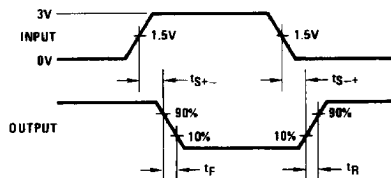
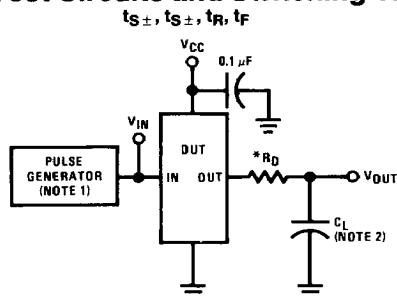


FIGURE 1

TL/F/7553-3

## AC Test Circuits and Switching Time Waveforms (Continued)

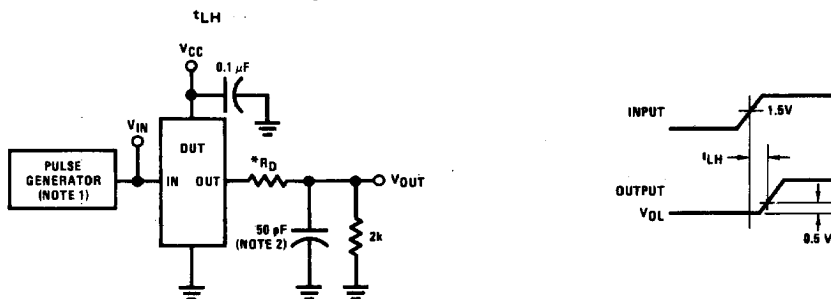


FIGURE 2

TL/F/7553-4

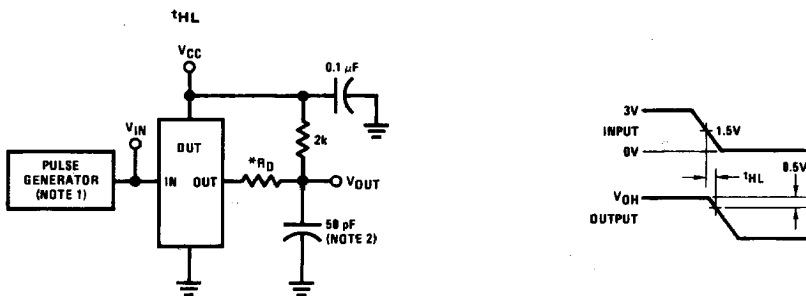


FIGURE 3

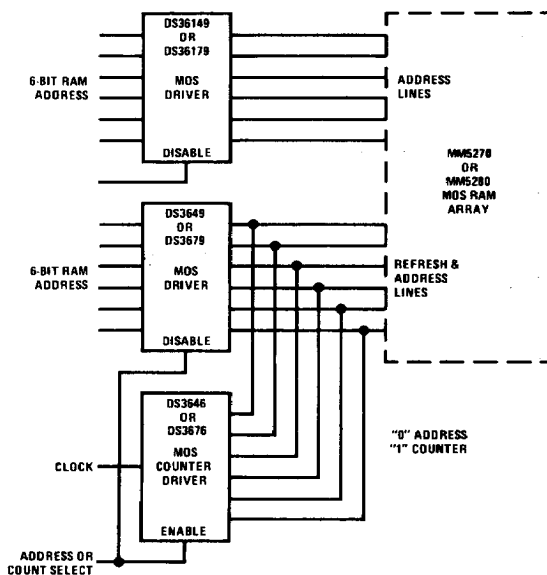
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\*Internal on DS16149 and DS36149

**Note 1:** The pulse generator has the following characteristics:  $Z_{OUT} = 50 \Omega$  and  $PRR \leq 1 \text{ MHz}$ . Rise and fall times between 10% and 90% points  $\leq 5 \text{ ns}$ .

**Note 2:**  $C_L$  includes probe and jig capacitance.

## Typical Applications



TL/F/7553-6