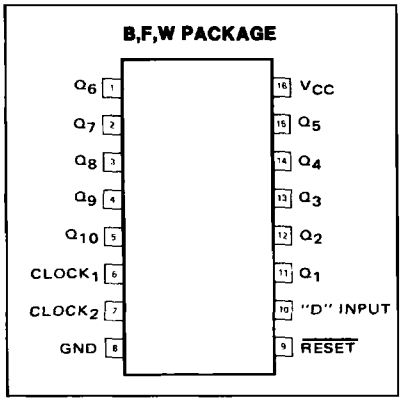
8273-B,F,W

DESCRIPTION

The 8273, 10-Bit Shift Register is an array of binary elements interconnected to perform the serial-in, parallel-out shift function. This device utilizes a common buffered reset and operates from either a positive or negative edge clock pulse. Clock 1 is triggered by a negative going clock pulse and Clock 2 is triggered by a positive going clock pulse. The unused clock input performs the inhibit function. The circuit configuration is arranged as a single serial input register with ten true parallel outputs.

PIN CONFIGURATION

B,F,W PACKAGE

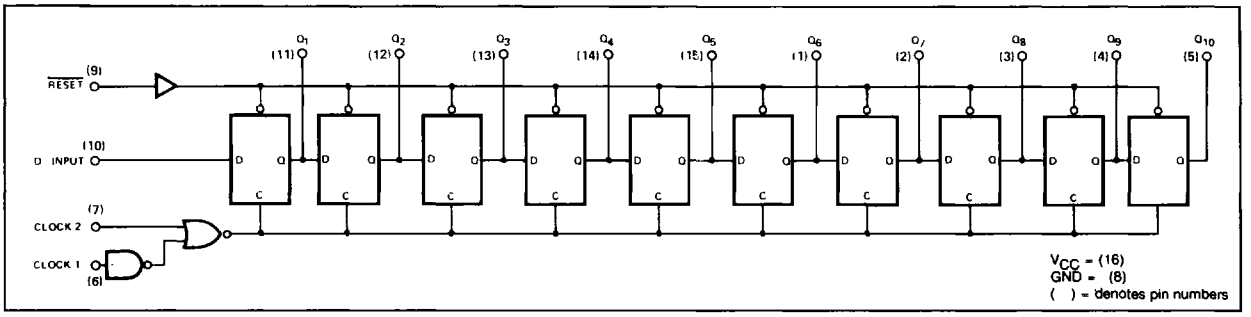


TRUTH TABLE

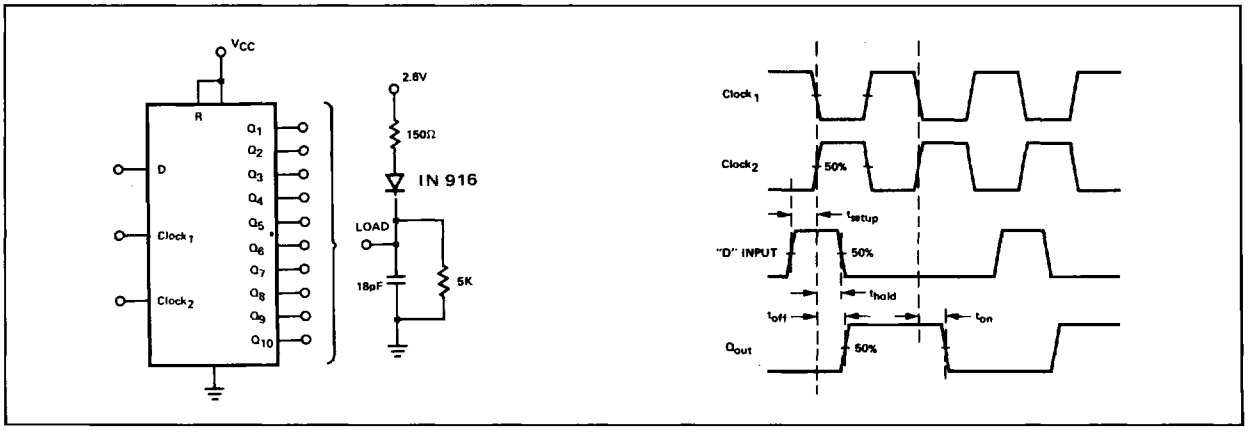
INPUT	$\overline{\text{RESET}}$	CLOCK 1	CLOCK 2	Q_n+1
1	1	Pulse	0	1
0	1	Pulse	0	0
1	1	1	Pulse	1
0	1	1	Pulse	0
1	1	Pulse	1	Q
0	1	Pulse	1	Q
1	1	0	Pulse	Q
0	1	0	Pulse	Q

NOTE:
The unused clock input performs the INHIBIT function.
$\overline{\text{RESET}}$ = 0 → Q = 0

LOGIC DIAGRAM



AC TEST FIGURE AND WAVEFORMS



NOTES:
1. Unused clock 2 input must be grounded.
2. Input pulse characteristics
   CLOCK
   Amplitude = 3.0V
   $t_r = t_f \leq 5$ns.

LOGIC

10-BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER — 8273

8273-B,F,W

SWITCHING CHARACTERISTICS T_A=25°C, V_{CC}=5V

PARAMETER		FROM INPUT	TO OUTPUT	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Data Transfer Rate					25	35		MHz
t_{on}	Turn-on delay	Clock 1		Clock 2 = OV:				
				Reset=4.5V		32	40	
		Clock 2		Reset=4.5V		28	40	ns
		Reset		Clock 1=4.5V		35	50	
t_{off}	Turn-off delay	Clock 1		Clock 2=OV		25	40	ns
		Clock 2		Clock 1=4.5V		19	40	
$t_{w(clock)}$	Width of clock	Clock 1		Clock 2=OV		16	25	ns
	Input pulse	Clock 2		Clock 1=4.5V		12	20	
t_{set-up}	Setup time	Clock 1		Clock 2=OV			15	ns
		Clock 2		Clock 1=4.5V			10	
t_{hold}	Hold time	Clock 1		Clock 2=OV			15	ns
		Clock 2		Clock 1=4.5V			10	

10-BIT PARALLEL-IN SERIAL-OUT SHIFT REGISTER — 8274

8274-B,F,W

DESCRIPTION

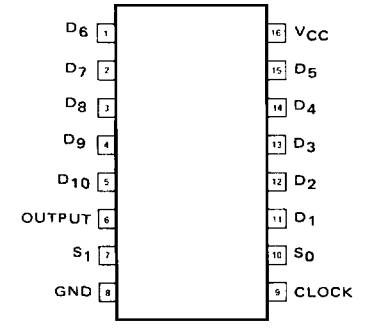
The 8274 10-Bit Shift Register is an array of binary elements interconnected to perform the parallel-in serial-out shift function. The circuit has ten parallel inputs and a single true serial output. The D_1 input can also be used for serial entry. Two control inputs, S_0 and S_1, determine the operating mode of the shift register as shown in the Truth Table. A single buffered clock line connects all ten flip-flops which are activated on the high-to-low transition of the clock pulse. Guaranteed input clock frequency is 25MHz. With the exception of the Hold Mode, the control inputs may be changed when the clock is in either the high or low state without causing false triggering. The Hold Mode can be entered only when the clock is low. Applications for the 8274 Shift Register include Parallel-to-Serial conversion, Modem Data Transmision, Pseudo-Random Code generation and Modulo-N Frequency Division.

TRUTH TABLE

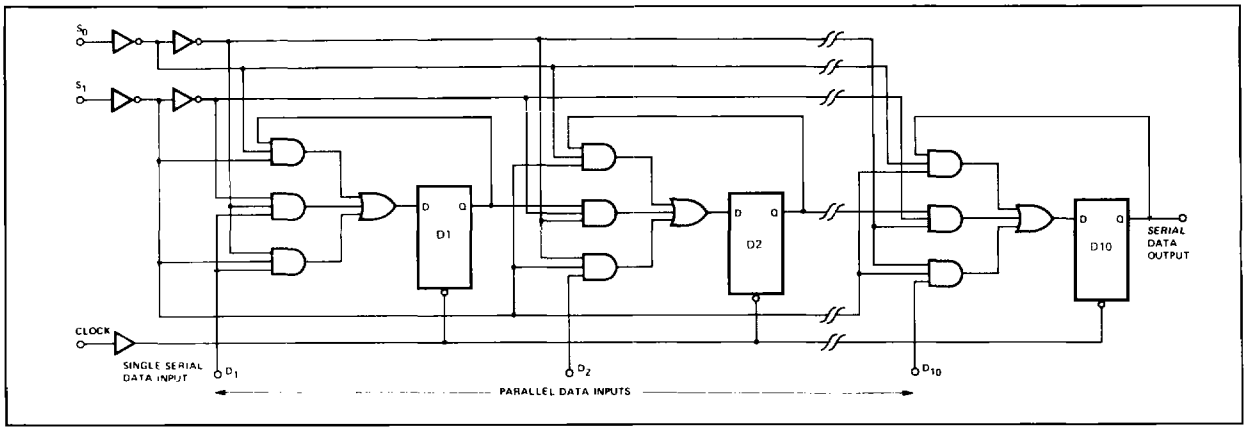
S_0	S_1	OPERATING MODE
0	0	Hold
0	1	Clear
1	0	Load
1	1	Shift

PIN CONFIGURATION

B,F,W PACKAGE



LOGIC DIAGRAM



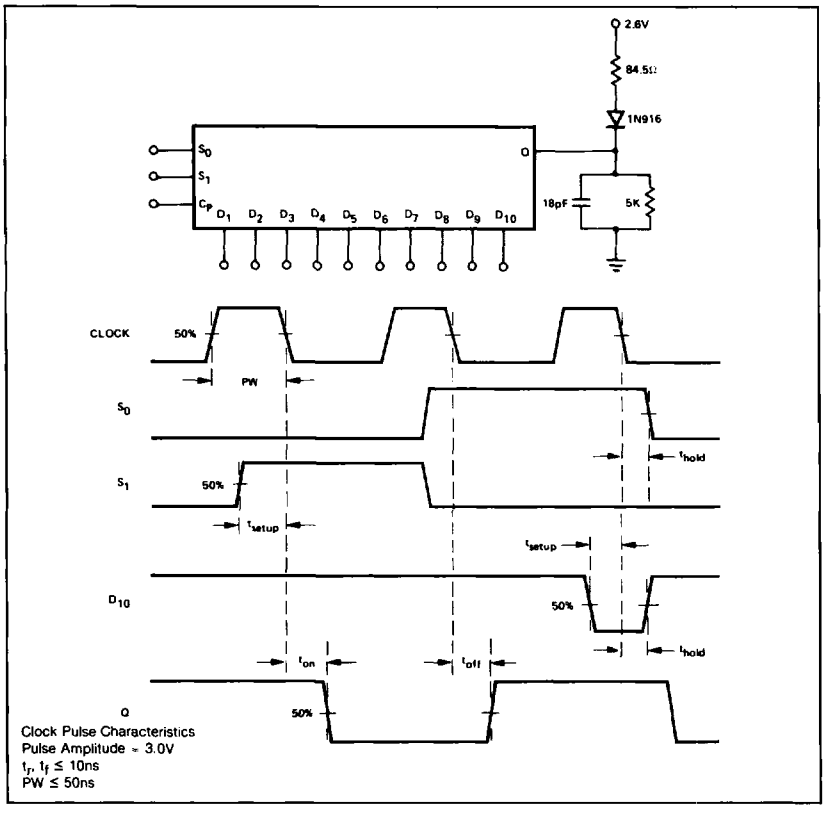
signetics

8274-B,F,W

SWITCHING CHARACTERISTICS T_A=25°C, V_{CC}=5V

PARAMETER		LIMITS MIN	TYP	MAX	UNIT
Data Transfer Rate		25	30		MHz
t_{on}	Turn-on delay				
	Clock to output		27	40	ns
t_{off}	Turn-off delay				
	Clock to output		21	40	ns
t_w	Width of clock pulse		15	20	ns
t_{setup}	Setup time				
	D_n		16	10	ns
	S_0, S_1		16	25	

AC TEST FIGURE AND WAVEFORMS



Clock Pulse Characteristics
Pulse Amplitude = 3.0V
t_r, $t_f \leq$ 10ns
PW ≤ 50ns

LOGIC