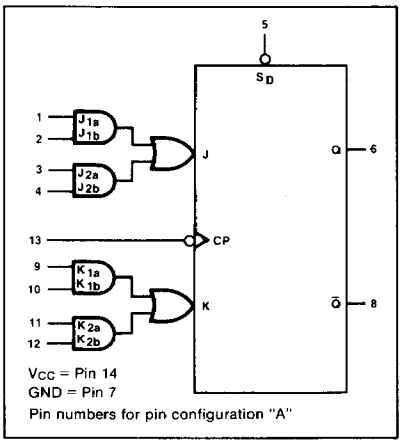
54H/74H101

DESCRIPTION

The "101" is a JK Negative Edge-Triggered Flip-Flop featuring AND-OR gated JK inputs and a direct Set input. The Set ($\overline{S}_D$) is an asynchronous active LOW input. When LOW, the $\overline{S}_D$ overrides the clock and data inputs and sets the Q output HIGH and the $\overline{Q}$ output LOW.

A HIGH level on the Clock ($\overline{CP}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may change while the $\overline{CP}$ is HIGH, and the flip-flop will perform according to the Truth Table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of $\overline{CP}$.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7
Pin numbers for pin configuration "A"

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = -55°C to +125°C
Plastic DIP	Fig. A	N74H101N	
Ceramic DIP	Fig. A	N74H101F	S54H101F
Flatpak	Fig. B		S54H101W

PIN CONFIGURATIONS

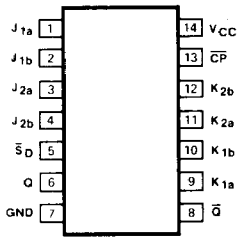


Figure A

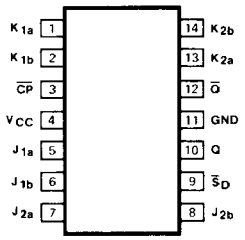


Figure B

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE (a)

PINS			54/74	54H/74H	54S/74S	54LS/74LS
$\overline{CP}$	Clock input	I_{IH} (μA) I_{IL} (mA)		-1.0 -4.8		
$\overline{S}_D$	Set input	I_{IH} (μA) I_{IL} (mA)		100 -2.0		
JK	Data inputs	I_{IH} (μA) I_{IL} (mA)		50 -2.0		
Q & $\overline{Q}$	Outputs	I_{OH} (μA) I_{OL} (mA)		-500 20		

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (b)

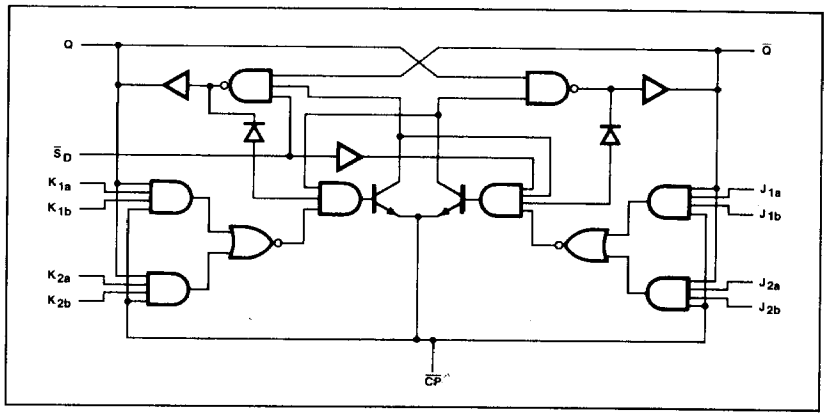
PARAMETER		TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
I_{IH} ($\overline{CP}$)	Input HIGH current	V_{CC} = Max, V_{CP} = 2.4V			0	-1.0					mA
I_{CC}	Supply current	V_{CC} = Max, V_{CP} = 0V				38					mA

NOTES

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H and see inside back cover for 54S/74S and 54LS/74LS specification.

LOGIC DIAGRAM



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous Set	L	X	X	X	H	L
Toggle	H	↓	h	h	$\overline{q}$	q
Load "0" (Reset)	H	↓	l	h	L	H
Load "1" (Set)	H	↓	h	l	H	L
Hold "no change"	H	↓	l	l	q	$\overline{q}$

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.
l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.
J = $(J_{1a} \bullet J_{1b}) + (J_{2a} \bullet J_{2b})$
K = $(K_{1a} \bullet K_{1b}) + (K_{2a} \bullet K_{2b})$

AC CHARACTERISTICS T_A = 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER		TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
					C_L = 25 pF, R_L = 280Ω						
			Min	Max	Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 4			40						MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 4				15 20					ns ns
t_{PLH}	Propagation delay Set to output	Waveform 5				12					ns
t_{PHL}		Waveform 5, CP = HIGH				20					ns
t_{PHL}		Waveform 5, CP = LOW				35					ns

AC SETUP REQUIREMENTS T_A = 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER		TEST CONDITIONS	54/74		54H/74H		54S/74S		54LS/74LS		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{W(H)}$	Clock pulse width (HIGH)	Waveform 4			10						ns
$t_{W(L)}$	Clock pulse width (LOW)	Waveform 4			15						ns
$t_{W(L)}$	Set pulse width (LOW)	Waveform 5			16						ns
$t_{s(H)}$	Setup time HIGH J or K to Clock	Waveform 4			10						ns
$t_{h(H)}$	Hold time HIGH J or K to Clock	Waveform 4			0						ns
$t_{s(L)}$	Setup time LOW J or K to Clock	Waveform 4			13						ns
$t_{h(L)}$	Hold time LOW J or K to Clock	Waveform 4			0						ns